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INTEGRATED AND DISCRETE

SEMICONDUCTORS

Allegro™ MicroSystems Inc.

AMS-500

INTEGRATED AND DISCRETE

SEMICONDUCTORS

Applications for

- EDP Peripherals
- Industrial Control
- Military
- Automotive
- Consumer
- Aerospace

Allegro MicroSystems, Inc.

Formerly Sprague Semiconductor Group

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(508) 853-5000

Data Book AMS-500
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GENERAL INFORMATION

ALLEGRO MICROSYSTEMS, INC.

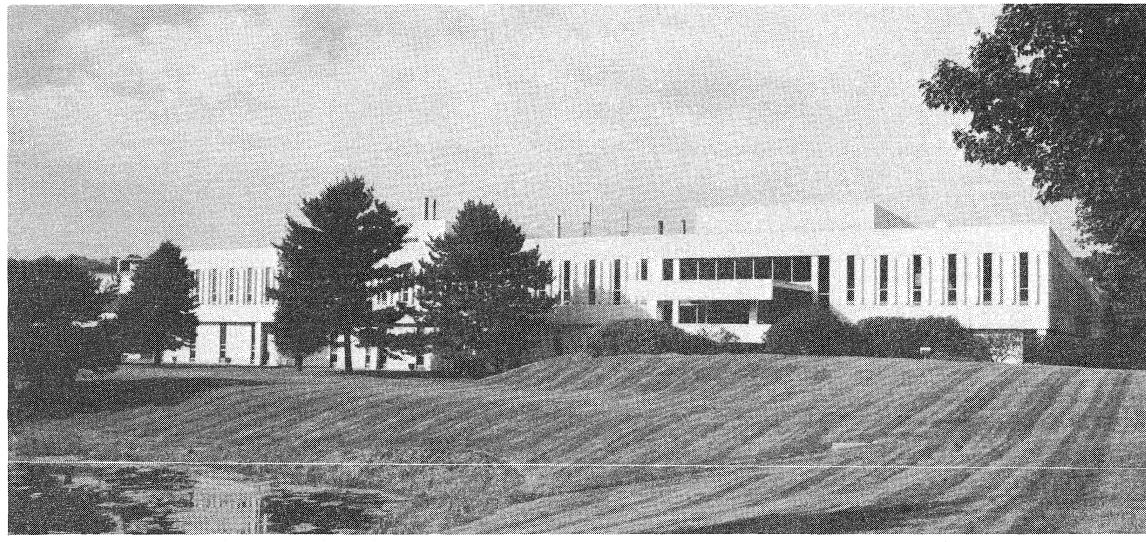
MISSION STATEMENT

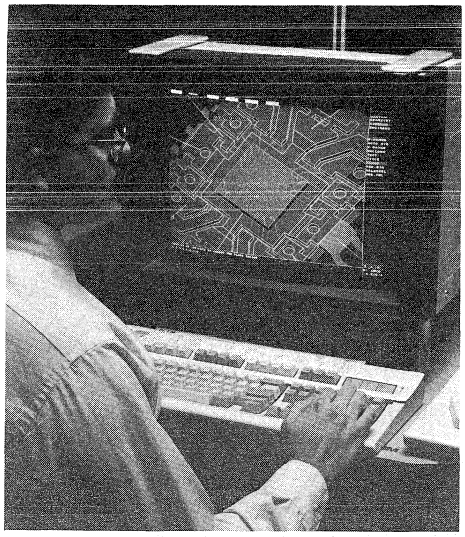
Allegro MicroSystems, Inc. is dedicated to providing value-added solutions to meet our customers' complex electronic systems needs through the design of mixed-signal integrated circuits that improve the performance, quality, and reliability of their end product. The measurements of our success will be customer satisfaction, market leadership, and profitability that meets the needs and expectations

Allegro MicroSystems, Inc. specializes in the design, manufacture, and marketing of advanced mixed-signal (analog + digital) integrated circuits as well as a line of discrete transistors and diodes. Allegro, formerly the Sprague Semiconductor Group of Sprague Electric Co., combines over 25 years of semiconductor experience, over a decade of extensive merged-technologies experience, and worldwide resources in design and applications engineering, process technology, packaging, quality control, manufacturing, and testing.

As a "mature start-up" re-named in July 1990, Allegro is well positioned to accelerate its growth as a leading supplier of mixed-signal solutions as it emphasizes system-level ICs for original equipment manufacturers primarily serving the computer peripherals, automotive, consumer, and industrial markets. Allegro's strengths center on an excellent track record in product quality and innovation, and a diversified base of major OEM customers. The company's reputation for quality spans both product design and manufacturing. This reputation is evident in the preferred vendor/ship-to-stock programs it has secured with several major customers. Allegro, also recognized as "Vendor of the Year" by Northern Telecom, is one of the few semiconductor firms to receive Ford Motor Company's Q-1 quality award, and is the only US IC manufacturer to have received IECQ manufacturer's approval.

Headquartered in Worcester, Massachusetts, Allegro currently operates two wafer-fabrication plants in Worcester and Willow Grove, Pennsylvania, as well as assembly/test operations in the Philippines.





Recently, Allegro has shifted from being product- or engineering-driven to being a market-driven company. This move has sharpened the company's focus on application-specific standard products and application-specific custom products for selected growth market segments. Allegro's product expertise in power ICs, signal processing ICs, and sensor ICs—believed to be unique in the industry—is supported by strong capabilities in bipolar, CMOS, and DMOS process technologies. Allegro can and does combine any two or all three of its product disciplines (and/or process technologies) in a single monolithic chip to deliver powerful system-level solutions. While the company is vigorously establishing itself as a significant supplier of mixed-signal ICs, it will continue to serve as a supplier of power and smart power ICs, Hall-effect sensors, and discrete devices.

Within the worldwide semiconductor market, Allegro has strategically positioned itself in the analog segment. Allegro primarily serves the analog IC industry through the development, manufacture, and marketing of a wide variety of complex products. The company emphasizes application-specific, market-driven products with high technology content. These include bipolar, CMOS, and DMOS technologies, as well as merged technologies such as BiCMOS (bipolar + CMOS), BCD (bipolar + CMOS + DMOS), and DABIC (digital + analog + BiCMOS). Original designs are emphasized, rather than second source products, in order to command a higher value in the marketplace. Many of these original designs have ultimately become industry standard products, such as the company's popular Hall-effect switches and power drivers.

Increased performance, market-specific features, higher levels of integration, and overall system cost reduction have become increasingly critical to maintain and extend a competitive advantage. Because of the strength of this fundamental trend among leading manufacturers, a significant segment of the analog IC market is changing from a "commodity-oriented/low-value-added" business to one that is "high-complexity/high value-added".

OEMs expect vendors to add tangible value at a system level because they need to maximize performance and speed time to market. Applications, design, and technology consultation provided by IC suppliers, therefore, become crucial, as does the working synergy between the two design partners. OEMs also need to feel confident in their IC supplier's ability to control the manufacturing and testing processes, thereby ensuring quality, reliability, and consistent delivery.

Allegro's top 25 customers account for approximately 50 percent of sales, with no single customer accounting for more than 10 percent.

Allegro is exceptionally positioned to serve each customer's system requirements with either application-specific custom products or a broad spectrum of application-specific standard products, including power, smart power, sensor, discrete, and signal-processing products.

Analog ICs can generally be separated into three classifications: sensor, signal processing, and power ICs. Sensors are analog ICs which respond to physical phenomena and provide inputs to an electronic system. Signal processing ICs represent a broad category of analog ICs which accept, generate, or process an analog signal. Power ICs are those products which act as the interface from an electronic system back to the physical world. These products typically operate at voltages and currents well in excess of those applied to other parts of the electronic system due to their requirement to drive motors, displays, solenoids, relays, lamps, and other devices.

Allegro is also the world leader in power and Hall-effect sensor package technology by employing innovative optimization approaches to significantly improve established packages. Even though Allegro's device packaging conforms to industry standards, the company has developed improvements to packaging materials and construction so that its devices substantially exceed the industry-standard specifications for allowable package power dissipation and long-term reliability.

GENERAL INFORMATION

DEFINITION OF TERMS

ABSOLUTE MAXIMUM RATINGS are limiting values of operation and should not be exceeded under the worst conditions. These values are chosen to provide acceptable serviceability of the device. The equipment manufacturer should design so that initially, and throughout life, no absolute maximum value is exceeded.

The absolute maximum output current ratings are the maximum allowable under any condition. In application, output current will be limited by number of outputs conducting, duty cycle and timing, ambient temperature, heat sinking and/or forced cooling, and other heat sources.

Under any set of conditions, the specified maximum junction temperature (usually +150°C) should not be exceeded. In those devices which include an internal thermal shutdown, fault conditions which produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

TYPICAL CHARACTERISTICS are given for circuit design information only and, unless otherwise stated, are usually given at the nominal operating voltage and an ambient temperature of +25°C. Although these values are indicative of the peak distribution for a large number of production lots, these values should not be construed as guaranteed for any particular device or production lot.

CHARACTERISTICS LIMITS are those values that are guaranteed under the test conditions shown.

The absolute magnitude convention is used for **Electrical Characteristics Limits** where the limits are defined as:

> maximum [minimum] limit: the greater [smaller] magnitude limit of a range of like-signed values; if the range includes both positive and negative values, both limiting values are maximums [the minimum is implicitly zero].

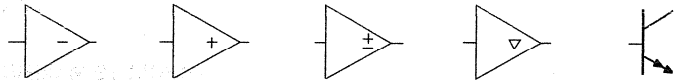
The algebraic convention is used for **Magnetic Characteristics Limits** where negative flux densities are defined as less than zero. The minimum value is therefore the most negative value, the maximum value is the most positive value, and zero has no special significance.

RECOMMENDED OPERATING CONDITIONS are given for optimum device performance. Operation outside these conditions is permitted (within the Absolute Maximum Ratings) without any implied guarantee of level of performance.

It is recommended that equipment manufacturers consult their local sales office whenever device applications involve unusual electrical, mechanical, or environmental operating conditions.

DEFINITION OF TERMS

SPECIAL SYMBOLS are sometimes used to simplify circuit drawings.



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ADVANCE INFORMATION is used to advise customers of proposed additions to the product line. The specifications given are target or goal specifications and may, therefore, change without notice. Allegro MicroSystems, Inc. reserves the right to not manufacture these proposed devices which have been announced as "advance information". Contact your local sales office for details of current status and latest specifications.

PRELIMINARY INFORMATION is issued to advise customers of additions to the product line which, nevertheless, still have "pre-production" status. Details may, therefore, change without notice although it is expected that the performance data is representative of "full production" status. Contact your local sales office for details of current status and latest specifications.

IMPORTANT NOTICE

Allegro MicroSystems, Inc., reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Changes and improvements made after the publication of this catalog will be reflected in updated data sheets or other literature as soon as possible. Components made under military approvals will be in accordance with the approval requirements.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Allegro MicroSystems, Inc. reserves the right to discontinue any device without notice.

Before placing an order, Allegro advises its customers to obtain the latest version of the relevant information to verify that the information being relied upon is current.

Allegro products are not intended for use in life support appliances, devices, or systems. Use of an Allegro product in such applications without the written consent of Allegro MicroSystems, Inc. is prohibited.

DEVICE PART-NUMBERING

ALLEGRO MICROSYSTEMS NEW PART NUMBERS

A 8958 S EA F-1

Instructions (optional; in the order listed).
- F = Active pull-down device (BiMOS only)
- -1 = (Any number except 883) Selected version, see detail specification
- BU = Burned-In parts to Double-Deuce program*
- MIL = Military grade, non-compliant, with screening to MIL-STD-883, Class B*
- 883 = Military grade, compliant with screening to MIL-STD-883, Class B*
- BS = Compliant, with screening to BS9493*
- TR = Tape and reel (surface-mount devices only)

Package Designation.
- A = Plastic, dual in-line
- B = Plastic, dual in-line semi-tab
- C = Unpackaged chip †
- CT = Unpackaged chip, tray-packed †
- CW = Probed wafer †
- EA = Plastic, leaded chip carrier, one semi-tab
- EB = Plastic, leaded chip carrier, two semi-tabs
- EK = Hermetic, leadless chip carrier
- EP = Plastic, leaded chip carrier
- H = Hermetic, metal-sealed co-fired ceramic dual in-line
- HH = Hermetic, ceramic, 3-lead single in-line (TO-260AA)
- K = Plastic, 4-lead mini-SIP
- KA = Plastic, 5-lead mini-SIP
- L = Plastic, SOIC
- LB = Plastic, wide-body SOIC power tab
- LL = Plastic, SOT-89, long-lead version
- LT = Plastic SOT-89/TO-243AA
- LW = Plastic, wide-body SOIC
- M = Plastic, 8-pin mini-DIP
- R = Hermetic, glass-sealed ceramic dual in-line
- T = Plastic, 3-lead mini-SIP
- U = Plastic, 3-lead thin mini-SIP
- UA = Plastic, short 3-lead thin mini-SIP
- V = Hermetic, 15-pin metal flange mount (MO-097AA)
- W = Plastic, 12-lead single in-line power tab
- X = Special
- Z = Plastic, 5-lead single in-line power tab (TO-220)
- ZH = Z Package with formed leads for horizontal mount
- ZV = Z Package with formed leads for vertical mount

Operating Temperature Range.
- C = Commercial (0°C to +70°C)
- S = Standard (-20°C to +85°C)
- E = Extended automotive/industrial (-40°C to +85°C)
- K = Industrial/military (-40°C to +125°C)
- L = Automotive/military (-40°C to +150°C)
- M = Military (-55°C to +125°C)
- X = Special (i.e., wafer probe at +25°C only)

Device Type (four digits).

Allegro MicroSystems Identifier.

* Instruction suffix 'BU' available only with temperature codes 'S', 'E', 'K, or 'L'; suffixes 'MIL' or '883' available only with temperature code 'M'; suffix 'BS' available only through European sales office.

† Discrete and integrated circuit chips are described in Brochure CN-193.

DEVICE PART-NUMBERING

ORIGINAL SPRAGUE SEMICONDUCTOR GROUP PART NUMBERS

UC N 5810 A F-1

Instructions (optional; in the order listed).
- F = Active pull-down device (BiMOS only)
- -1 = (Any number except 883) Selected version, see detail specifications
- BU = Burned-In device to Double-Deuce program*
- MIL = Military grade, non-compliant, with screening to MIL-STD-883, Class B*
- 883 = Military grade, compliant, with screening to MIL-STD-883, Class B*
- BS = Compliant, with screening to BS9493*

Package Designation.
- A = Plastic, dual in-line
- B = Plastic, dual in-line semi-tab
- C = Unpackaged chip †
- CT = Unpackaged chip, tray-packed †
- CW = Probed wafer †
- EA = Plastic, leaded chip carrier, one semi-tab
- EB = Plastic, leaded chip carrier, two semi-tabs
- EK = Hermetic, leadless chip carrier
- EP = Plastic, leaded chip carrier
- H = Hermetic, metal-sealed co-fired ceramic dual in-line
- HH = Hermetic, ceramic, 3-lead single in-line (TO-260AA)
- K = Plastic, 4-lead mini-SIP
- KA = Plastic, 5-lead mini-SIP
- L = Plastic, SOIC
- LB = Plastic, wide-body SOIC power tab
- LL = Plastic, SOT-89, long-lead version
- LT = Plastic SOT-89/TO-243AA
- LW = Plastic, wide-body SOIC
- M = Plastic, 8-pin mini-DIP
- R = Hermetic, glass-sealed ceramic dual in-line
- T = Plastic, 3-lead mini-SIP
- U = Plastic, 3-lead thin mini-SIP
- UA = Plastic, short 3-lead thin mini-SIP
- V = Hermetic, 15-pin metal flange mount (MO-097AA)
- W = Plastic, 12-lead single in-line power tab
- X = Special
- Z = Plastic, 5-lead single in-line power tab (TO-220)
- ZH = Z Package with formed leads for horizontal mount
- ZV = Z Package with formed leads for vertical mount

Device Type (four digits).

Operating Temperature Range.
- N = Commercial/industrial
- Q = Extended automotive/industrial
- S = Military

Family (UC, UD, UG, UL, or UM).

* Instruction suffix 'BU' available only with temperature codes 'N' or 'Q'; suffixes 'MIL' or '883' available only with temperature code 'S'; suffix 'BS' available only through European sales office.

† Discrete and integrated circuit chips are described in Brochure CN-193.

DEVICE PART-NUMBERING

ORIGINAL SPRAGUE SEMICONDUCTOR GROUP PART NUMBERS

TIC 6118 -2 FM

Shipping style (TIC prefix only).
- FM = Wafer sawn on frame
- TS = Tray pack
- WA = Whole wafer

Instructions (optional).

Device Type (three or four digits).

Family.
- BA- = Pro-Electron registered diode
- BC- = Pro-Electron registered diode
- BZ- = Pro-Electron registered Zener diode
- TH-* = Unpackaged discrete device chip †
- TIC = Integrated circuit chip or probed wafer †
- TMP-* = SOT-23/TO-236AB packaged discrete device
- TND = Diode array
- TP = Bipolar transistor in TO-92/TO-226AA/AB
- TPP = Darlington array
- TPQ = Quad transistor array
- 2N = JEDEC registered transistor

* D = diode T = transistor
F = JFET Z = Zener

†Discrete and integrated circuit chips are described in Brochure CN-193.

MILITARY PART NUMBERS

85500 01 C C

5962 - 86058 01 M V C

Lead Finish.
- A = Solder dip
- C = Gold plate
- X = Any (A or C acceptable by user)

Package Designation.
- C = Hermetic, metal-sealed co-fired ceramic 14-pin dual in-line
- E = Hermetic, metal-sealed co-fired ceramic 16-pin dual in-line
- V = Hermetic, metal-sealed co-fired ceramic 18-pin dual in-line
- 2 = Hermetic, metal-sealed co-fired ceramic 20-terminal chip carrier

Device Class.
- M = Monolithic integrated circuit (optional for drawing numbers below 90000)

Device Type.

Drawing Number.
(first two digits are year of issuance except that '38' indicates MIL-M-38510 device with remaining digits indicating the slash sheet).

Standardized Military Drawing Program Designator
(Drawing numbers higher than 86000; not used for DESC drawing numbers below 86000).

All possible combinations of device type, operating temperature range, and package style are not necessarily available. Consult individual device specification or sales office for complete information.

GENERAL INFORMATION

ORDERING INFORMATION

To place an order, obtain price and delivery information, or to request technical literature, contact your local Allegro sales office or sales representative. See back of book, or:

From United States and Canada	Allegro MicroSystems, Inc. 115 Northeast Cutoff Box 15036 Worcester, MA 01615 Tel: (508) 853-5000 Fax: (508) 853-5049
From Europe and Mideast	Allegro Europe Ltd. Balfour House, Churchfield Road Walton-on-Thames, Surrey KT12 2TD UNITED KINGDOM Tel: (44-932) 253-355 Fax: (44-932) 246-622
From Asia	Allegro MicroSystems Philippines, Inc. Sampaguita Street, Marimar Village Parangue, Metro Manila 1700 PHILIPPINES Tel: (63-2) 828-9026 Fax: (63-2) 828-4045

TECHNICAL ASSISTANCE

Requests for additional technical information or applications assistance should be referred to your local Allegro sales office or sales representative. See back of book, or:

For Integrated Circuits	Allegro MicroSystems, Inc. 115 Northeast Cutoff Box 15036 Worcester, MA 01615 Tel: (508) 853-5000 Fax: (508) 853-5049
For Sensors and Discrete Devices	Allegro MicroSystems, Inc. 53 Regional Drive Concord, NH 03301 Tel: (603) 228-5533 Fax: (603) 224-2466

INTEGRATED CIRCUITS AND TRANSISTOR ARRAYS

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* Complete part number includes additional characters to indicate operating temperature range and package style. See detailed specification.

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* Complete part number includes additional characters to indicate operating temperature range and package style. See detailed specification.

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* Complete part number includes additional characters to indicate operating temperature range and package style. See detailed specification.

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* Complete part number includes additional characters to indicate operating temperature range and package style. See detailed specification.

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PERIPHERAL POWER AND DISPLAY DRIVERS

Sections 3 and 5, unless otherwise indicated

IN ORDER OF 1) OUTPUT CURRENT, 2) OUTPUT VOLTAGE, 3) NUMBER OF DRIVERS

Output Ratings *			Features						
mA	V	#	Serial Input	Latched Drivers	Diode Clamp	Saturated Outputs	Internal Protection	Mil Avail.	Part Number †
Sink Drivers									
14	-115	8	—	—	—	—	—	—	7180
100	20	8	—	—	—	X	—	—	2595
	30	32	X	X	—	—	—	—	5833
	40	8	—	—	—	X	—	—	2595-1
	40	32	X	X	—	X	—	—	5832
	50	8	X	X	—	X	—	—	5824
250	150	7	—	—	X	—	—	—	7003
300	60	2	Hall Sensor/Driver		—	X	—	—	Series 5275 ‡
	45	1	Hall Sensor/Driver		X	—	X	—	5140 ‡
	50	8	—	—	X	X	—	—	2596
	80	2	—	—	—	X	—	X	3611 thru 3614
	80	4	—	—	X	X	—	—	5703 and 5706
350	50	4	—	X	X	—	—	X	5800
	50	8	—	X	X	—	—	X	5801
	50	8	X	X	—	—	—	—	5821
	50	8	X	X	X	—	—	—	5841
	60	16	4 to 16-Line Latched Decoder/Driver			—	—	—	5816
	80	8	X	X	—	—	—	X	5822
	80	8	X	X	X	—	—	X	5842
	100	8	X	X	—	—	—	—	5823
	100	8	X	X	X	—	—	—	5843
500	70	2	—	—	X	X	—	—	5732
600	60	4	—	—	—	X	X	—	2547
	60	4	—	—	X	X	X	—	2549
	70	2	—	—	X	X	—	—	Series 5740
700	60	4	—	—	X	X	X	—	2543
750	50	8	—	—	X	X	—	—	2597
800	50	4	—	X	X	—	—	—	5830
	50	4	—	X	X	X	—	—	5831
1000	70	2	—	—	X	X	—	—	5725
1250	50	4	Stepper Motor Translator/Driver			—	X	—	5804
	50	2	—	—	X	—	—	—	2061
	50	4	—	—	X	—	—	X	2064, 2068, & 2074
1500	80	2	—	—	X	—	—	—	2062
	80	4	—	—	X	—	—	X	2065 and 2069

* Current is maximum specified test condition, voltage is maximum rating.
See specification for sustaining voltage limits or over-current protection voltage limits.

Continued next page...

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Hall effect or optoelectronic sensor. See Section 4.

PERIPHERAL POWER AND DISPLAY DRIVERS

Output Ratings *			Features						
mA	V	#	Serial Input	Latched Drivers	Diode Clamp	Saturated Outputs	Internal Protection	Mil Avail.	Part Number †
Sink Drivers (cont'd)									
1600	50	9	X	X	—	—	X	—	5829
1800	50	4	—	—	X	—	—	—	2544
	50	4	—	—	X	—	—	—	2540
4000	50	4	—	—	X	—	—	—	2878
	80	4	—	—	X	—	—	—	2879
Source Drivers									
-25	60	8	—	X	—	—	—	—	5815
	60	10	X	X	—	—	—	X	5810
	60	10	X	X	Active Pull-Down	—	—	—	5810-F
	60	12	X	X	—	—	—	—	5811
	60	20	X	X	Active Pull-Down	—	—	—	5812-F
	60	32	X	X	Active Pull-Down	—	—	—	5818-F
	65	6	—	—	—	—	—	—	6116-2
	65	8	—	—	—	—	—	—	6118-2
	80	8	—	X	—	—	—	—	5815-1
	80	10	X	X	—	—	—	—	5810-1
	80	10	X	X	Active Pull-Down	—	—	—	5810-F-1
	80	12	X	X	—	—	—	—	5811-1
	80	20	X	X	Active Pull-Down	—	—	—	5812-F-1
	80	32	X	X	Active Pull-Down	—	—	—	5818-F-1
	85	6	—	—	—	—	—	—	6116
	85	8	—	—	—	—	—	X	6118
	115	6	—	—	—	—	—	—	6116-1
	115	8	—	—	—	—	—	—	6118-1
-120	-25	8	—	—	X	X	—	—	2585
	30	8	—	—	X	X	—	—	2985
	50	8	X	X	X	X	—	—	5895
-350	35	8	—	—	X	—	X	—	2987
	50	8	X	X	X	—	—	—	5891
	-50	8	—	—	X	—	—	—	2580 and 2588
	-80	5	—	—	X	—	—	—	2957
	-80	8	—	—	X	—	—	—	2580-1 and 2588-1
	80	8	—	—	X	—	—	X	2981 thru 2984
	80	8	X	X	X	—	—	—	5890
-4000	60	4	—	—	X	—	—	—	2944

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits or over-current protection voltage limits.

Continued next page...

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Hall effect or optoelectronic sensor. See Section 4.

PERIPHERAL POWER AND DISPLAY DRIVERS

Output Ratings *			Features					Mil Avail.	Part Number †
mA	V	#	Serial Input	Latched Drivers	Diode Clamp	Saturated Outputs	Internal Protection		
Source/Sink Drivers									
±500	40	4	Dual Full Bridge		X	—	—	—	2993
±750	45	4	Dual PWM Bridge		X	X	X	—	2916
±800	16	2	Voice-Coil Motor Driver				X	—	8931 and 8958
±900	7.0	3	3-Ø Brushless Controller/Driver			DMOS	X	—	8901 and 8902
	14	3	3-Ø Brushless Controller/Driver			DMOS	X	—	8903
±1000	28	1	Power Op Amp		X	—	—	—	3751
	40	2	Dual Power Op Amp		X	—	—	—	3755
±1500	45	4	Dual PWM Full Bridge		X	—	X	—	2917
±2000	14	3	3-Ø Brushless Controller/Driver			DMOS	X	—	8922
	30	1	Half Bridge		X	—	X	—	2935 and 2950
	45	3	3-Ø Brushless Controller/Driver			—	X	X	2936 and 2936-120
	50	2	PWM Full Bridge		X	—	X	X	2953 and 2954
	50	4	Dual Full Bridge		X	—	X	X	2998
±3000	45	2	PWM Control		X	—	—	—	2962
	45	2	—	—	X	—	X	—	2974
±3400	45	1	PWM Control		X	—	X	—	2961
±4000	14	3	3-Ø Brushless Controller/Driver			DMOS	X	—	8925
±4800	65	2	PWM Control		X	—	X	—	2966
±6000	40	1	—	—	X	—	X	—	2955-2

* Current is maximum specified test condition, voltage is maximum rating.
See specification for sustaining voltage limits or over-current protection voltage limits.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Hall effect or optoelectronic sensor. See Section 4.

SELECTION GUIDE

HIGH-VOLTAGE PERIPHERAL POWER AND DISPLAY DRIVERS

IN ORDER OF 1) OUTPUT VOLTAGE, 1) OUTPUT CURRENT, 3) NUMBER OF DRIVERS

Output Ratings *			Features					Mil Avail.	Part Number †
V	mA	#	Serial Input	Latched Drivers	Diode Clamp	Saturated Outputs	Internal Protection		
100	350	8	X	X	—	—	—	—	5823
	350	8	X	X	X	—	—	—	5843
-115	14	8	—	—	—	—	—	—	7180
115	-25	6	—	—	—	—	—	—	6116-1
	-25	8	—	—	—	—	—	—	6118-1
150	250	7	—	—	X	—	—	—	7003

* Current is maximum test condition; voltage is absolute maximum allowable.
Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

SELECTION GUIDE

BiMOS SMART POWER INTERFACE DRIVERS

Sections 3 and 5

	Output Ratings *		Mil Avail.	Part Number †
Serial-Input Latched Drivers				
8-Bit (saturated drivers)	100 mA	50 V‡	—	5824
8-Bit (saturated drivers)	-120 mA	50 V‡	—	5895
8-Bit	350 mA	50 V	—	5821
8-Bit	350 mA	50 V‡	—	5841
8-Bit	-350 mA	50 V‡	—	5891
8-Bit	350 mA	80 V	X	5822
8-Bit	350 mA	80 V‡	—	5842
8-Bit	-350 mA	80 V‡	—	5890
8-Bit	350 mA	100 V	—	5823
8-Bit	350 mA	100 V‡	—	5843
9-Bit	1.6 A	50 V	—	5829
10-Bit	-25 mA	60 V	X	5810
10-Bit (active pull-downs)	-25 mA	60 V	—	5810-F
10-Bit	-25 mA	80 V	—	5810-1
10-Bit (active pull-downs)	-25 mA	80 V	—	5810-F-1
12-Bit	-25 mA	60 V	—	5811
12-Bit	-25 mA	80 V	—	5811-1
20-Bit (active pull-downs)	-25 mA	60 V	—	5812-F
20-Bit (active pull-downs)	-25 mA	80 V	—	5812-F-1
32-Bit (active pull-downs)	-25 mA	60 V	—	5818-F
32-Bit (active pull-downs)	-25 mA	80 V	—	5818-F-1
32-Bit	100 mA	30 V	—	5833
32-Bit	100 mA	40 V	—	5832
Parallel-Input Latched Drivers				
4-Bit	350 mA	50 V‡	X	5800
4-Bit	800 mA	50 V‡	—	5830
4-Bit (saturated drivers)	800 mA	50 V‡	—	5831
8-Bit	-25 mA	60 V	X	5815
8-Bit	-25 mA	80 V	—	5815-1
8-Bit	350 mA	50 V‡	X	5801
Special-Purpose Functions				
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	—	5804
Addressable Latched Hexadecimal Driver	350 mA	60 V‡	—	5816

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

SELECTION GUIDE

MOTOR DRIVERS

Sections 3, 4, and 5

Function	Output Ratings *		Part Number †	Detailed Info. Section
Integrated Circuits for Brushless DC Motors				
3-Phase Controller/Drivers	±2.0 A	45 V	2936 and 2936-120	3, 5
2-Phase Hall-Effect Sensor/Controller	20 mA	25 V	3235	4
Hall-Effect Latched Sensors	10 mA	24 V	3175 and 3177	4
Hall-Effect Latched Sensor	20 mA	25 V	3275	4
Hall-Effect Latched Sensor	300 mA	60 V	5275	4
2-Phase Driver	800 mA	50 V	5725	3
3-Phase Back-EMF Controller/Drivers	±900 mA	7 V	8901 and 8902	3
3-Phase Back-EMF Controller/Driver	±900 mA	14 V	8903	3
3-Phase Controller/DMOS Driver	±2.0 A	14 V	8922	3
3 Phase Controller/DMOS Driver	±4.0 A	14 V	8925	3
Full-Bridge Drivers for DC and Bipolar Stepper Motors				
PWM Current Controlled Dual Full Bridge	±750 mA	45 V	2916	3
PWM Current Controlled Dual Full Bridge	±1.5 A	45 V	2917	3
PWM Current Controlled Full Bridges	±2.0 A	50 V	2953 and 2954	3, 5
Dual Full Bridge	±500 mA	40 V	2993	3
Dual Full Bridge	±2.0 A	50 V	2998	3, 5
Other Motor Drivers				
Unipolar Stepper Motor Driver	1.8 A	50 V	2544	3
Linear Servo Motor Driver	±1.0 A	28 V	3751	3
Dual Linear Servo Motor Driver	±1.0 A	40 V	3755	3
Unipolar Stepper-Motor Translator/Driver	1.25 A	50 V	5804	3
Voice-Coil Motor Drivers	±800 mA	16 V	8931 and 8958	3

* Current is maximum specified test condition, voltage is maximum rating.
See specification for sustaining voltage limits or over-current protection voltage limits.
Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

SELECTION GUIDE

HALL-EFFECT AND OPTOELECTRONIC SENSORS

Switch Points (at T_A = +25°C) Max. Operate	Min. Release	Max. Output Ratings	Part Number *	Ext. Temp. Available
Unipolar Hall-Effect Switches				
175 G	25 G	2 x 25 mA†/25 V	3235	—
200 G	50 G	25 mA/25 V	3140	yes
200 G	50 G	900 mA/28 V	5140	—
300 G	-25 G	24 V‡	3055	yes
350 G	50 G	25 mA/25 V	3120	yes
450 G	30 G	25 mA/25 V	3113	—
500 G	125 G	25 mA/25 V	3119	yes
Gear-Tooth Sensor		25 mA/24 V	3059	yes
Vane Switch		25 mA/25 V	6450	—

* Complete part number includes additional characters to indicate operating temperature range and package style.

† Output 1 switches on south pole, output 2 switches on north pole.

‡ Multiplexed two-wire sensor; after proper address, power/signal bus current indicates magnetic field condition.

Switch Points (at T_A = +25°C) Max. Operate	Min. Release	Max. Output Ratings	Part Number *	Ext. Temp. Available
Bipolar Hall-Effect Switches				
+75 G	-75 G	25 mA/25 V	3133	yes
+95 G	-95 G	25 mA/25 V	3132	yes
+150 G	-150 G	25 mA/25 V	3130	yes

Switch Points (at T_A = +25°C) Min. Operate	Max. Operate	Max. Output Ratings	Part Number *	Ext. Temp. Available
Bipolar Hall-Effect Latches				
±50 G	±150 G	15 mA/24 V	3177	—
±25 G	±170 G	15 mA/24 V	3175	—
±25 G	±250 G	2 x 50 mA/25 V†	3275	—
±25 G	±250 G	2 x 500 mA/30 V†	5275	—

* Complete part number includes additional characters to indicate operating temperature range and package style.

† Complementary outputs for 2-phase unipolar brushless dc motor control.

HALL-EFFECT AND OPTOELECTRONIC SENSORS

Description	Part Number *	Ext. Temp. Available
Linear Hall-Effect Sensors		
Typical output 0.7 mV/gauss	3501	—
Typical output 1.3 mV/gauss	3503	yes

Description	Part Number *
Optoelectronic Switches	
Twilight sensor, ON below 10 µW/cm2 typ.	3390
Open collector, ON below 55 µW/cm2 typ.	3330
Internal pull-up, ON below 55 µW/cm2 typ.	3360
Open collector, OFF below 55 µW/cm2 typ.	3363
Linear Optoelectronic Sensors	
Minimum output 280 nA/µW/cm2	3311
Minimum output 350 nA/µW/cm2	3312

* Complete part number includes additional characters to indicate operating temperature range and package style.

See also, 2429 fluid detector and 5348 smoke detector, Section 6.

SELECTION GUIDE

MILITARY POWER AND SMART POWER DRIVERS

Part Number	Description*
SMDP Devices	
5962-3814103BEC	See ULS2003H
5962-3814106BVC	See ULS2801H
5962-3814107BVC	See ULS2802H
5962-3814108BVC	See ULS2803H
5962-3814109BVC	See ULS2804H
5962-3814110BVC	See ULS2805H
5962-8605801MVC	See ULS2803H
5962-8605801M2C	See ULS2803EK
5962-8753201MEC	See ULS2069H
5962-8753202MEC	See ULS2070H
5962-8764001MWC	See UCS5801H
5962-8764101MWC	See UCS5822H
5962-8851901MVC	See UDS2981H
5962-8968401MVC/A	See ULS2821H/R
5962-8968401M2C	See ULS2821EK
5962-8968501MVC/A	See ULS2823H/R
5962-8968501M2C	See ULS2823EK
5962-8968601MVC/A	See ULS2824H/R
5962-8968601M2C	See ULS2824EK
MIL-STD-883 Compliant Devices †	
2001 thru 2005	7-Channel 50 V/350 mA Darlington Arrays
2011 thru 2015	7-Channel 50 V/500 mA Darlington Arrays
2021 thru 2025	7-Channel 95 V/350 mA Darlington Arrays
2064 thru 2077	Quad 1.25 A Darlington Switches
2801 thru 2805	8-Channel 50 V/350 mA Darlington Arrays
2811 thru 2815	8-Channel 50 V/500 mA Darlington Arrays
2821 thru 2825	8-Channel 95 V/350 mA Darlington Arrays
2936	3-Phase 45 V/±2 A Brushless DC Motor Controller/Driver
2953	Full-Bridge 50 V/±2 A PWM Motor Driver
2981 thru 2984	8-Channel 50 V or 80 V/-350 mA Source Drivers
2998	Dual 50 V/±1.8 A Full-Bridge Motor Driver
3119 thru 3140	Hall Effect Switches ‡
3611 thru 3614	Dual 80 V/300 mA Peripheral/Power Drivers §
5800	4-Bit 50 V/350 mA Latched Driver
5801	8-Bit 50 V/350 mA Latched Driver
5810	10-Bit Serial-In, 60 V/-25 mA Latched Source Driver
5815	8-Channel, 60 V/-25 mA Latched Source Driver
5822	8-Bit Serial-In, 80 V/350 mA Latched Driver
6118	8-Channel 85 V/-25 mA VF Display Driver

* Current is maximum specified test condition, voltage is maximum rating.
See specification for sustaining voltage limits or over-current protection voltage limits.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ NON-COMPLIANT because of differences in moisture resistance test method.

§ NON-COMPLIANT because of package dimensions.

SELECTION GUIDE

AUTOMOTIVE, SIGNAL-PROCESSING, AND CONSUMER ICs

Part Number *	Inputs	Function	Supply Voltage Range
Linear Integrated Circuits for Radio Applications (Detailed Information in Section 6)			
3827	Composite Audio	FM Stereo Decoder w/Noise Actuated Blend	7.5-12 V
3845	to 30 MHz	AM Stereo Noise Blanker	7.5-12 V
3846	to 30 MHz	AM Noise Blanker	7.5-12 V
3847	to 20 MHz	Dual-Conversion AM Receiver	6.5-16 V

* Complete part number includes additional characters to indicate operating temperature range and package style.

Part Number*	Function	Detailed Info Section
Specialized Integrated Circuits for Automotive Applications		
2429	Low-Coolant Detector	6
2436 and 2437	Rear-Window Defogger Timers	6
2453 and 2454	Dual Automotive Lamp Monitors	6
2455	Quad Automotive Lamp Monitor	6
2460	Electronic Spark Timing	6
3059	Hall Effect Gear-Tooth Sensor	4
3360 and 3390	Twilight Sensors	4
5233 thru 5604	Vacuum Fluorescent Automotive Clocks	6
5615 and 5616	LCD Automotive Clocks	6
Specialized Integrated Circuits for Consumer Applications		
2429	Fluid Detector	6
2436 and 2437	Countdown Power Timers	6
2455	Quad Comparator	6
3059	Hall Effect Gear-Tooth Sensor	4
3360	Twilight Sensor	4
5348	Ionization-Type Smoke Detector	6
6450	Hall Effect Vane Switch	4
8931 and 8958	Brushless DC Motor Drivers	3
Other Analog Integrated Circuits		
3311 and 3312	Precision Light Sensors	4
3501 and 3503	Linear Output Hall Effect Sensors	4
3751	Power Operational Amplifier	3
3755	Dual Power Operational Amplifier	3
8931 and 8958	Voice-Coil Motor Drivers	3

* Complete part number includes additional characters to indicate operating temperature range and package style.

CROSS REFERENCE

IN ALPHA-NUMERICAL ORDER

The suggested replacement devices are based on similarity as shown in currently published data. Exact replacement in all applications is not guaranteed and the user should compare the specifications of the competitive and recommended replacement.

MFG CODES:

AMI	American Microsystems
ASAHI	Asahi
CS	Cherry Semiconductor
DI	Dionics, Inc.
EXR	Exar Integrated Systems
FSC	Fairchild Semiconductor
HIT	Hitachi Ltd.
IP	Integrated Power
MAT	Matsushita
MICR	Microswitch
MIT	Mitsubishi Electric Corp.
MOT	Motorola Semiconductor
MT	Mietec
NS	National Semiconductor
OKI	Oki Semiconductor
PE	Pro-Electron ‡
QPL	Qualified (QPL) to MIL-M-38510
RCA	RCA (Harris)
RFA	Rifa
SAM	Samsung Semiconductor
SG	Silicon General Inc.
SIEM	Siemens Corp.
SIG	Signetics Corp.
SGS	SGS/ATES
SMDP	Standard Military Drawing Program †
SPR	Sprague Semiconductor Group
SYL	Sylvania
THM	Thomson-CSF
TI	Texas Instruments
TOS	Toshiba Corp.
TRW	TRW
UNI	Unitrode

‡ European registration; manufactured by various companies including ITT, Philips, SGS/ATES, Siemens, Thomson-CSF, AEG-Telefunken, Valvo, & others.

† Ordering part number is SMDP Drawing number as listed. Commercial part number is shown for reference only.

* Functional equivalent only; usually improved performance but not necessarily pin compatible.

CROSS REFERENCE
CA-NE

Competitive Part Number						Competitive Part Number					
Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes	Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes
CA	3219	AE	RCA	UDN2543B		L	293		SGS	UDN2993B	*
CA	3219	E	RCA	UDQ2543B		L	293	D	SGS/UNI	UDN2993B	*
CA	3242	E	RCA	UDN2543B		L	295		SGS/UNI	UDN2962W	*
CA	3262	E	RCA	UDN2543B		L	298		SGS/UNI	UDN2998W	*
CS	166		CS	ULN2429A		L	298	D	SGS	UDN2998W	*
DI	300		DI	UDN7180A		L	298	DNE	TI	UDN2993B	*
DI	507		DI	UDN6116A-1	*	L	6220		SGS	UDN2544B	
DI	508		DI	UDN6116A	*	L	6221		SGS	UDN2540B	
DI	509		DI	UDN6116A-2	*	M	2064	P	MIT	ULN2064B	*
DI	509	BR	DI	UDQ6116A-2	*	M	2065	P	MIT	ULN2065B	
DI	514		DI	UDN6118A-2	*	M	2580	P	MIT	UDN2580A	
DN	6835		NS/MAT	UGN3501U		M	2580	P-I	MIT	UDN2580A-1	
DN	6836		NS/MAT	UGN3501U		M	2981	P	MIT	UDN2981A	
DN	6837		NS/MAT	UGN3119U		M	2982	P	MIT	UDN2982A	
DN	6838		NS/MAT	UGN3130U		M	2983	P	MIT	UDN2983A	
DN	6839		NS/MAT	UGN3119U		M	2984	P	MIT	UDN2984A	
ECG	2021		SYL	UDN6118A		M	38510/14103	BEC	QPL	ULS2003H883	
ECG	2026		SYL	UDN6116A-1		M	38510/14106	BVC	QPL	ULS2801H883	
EW	500		ASAHI	UGN3175U		M	38510/14107	BVC	QPL	ULS2802H883	
EW	550		ASAHI	UGN3140U		M	38510/14108	BVC	QPL	ULS2803H883	
FPQ	2222		FSC	TPQ2222		M	38510/14109	BVC	QPL	ULS2804H883	
FPQ	2907		FSC	TPQ2907		M	38510/14110	BVC	QPL	ULS2805H883	
FSA	2619	P	FSC	TND908		M	54532	P	MIT	ULN2064B	*
FSA	2719	P	FSC	TND903		M	54562	P	MIT	UDN2982A	
HA	13007		HIT	UDN2540B		M	54563	P	MIT	UDN2981A	
HA	13415		HIT	UDN2543B		MC	3479	P	MOT	UCN5804B	*
HA	13421	A	HIT	UDN2993B	*	MPQ	2222		MOT	TPQ2222	
HA	16617	P	HIT	UDN6118A-2		MPQ	2369		MOT	TPQ2369	
HA	16617	PJ	HIT	UDQ6118A-2		MPQ	2484		MOT	TPQ2484	
IP	293	D	IP	UDN2993B	*	MPQ	2907		MOT	TPQ2907	
IP	2064	N	IP	ULN2064B		MPQ	3799		MOT	TPQ3799	
IP	2065	N	IP	ULN2065B		MPQ	3904		MOT	TPQ3904	
IP	2068	N	IP	ULN2068B		MPQ	3906		MOT	TPQ3906	
IP	2069	N	IP	ULN2069B		MPQ	6002		MOT	TPQ6002	
IP	2074	N	IP	ULN2074B		MPQ	6502		MOT	TPQ6502	
JAN	2003	J	SG	ULS2003R		MPQ	6700		MOT	TPQ6700	
KA	2580	A	SAM	UDN2580A		MSL	912	R	OKI	UDN6118A-2	
KA	2588	A	SAM	UDN2588A		MTC	6020		MT	UCN5801A	
L	165		SGS	ULN3751Z		NE	594	N	SIG	UDN6118A-2	
L	272		SGS	ULN3755B	*	NE	594	F	SIG	UDN6118R-2	

* Functional equivalent only; usually improved performance but not necessarily pin compatible.

CROSS REFERENCE
OH-TL

Competitive Part Number						Competitive Part Number					
Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes	Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes
OH	360		TRW	UGN3120-		SN	65518	FN	TI	UCQ5818EPF	
OHN	3013	U	TRW	UGN3113U		SN	65518	N	TI	UCQ5818AF	
OHN	3019	U	TRW	UGN3119U		SN	75064	NE	TI	ULN2064B	
OHN	3020	U	TRW	UGN3120U		SN	75065	NE	TI	ULN2065B	
OHN	3030	U	TRW	UGN3130U		SN	75068	NE	TI	ULN2068B	
OHN	3040	U	TRW	UGN3140U		SN	75069	NE	TI	ULN2069B	
OHS	3019	U	TRW	UGS3119U		SN	75074	NE	TI	ULN2074B	
OHS	3020	U	TRW	UGS3120U		SN	75407	P	TI	UDN5752M	
OHS	3030	U	TRW	UGS3130U		SN	75437	ANE	TI	UDN2543B	
OHS	3040	U	TRW	UGS3140U							
						SN	75512	BN	TI	UCN5811A	
PBD	3517		RFA	UCN5804B	*	SN	75518	FN	TI	UCN5818EPF	
PBL	3717		RFA	UDN2953B	*	SN	75518	N	TI	UCN5818AF	
PBL	3770		RFA	UDN2953B	*	SN	75605	K	TI	UDN2950Z	
Q2T	2222		TI	TPQ2222		SN	754410		TI	UDN2993B	*
S	4534		AMI	UCN5810A		SN	754411		TI	UDN2993B	*
S	4535		AMI	UCN5818AF		SS	31	EA	MICR	UGS3131-	
SA	594	F	SIG	UDQ6118R-2		SS	41		MICR	UGS3131UA	
SA	594	N	SIG	UDQ6118A-2		SS	46		MICR	UGN3130UA	
SAA	1027		SIG/PE	UCN5804B	*	SS	81	CA	MICR	UGS3131-	
SAA	1042		MOT/PE	UCN5804B	*	SS	81	EA	MICR	UGN3131-	
SAS	251	S5	SIEM	UGN3119-		TA	7272	P	TOS	ULN3755W	*
SG	298	D	SG	UDN2998W	*	TCA	365		PE/SIEM	ULN3751Z	*
SG	2001	J	SG	ULS2001R883		TD	62064	AP	TOS	ULN2064B	
SG	2002	J	SG	ULS2002R883		TD	62064	P	TOS	ULN2064B	
SG	2003	J	SG	ULS2003R883		TD	62074	AP	TOS	ULN2074B	
SG	2004	J	SG	ULS2004R883		TD	62074	P	TOS	ULN2074B	
SG	2064	W	SG	ULN2064B		TD	62781	AP	TOS	UDN6118A-2	
SG	2065	W	SG	ULN2065B		TDA	3717		PE	UDN2953B	*
SG	2068	W	SG	ULN2068B		TEA	3717		PE	UDN2953B	*
SG	2069	W	SG	ULN2069B		TID	121		TI	TND933	
SG	2074	W	SG	ULN2074B		TID	122		TI	TND940	
SG	3173	P	SG	ULN3751Z		TID	123		TI	TND938	
SG	3635	P	SG	UDN2935Z		TID	124		TI	TND939	
SG	3643	S	SG	UDN2962W	*	TL	170		TI	UGN3130U	*
SG	3851	J	SG	ULS2011R883		TL	172	C	TI	UGN3119U	*
SG	3852	J	SG	ULS2012R883		TL	173	C	TI	UGN3503U	*
SG	3853	J	SG	ULS2013R883		TL	173	I	TI	UGN3503U	*
SG	3854	J	SG	ULS2014R883		TL	4810	BDW	TI	UCN5810LWF	
SG	6118	N	SG	UDN6118A		TL	4810	BIDW	TI	UCQ5810LWF	
SN	65512	BN	TI	UCQ5811A		TL	4810	BIN	TI	UCQ5810AF	

* Functional equivalent only; usually improved performance but not necessarily pin compatible.

CROSS REFERENCE
TL-ULN

Competitive Part Number						Competitive Part Number					
Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes	Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes
TL	4810	BN	TI	UCN5810AF		UDN	6184	A	SPR	UDN6118A-1	
TL	5812	FN	TI	UCN5812EPF		UGN	3013	—	SPR	UGN3113-	
TL	5812	N	TI	UCN5812AF		UGN	3019	—	SPR	UGN3119-	
TL	5812	FN	TI	UCN5812EPF		UGN	3020	—	SPR	UGN3120-	
TL	5812	IFN	TI	UCQ5812EPF		UGN	3030	—	SPR	UGN3130-	
TL	5812	IN	TI	UCQ5812AF		UGN	3040	—	SPR	UGN3140-	
µA	9667	DMBQ	FSC	ULS2003R883		UGN	3075	—	SPR	UGN3175-	
UC	2950	T	UNI	UDN2950Z		UGN	3077	—	SPR	UGN3177-	
UC	3175		UNI	A8958SEA		UGN	3131	—	SPR	UGN3132-	
UC	3517		UNI	UCN5804B	*	UGN	3501	M	SPR	UGN3501LI	*
UC	3620		UNI	UDN2936W	*	UGS	3019	—	SPR	UGS3119-	
UC	3717	A	UNI	UDN2953B	*	UGS	3020	—	SPR	UGS3120-	
UC	3770		UNI	UDN2954W	*	UGS	3030	—	SPR	UGS3130-	
UCN	4202	A	SPR	UCN5804B	*	UGS	3040	—	SPR	UGS3140-	
UCN	4203	A	SPR	UCN5804B	*	UGS	3131	—	SPR	UGS3132-	
UCN	4205	B-2	SPR	UCN5804B		UHP	181		SPR	UDN5706A	*
UCN	4401	A	SPR	UCN5800A		UHP	400		SPR	UDN5706A	*
UCN	4801	A	SPR	UCN5801A		UHP	400	-1	SPR	UDN5706A	*
UCN	4801	ADP	THM	UCN5801A		UHP	402		SPR	UDN5703A	*
UCN	4810	A	SPR	UCN5810A		UHP	402	-1	SPR	UDN5703A	*
UCN	4810	N	TI	UCN5810A		UHP	406		SPR	UDN5706A	*
UCN	4815	A	SPR	UCN5815A		UHP	406	-1	SPR	UDN5706A	*
UCN	4821	A	SPR	UCN5821A		ULN	2064	B	MOT/SGS	ULN2064B	
UCN	4822	A	SPR	UCN5822A		ULN	2064	N	IP	ULN2064B	
UCN	4823	A	SPR	UCN5823A		ULN	2064	NE	MOT/TI	ULN2064B	
UCN	5812	A	SPR	UCN5812AF		ULN	2065	B	MOT/SGS	ULN2065B	
UCN	5812	AF-1	SPR	UCN5812AF-1		ULN	2065	N	IP	ULN2065B	
UCN	5812	EP	SPR	UCN5812EPF		ULN	2065	NE	MOT/TI	ULN2065B	
UCN	5812	EP-1	SPR	UCN5812EPF-1		ULN	2068	B	MOT/SGS	ULN2068B	
UD	4181		SPR	UDN5706A	*	ULN	2068	N	IP	ULN2068B	
UDN	2541	B	SPR	UDN2543B	*	ULN	2068	NE	MOT/TI	ULN2068B	
UDN	2542	B	SPR	UDN2543B	*	ULN	2069	B	MOT/SGS	ULN2069B	
UDN	2949	Z	SPR	UDN2950Z		ULN	2069	N	IP	ULN2069B	
UDN	2952	B	SPR	UDN2953B	*	ULN	2069	NE	MOT/TI	ULN2069B	
UDN	2952	W	SPR	UDN2954W	*	ULN	2074	B	MOT/SGS	ULN2074B	
UDN	2956	A	SPR	UDN2957A	*	ULN	2074	N	IP	ULN2074B	
UDN	2975	W	SPR	UDN2962W	*	ULN	2074	NE	MOT/TI	ULN2074B	
UDN	5732	M	SPR	UDN5752M		ULN	2401	A	SPR	ULN2455A	*
UDN	6126	A	SPR	UDN6116A		ULN	3006	T	SPR	UGN3119U	
UDN	6164	A	SPR	UDN6116A-1		ULN	3008	T	SPR	UGN3501U	

* Functional equivalent only; usually improved performance but not necessarily pin compatible.

CROSS REFERENCE
ULN-XR

Competitive Part Number						Competitive Part Number					
Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes	Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes
ULN	3310	T	SPR	ULN3312T		ULS	2805	L	IP	ULS2805H883	
ULS	2001	J	IP	ULS2001R883		ULS	2811	J	IP	ULS2811R883	
ULS	2001	L	IP	ULS2001H883		ULS	2811	L	IP	ULS2811H883	
ULS	2002	J	IP	ULS2002R883		ULS	2812	J	IP	ULS2812R883	
ULS	2002	L	IP	ULS2002H883		ULS	2812	L	IP	ULS2812H883	
ULS	2003	J	IP	ULS2003R883		ULS	2813	J	IP	ULS2813R883	
ULS	2003	L	IP	ULS2003H883		ULS	2813	L	IP	ULS2813H883	
ULS	2004	J	IP	ULS2004R883		ULS	2814	J	IP	ULS2814R883	
ULS	2004	L	IP	ULS2004H883		ULS	2814	L	IP	ULS2814H883	
ULS	2005	J	IP	ULS2005R883		ULS	2815	J	IP	ULS2815R883	
ULS	2005	L	IP	ULS2005H883		ULS	2815	L	IP	ULS2815H883	
ULS	2011	J	IP	ULS2011R883		ULS	2821	J	IP	ULS2821R883	
ULS	2011	L	IP	ULS2011H883		ULS	2821	L	IP	ULS2821H883	
ULS	2012	J	IP	ULS2012R883		ULS	2822	J	IP	ULS2822R883	
ULS	2012	L	IP	ULS2012H883		ULS	2822	L	IP	ULS2822H883	
ULS	2013	J	IP	ULS2013R883		ULS	2823	J	IP	ULS2823R883	
ULS	2013	L	IP	ULS2013H883		ULS	2823	L	IP	ULS2823H883	
ULS	2014	J	IP	ULS2014R883		ULS	2824	J	IP	ULS2824R883	
ULS	2014	L	IP	ULS2014H883		ULS	2824	L	IP	ULS2824H883	
ULS	2015	J	IP	ULS2015R883		ULS	2825	J	IP	ULS2825R883	
ULS	2015	L	IP	ULS2015H883		ULS	2825	L	IP	ULS2825H883	
ULS	2021	J	IP	ULS2021R883		ULS	3006	T	SPR	UGS3119U	
ULS	2021	L	IP	ULS2021H883		US	7438	A	SPR	UDN5706A	*
ULS	2022	J	IP	ULS2022R883		XR	6116	P-2	EXR	UDQ6116A-2	
ULS	2022	L	IP	ULS2022H883		XR	6118	P	EXR	UDN6118A	
ULS	2023	J	IP	ULS2023R883		XR	6118	P-2	EXR	UDN6118A-2	
ULS	2023	L	IP	ULS2023H883			6	SS	MICR	UGN3501-	*
ULS	2024	J	IP	ULS2024R883			8	SS1	MICR	UGS3130-	*
ULS	2024	L	IP	ULS2024H883			8	SS1E1	MICR	UGN3130-	*
ULS	2025	J	IP	ULS2025R883			8	SS3	MICR	UGS3119-	*
ULS	2025	L	IP	ULS2025H883			8	SS3E1	MICR	UGN3113-	*
ULS	2801	J	IP	ULS2801R883			8	SS5	MICR	UGS3130-	*
ULS	2801	L	IP	ULS2801H883			8	SS5E1	MICR	UGN3130-	*
ULS	2802	J	IP	ULS2802R883			8	SS7	MICR	UGN3119-	*
ULS	2802	L	IP	ULS2802H883			8	SS7E1	MICR	UGN3119-	*
ULS	2803	J	IP	ULS2802R883			55	SS16	MICR	UGN3113-	*
ULS	2803	L	IP	ULS2803H883			65	SS2	MICR	UGN3113-	*
ULS	2804	J	IP	ULS2804R883			91	SS12-2	MICR	UGN3501-	*
ULS	2804	L	IP	ULS2804H883			92	SS12-2	MICR	UGN3501-	*
ULS	2805	J	IP	ULS2805R883			103	SR	MICR	UGN3501-	*

* Functional equivalent only; usually improved performance but not necessarily pin compatible.

CROSS REFERENCE

Competitive Part Number					
Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes
	103	SR5A-1	MICR	UGN3113-	*
	103	SR13A-1	MICR	UGS3119-	*
	103	SR17A-1	MICR	UGS3130-	*
	513	SS16	MICR	UGS3120-	*
	517	SS16	MICR	UGS3131-	*
	613	SS2	MICR	UGN3119-	*
	617	SS2	MICR	UGS3130-	*
	5962-3814103	BEC	QPL	ULS2003H883	
	5962-3814106	BVC	QPL	ULS2801H883	
	5962-3814107	BVC	QPL	ULS2802H883	
	5962-3814108	BVC	QPL	ULS2803H883	
	5962-3814109	BVC	QPL	ULS2804H883	
	5962-3814110	BVC	QPL	ULS2805H883	
	5962-8605801	MVC	SMDP	ULS2803H883	†
	5962-8605801	M2C	SMDP	ULS2803EK883	†
	5962-8605801	VC	SMDP	ULS2803H883	†
	5962-8605801	2C	SMDP	ULS2803EK883	†
	5962-8753201	EC	SMDP	ULS2069H883	†
	5962-8753201	MEC	SMDP	ULS2069H883	†
	5962-8753202	MEC	SMDP	ULS2070H883	†
	5962-8764001	MWC	SMDP	UCS5801H883	†
	5962-8764001	WC	SMDP	UCS5801H883	†
	5962-8764101	MWC	SMDP	UCS5822H883	†
	5962-8764101	WC	SMDP	UCS5822H883	†
	5962-8851901	MVC	SMDP	UDS2981H883	†

Competitive Part Number					
Prefix	Base Number	Suffix	Mfg. Code(s)	Suggested Replacement	Notes
	5962-8968401	MV-	SMDP	ULS2821H/R883	†
	5962-8968401	M2-	SMDP	ULS2821EK883	†
	5962-8968401	V-	SMDP	ULS2821H/R883	†
	5962-8968401	2-	SMDP	ULS2821EK883	†
	5962-8968501	MV-	SMDP	ULS2823H/R883	†
	5962-8968501	M2-	SMDP	ULS2823EK883	†
	5962-8968501	V-	SMDP	ULS2823H/R883	†
	5962-8968501	2-	SMDP	ULS2823EK883	†
	5962-8968601	MV-	SMDP	ULS2824H/R883	†
	5962-8968601	M2-	SMDP	ULS2824EK883	†
	5962-8968601	V-	SMDP	ULS2824H/R883	†
	5962-8968601	2-	SMDP	ULS2824EK883	†
	9665	DM	FSC	ULS2001R883	
	9666	DM	FSC	ULS2002R883	
	9667	DMQB	FSC	ULS2003R883	
	9668	DM	FSC	ULS2004R883	

* Functional equivalent only; usually improved performance but not necessarily pin compatible.

† Ordering part number is DESC Drawing number, or SMDP Drawing number as listed. Commercial part number is shown for reference only.

COMPETITIVE IC PART NUMBERING

Cherry Semiconductor:

CS 123 D

Package.
D = Small Outline
DW = Wide-Body Small Outline
FN = Plastic Leaded Chip Carrier
J = Ceramic DIP
N = Plastic DIP
V = Power Tab SIP
VH = Power Tab SIP with Lead Form

Exar:

XR 2001 C N

Package.
D = Small Outline
N = CerDIP
P = Plastic DIP

Grade.
C = Commercial (0°C to +70°C)
M = Military (-55°C to +125°C)
Blank = Improved Commercial

Fairchild:

µA 705 P C

Temperature.
C = Commercial (0°C to +70 or +75°C)
L = -55°C to +85°C
M = Military (-55°C to +125°C)

Package.
D = Ceramic DIP
J = Flange Mount (TO-66)
K = Flange Mount (TO-3)
P = Plastic DIP
R = Ceramic Mini-DIP
T = Plastic Mini-DIP
U = Power Tab (TO-220)

Fujitsu:

MB 3759 E C

Package.
C = Ceramic
P = Plastic DIP
Z = CerDIP

Hitachi:

HA 1199 P

Package.
P = Plastic DIP
C = Ceramic DIP
CG = Ceramic Leadless Chip Carrier
CP = Plastic Leaded Chip Carrier
G = CerDIP
SO = Small Outline

Integrated Power:

IP 3 P 45 T

Package.
D = Ceramic
J = CerDIP
K = Flange Mount (TO-3)
N = Plastic DIP
T = Power Tab (TO-220)

Temperature.
1 = -55°C to +125°C
2 = -25°C to +85°C
3 = 0°C to +70°C

COMPETITIVE IC PART NUMBERING

Mitsubishi:

M 5 4523 P

Package. K = CerDIP
P = Plastic DIP
S = Ceramic DIP

Temperature. 5 = Commercial/Industrial
9 = Military

Motorola:

MC 1311 P

Package. D = Small Outline
K = Metal Flange Mount (TO-3)
L = Ceramic DIP
P = Plastic DIP
PQ = Plastic Quad In-Line
R = Metal Flange Mount (TO-66)
T = Power Tab (TO-220)
U = Ceramic DIP

National Semiconductor:

LM 380 N

Package. D = Ceramic DIP
E = Ceramic Leadless Chip Carrier
J = CerDIP
M = Small Outline
N = Plastic DIP
T = Power Tab (TO-220)
V = Plastic Leaded Chip Carrier
WM = Wide-Body Small Outline

Pro-Electron:

TD A 1060 P P

Material. C = Metal-Ceramic
G = Glass-Ceramic (CerDIP)
M= Metal
P = Plastic

Package. D = Dual In Line
G = Flat Quad
K = Diamond

Temperature. A = See Detail Specification
B = 0°C to +70°C
C = -55°C to +125°C
D = -25°C to +70°C
E = -25°C to +85°C
F = -40°C to +85°C
G = -55°C to +85°C

RCA (Harris):

CA 758 E

Package. D = Ceramic DIP
E = Plastic DIP
F = CerDIP
M = Small Outline
Q = Plastic Leaded Chip Carrier
W = Staggered Quad In-Line Plastic
Blank = See Detail Specification

COMPETITIVE IC PART NUMBERING

SGS-Thomson:

L 292 C V

Package.
M = Mini-DIP
N = DIP
T = Flange Mount
V = Power Tab SIP (TO-220)
VH = Power Tab SIP with Lead Form

Special.
C = Commercial Temperature
D = Internal Diodes

Signetics:

NE 564 N

Package.
A = Plastic Leaded Chip Carrier
D = Small Outline
F = CerDIP
FE = Mini-CerDIP
G = Leadless Chip Carrier
I = Ceramic DIP
N = Plastic DIP
U = Plastic SIP

Temperature.
N or NE = 0°C to +70°C
SA = -40°C to +85°C
S or SE = -55°C to +125°C
SU = -25°C to +85°C

Silicon General:

SG 1524 F

Package.
D = Small Outline
DM = 8-Lead Small Outline
DW = Wide-Body Small Outline
G = Power Tab (TO-220)
H = Ceramic DIP
J = CerDIP
L = Leadless Ceramic Chip Carrier
M = Plastic Mini-DIP
N = Plastic DIP
P = Power Tab (TO-220)
W = Plastic DIP Semi-Tab
Y = Ceramic Mini-DIP

COMPETITIVE IC PART NUMBERING

Texas Instruments:

SN 75 064 NE

Package.
D = Small Outline
DW = Wide-Body Small Outline
FG = Ceramic Rectangular Leadless Chip Carrier
FH = Ceramic Square Leadless Chip Carrier
FK = Ceramic Square Leadless Chip Carrier
FM = Plastic Rectangular Leaded Chip Carrier
FN = Plastic Square Leaded Chip Carrier
J = CerDIP
JD = Ceramic DIP
K = Power Tab (TO-220)
N = Plastic DIP
ND = Plastic DIP Semi-Tab
NE = Plastic DIP Semi-Tab
P = Plastic Mini-DIP

Temperature. 55 = -55°C to +125°C
75 = 0°C to +70°C

TL 494 C J

Package. As shown above.

Temperature.
C = Commercial (0°C to +70°C)
E = Extended (-40°C to +85°C)
I = Industrial (-25°C to +85°C)
M = Military (-55°C to +125°C)

Toshiba:

TA 7272 P

Package.
C = Ceramic
D = CerDIP
J = Plastic SOJ
P = Plastic DIP
T = PLCC

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PRODUCT SELECTION GUIDES 2

PERIPHERAL POWER & DISPLAY DRIVER ICs 3

HALL-EFFECT & OPTOELECTRONIC SENSOR ICs 4

INTEGRATED CIRCUITS to MIL-STD-883 5

AUTOMOTIVE, SIGNAL-PROCESSING, & CONSUMER ICs 6

DISCRETE TRANSISTORS, DIODES, & ARRAYS 7

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SECTION 3. TECHNICAL DATA & APPLICATION NOTES FOR PERIPHERAL POWER AND DISPLAY DRIVER ICS

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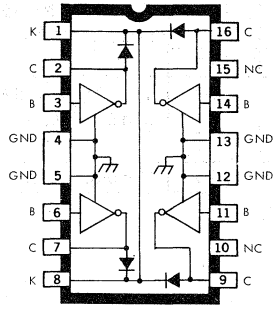
2061 THRU 2074

1.5 A DARLINGTON SWITCHES

ULN2064/65B



Dwg. No. A-9765A

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for Any One Driver (unless otherwise noted)

Output Voltage, V_{CEX} . . . . . **See Guide**
Output Sustaining Voltage, $V_{CE(SUS)}$ . . . . . **See Guide**
Output Current, I_{OUT} (Note 1) . . . . . **1.75 A**
Input Voltage, V_{IN} (Note 2) . . . . . **See Guide**
Input Current, I_B (Note 3) . . . . . **25 mA**
Supply Voltage, V_S (ULN2068B/LB & 2069B) . . . . . **10 V**
Total Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to -150°C**

1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.
2. Input voltage is referenced to the substrate (no connection to other pins) for the ULN2061/62M and ULN2074B, reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

High-voltage, high-current Darlington arrays ULN2061M through ULN2074B are designed for interface between low-level logic and a variety of peripheral loads such as relays, solenoids, dc and stepper motors, magnetic print hammers, multiplexed LED and incandescent displays, heaters, and similar loads. Output OFF voltage ratings of 50 V and 80 V are available. In the DIP, the quad drivers can drive resistive loads to 480 watts (1.5 A x 80 V, 26% duty cycle). For inductive loads, sustaining voltages of 35 V and 50 V at 100 mA are specified.

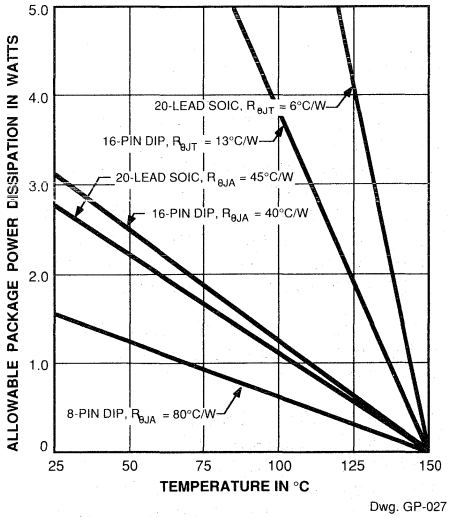
Dual-driver arrays ULN2061M and the higher-voltage ULN2062M are used for common-emitter (externally connected) or emitter-follower applications. They are supplied in 8-pin plastic mini-DIPs.

Quad drivers ULN2064B/LB, ULN2065B, ULN2068B/LB, and ULN2069B are intended for use with TTL, low-speed TTL, and 5 V MOS logic. The ULN2065B and ULN2069B are selected for the 80 V minimum output breakdown specification. The ULN2068B/LB and ULN2069B have pre-driver stages and are recommended for applications requiring high gain (low input-current loading). Isolated Darlington array ULN2074B is identical to the ULN2064B except for the isolated Darlington pinout and the deletion of suppression diodes. This switch is for emitter-follower applications. Quad-driver arrays are supplied with heat-sink contact tabs in 16-pin plastic DIPs (suffix B) and 20-lead surface-mountable wide-body SOICs (suffix LB).

FEATURES

- TTL, DTL, MOS, CMOS Compatible Inputs
- Transient-Protected Outputs
- Loads to 480 Watts
- Heat-Sink Contact Tabs on Quad Arrays

Always order by complete part number, e.g., **ULN2061M** . See matrix on next page. Note that all devices are not available in all package types.



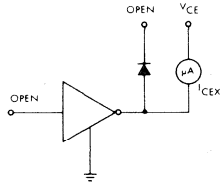
Dwg. GP-027

SELECTION GUIDE

Part Number*	Max. V_{CEX}	Min. $V_{CE(SUS)}$	Max. V_{IN}	Application
ULN2061M	50 V	35 V	30 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULN2062M	80 V	50 V	60 V	
ULN2064B ULN2064LB	50 V	35 V	15 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULN2065B	80 V	50 V	15 V	
ULN2068B ULN2068LB	50 V	35 V	15 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULN2069B	80 V	50 V	15 V	
ULN2074B	50 V	35 V	30 V	General Purpose

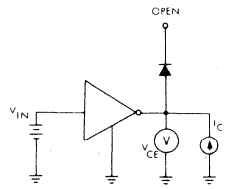
* Suffixes 'LB' are SOICs, 'B' and 'M' are DIPs.

TEST FIGURES



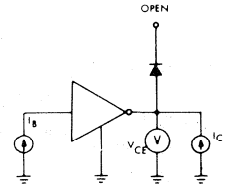
Dwg. No. A-9729A

FIGURE 1



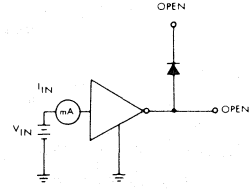
Dwg. No. A-10,350

FIGURE 2



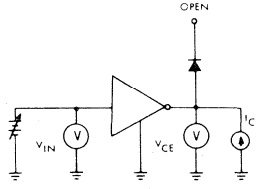
Dwg. No. A-10,349

FIGURE 3



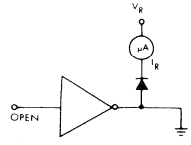
Dwg. No. A-9732

FIGURE 4



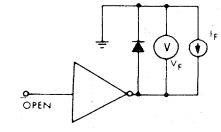
Dwg. No. A-9734A

FIGURE 5



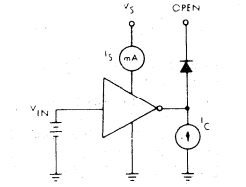
Dwg. No. A-9735A

FIGURE 6



Dwg. No. A-9736

FIGURE 7

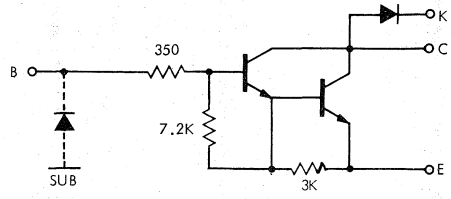


Dwg. No. A-10,351

FIGURE 8

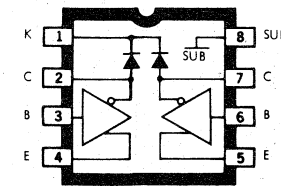
2061 THRU 2074
1.5 A DARLINGTON SWITCHES

PARTIAL SCHEMATIC



Dwg. No. A-10,352B

ULN2061/62M



Dwg. No. A-10,230A

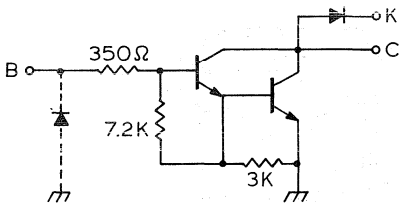
ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN2061M	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN2062M	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2061M	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN2062M	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, I_B = 625 µA	—	1.1	V
				I_C = 750 mA, I_B = 935 µA	—	1.2	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.3	V
				I_C = 1.25 A**, I_B = 2.0 mA	—	1.4	V
			ULN2062M	I_C = 1.5 A**, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.4 V	1.4	4.3	mA
				V_{IN} = 3.75 V	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
			ULN2061M	V_{CE} = 2.0 V, I_C = 1.25 A**	—	2.5	V
			ULN2062M	V_{CE} = 2.0 V, I_C = 1.5 A**	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.5	µs
Clamp Diode Leakage Current	I_R	6	ULN2061M	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = 70°C	—	100	µA
			ULN2062M	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = 70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

**Pulse-Test

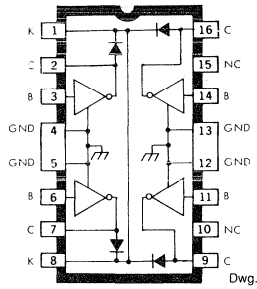
2061 THRU 2074
1.5 A DARLINGTON SWITCHES

PARTIAL SCHEMATIC



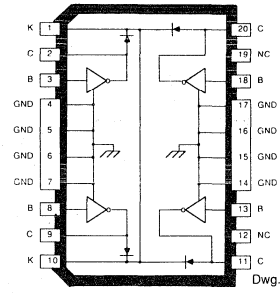
Dwg. No. A-10,353C

ULN2064/65B



Dwg. No. A-9765A

ULN2064LB



Dwg. No. A-14,326

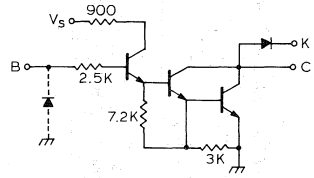
ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	1	ULN2064*	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN2065B	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2064*	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN2065B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, I_B = 625 µA	—	1.1	V
				I_C = 750 mA, I_B = 935 µA	—	1.2	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.3	V
				I_C = 1.25 A, I_B = 2.0 mA	—	1.4	V
			ULN2065B	I_C = 1.5 A, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.4 V	1.4	4.3	mA
				V_{IN} = 3.75 V	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
			ULN2064*	V_{CE} = 2.0 V, I_C = 1.25 A	—	2.5	V
			ULN2065B	V_{CE} = 2.0 V, I_C = 1.5 A	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.5	µs
Clamp Diode Leakage Current	I_R	6	ULN2064*	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = 70°C	—	100	µA
			ULN2065B	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = 70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

* Complete part number includes suffix to identify package style: B = DIP with heat sink tabs, LB = SOIC with heat sink tabs.

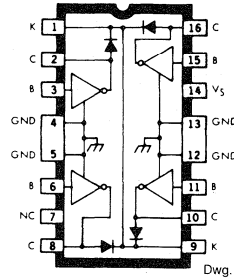
2061 THRU 2074
1.5 A DARLINGTON SWITCHES

PARTIAL SCHEMATIC



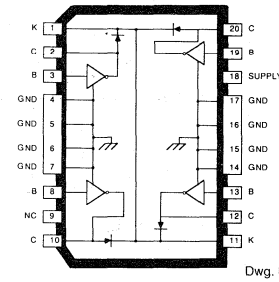
Dwg. No. A-10,354C

ULN2068/69B



Dwg. No. A-10,310

ULN2068LB



Dwg. No. A-14,327

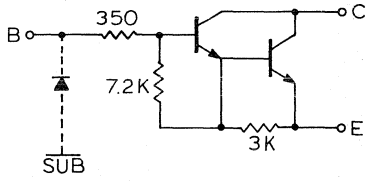
ELECTRICAL CHARACTERISTICS at +25°C, V_S = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	1	ULN2068*	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN2069B	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2069*	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN2069B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, V_{IN} = 2.75 V	—	1.1	V
				I_C = 750 mA, V_{IN} = 2.75 V	—	1.2	V
				I_C = 1.0 A, V_{IN} = 2.75 V	—	1.3	V
				I_C = 1.25 A, V_{IN} = 2.75 V	—	1.4	V
			ULN2069B	I_C = 1.5 A, V_{IN} = 2.75 V	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.75 V	—	550	µA
				V_{IN} = 3.75 V	—	1000	µA
Input Voltage	$V_{IN(ON)}$	5	ULN2068*	V_{CE} = 2.0 V, I_C = 1.25 A	—	2.75	V
			ULN2069B	V_{CE} = 2.0 V, I_C = 1.5 A	—	2.75	V
Supply Current	I_S	8	Both	I_C = 500 mA, V_{IN} = 2.75 V	—	6.0	V
Turn-On Delay	t_{PLH}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	Both	0.5 E_{in} to 0.5 E_{out}, I_C = 1.25 A	—	1.5	µs
Clamp Diode Leakage Current	I_R	6	ULN2068*	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = 70°C	—	100	µA
			ULN2069B	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = 70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

*Complete part number includes suffix to identify package style: B = DIP with heat sink tabs, LB = SOIC with heat sink tabs.

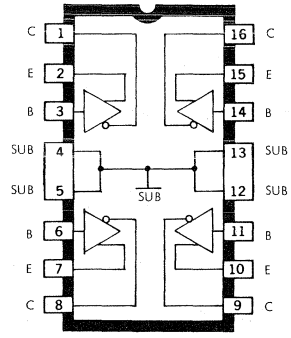
2061 THRU 2074
1.5 A DARLINGTON SWITCHES

PARTIAL SCHEMATIC



Dwg. No. A-10,355B

ULN2074B

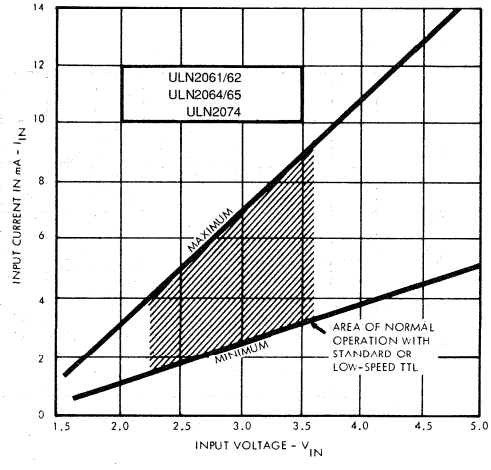


Dwg. No. A-9766

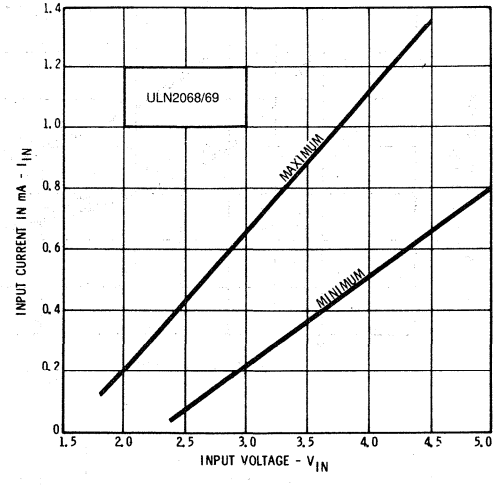
ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	1	V_{CE} = 50 V	—	100	µA
			V_{CE} = 50 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	I_C = 500 mA, I_B = 625 µA	—	1.1	V
			I_C = 750 mA, I_B = 935 µA	—	1.2	V
			I_C = 1.0 A, I_B = 1.25 mA	—	1.3	V
			I_C = 1.25 A, I_B = 2.0 mA	—	1.4	V
Input Current	$I_{IN(ON)}$	4	V_{IN} = 2.4 V	1.4	4.3	mA
			V_{IN} = 3.75 V	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
			V_{CE} = 2.0 V, I_C = 1.25 A	—	2.5	V
Turn-On Delay	t_{PLH}	—	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	0.5 E_{in} to 0.5 E_{out}	—	1.5	µs

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE AT +25°C

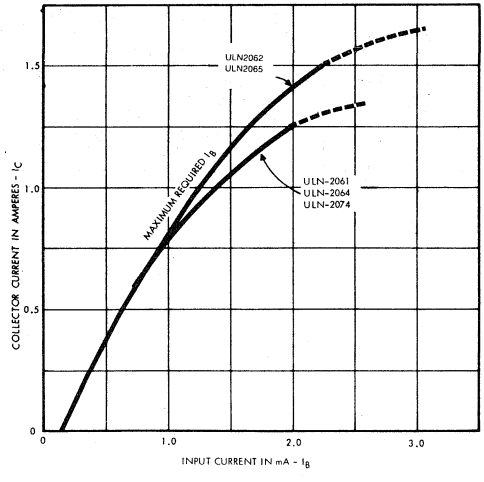


Dwg. No. A-10,363C



Dwg. No. A-12,306A

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT AT +25°C



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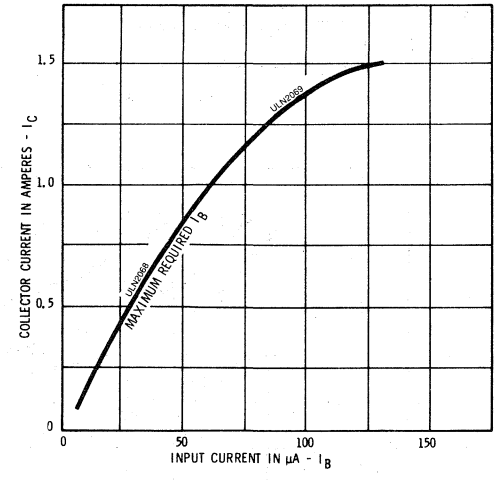
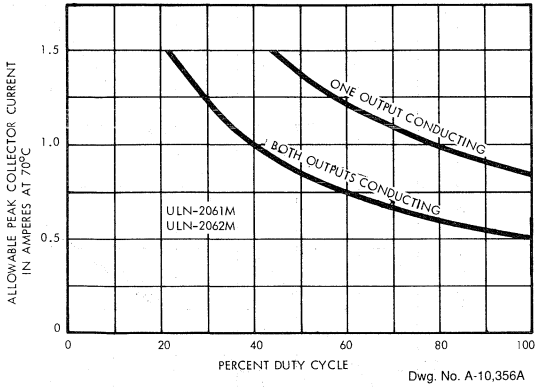
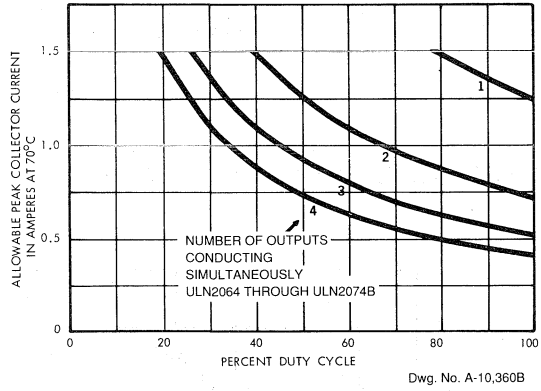


Dwg. No. A-12,306A

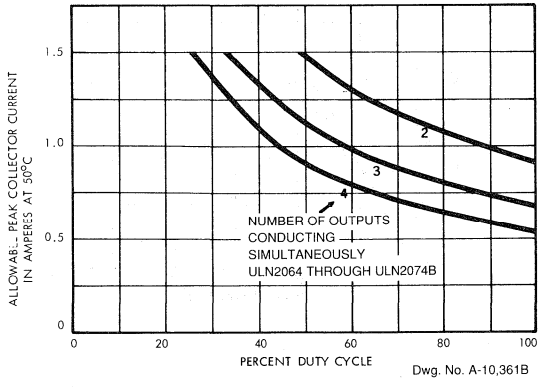
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE
(DUAL IN-LINE PACKAGED DEVICES)



Dwg. No. A-10,356A



Dwg. No. A-10,360B



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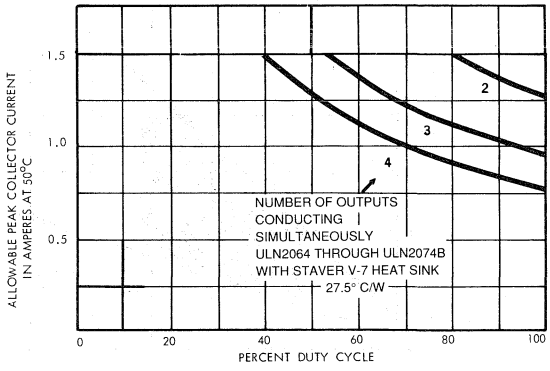
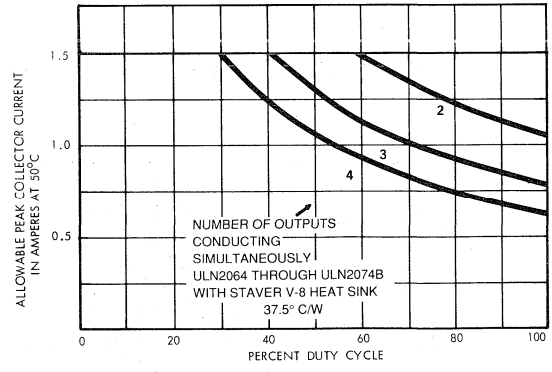
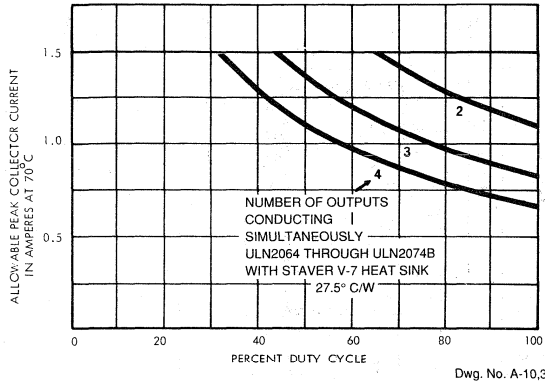


Dwg. No. A-10,398C

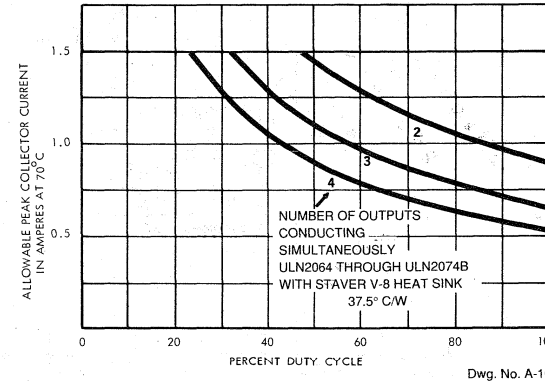


Dwg. No. A-10,400C

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE
(DUAL IN-LINE PACKAGED DEVICES, cont'd)

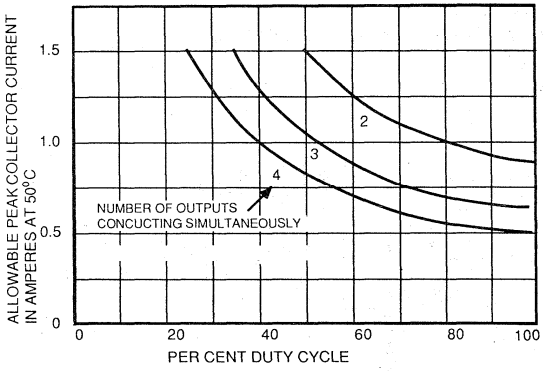


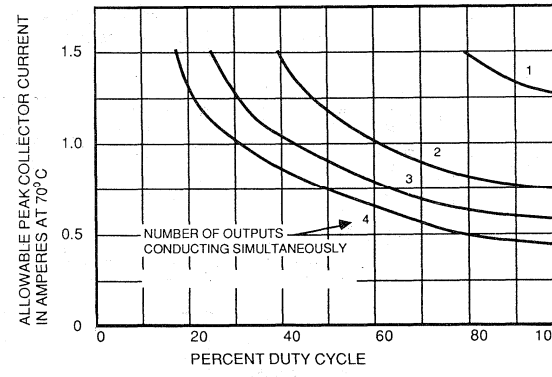
Dwg. No. A-10,399C



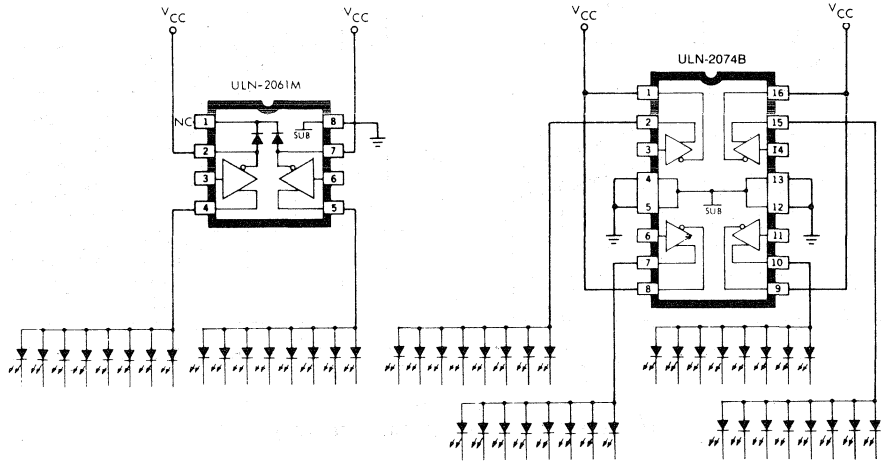
Dwg. No. A-10,401C

(ULN2064LB and ULN2068LB only)





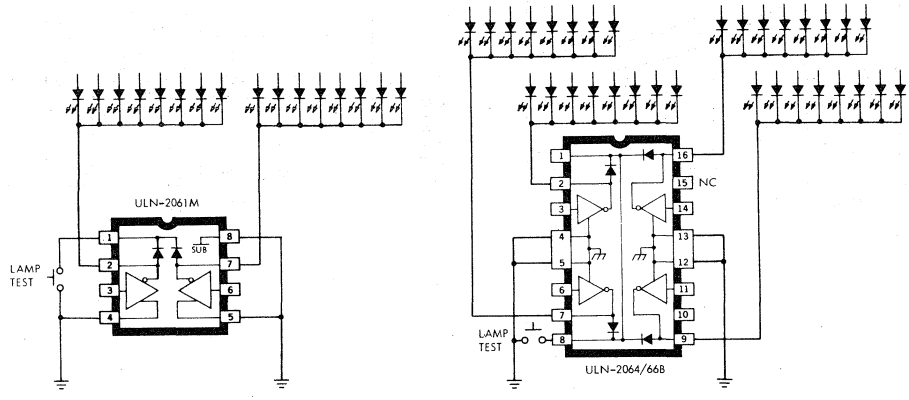
TYPICAL APPLICATIONS



Dwg. No. B-1364A

COMMON-ANODE LED DRIVERS

(Series UDN2980A/EP/LW devices can be used in similar applications at currents of up to 500 mA)



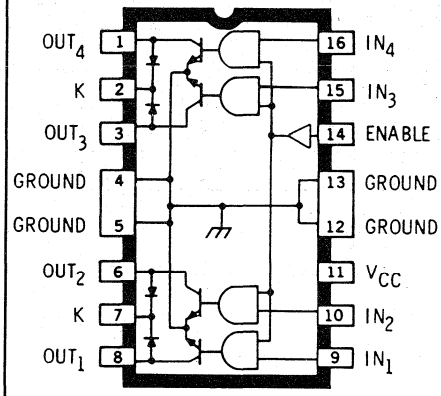
Dwg. No. B-1365

COMMON-CATHODE LED DRIVERS

(Type ULN2068B/LB is also applicable)

2540

QUAD DARLINGTON POWER DRIVER



Dwg. No. A-11,561A

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} . . . . . **50 V**
Output Current, I_{OUT} (peak) . . . . . **2.5 A**
(continuous) . . . . . **1.8 A**
Logic Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} . . . . . **7.0 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Combining AND logic gates and inverting high-current bipolar outputs, the UDN2540B quad Darlington power driver provides interface between low-level signal-processing circuits and power loads totaling 360 W. Each of the four independent outputs can sink up to 1.8 A in the ON state with peak inrush currents to 2.5 A. The four power outputs are each comprised of an open-collector Darlington driver and an internal flyback/clamp diode for switching inductive leads. They feature a minimum breakdown and sustaining voltage of 50 V. The logic inputs are compatible with TTL and 5 V CMOS logic systems.

Typical applications include print heads, relays, solenoids, and dc stepping motors. The UDN2540B can also be used to drive high-current incandescent lamps, LEDS, and heaters. A similar device, specifically intended for driving a unipolar stepper motor in the two-phase drive format, is the UDN2544B.

The UDN2540B is supplied in a 16-pin batwing power DIP. The batwing construction provides for maximum package power dissipation in a standard DIP construction. At 25°C, and with only 1 sq. in. of copper foil at the ground tabs, the package is capable of safely dissipating 3.8 W.

FEATURES

- 1.8 A Continuous Output Current
- Output Voltage to 50 V
- TTL and 5 V CMOS Compatible Inputs
- Efficient Input/Output Pinning
- Integral Transient-Suppression Diodes
- Replaces L6221A

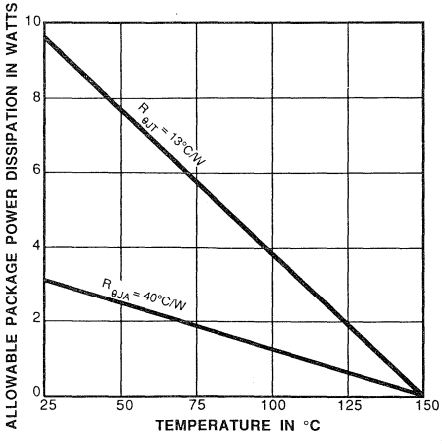
Always order by complete part number: **UDN2540B** .

2540
QUAD DARLINGTON POWER DRIVER

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $T_J \leq$ 150°C, V_{CC} = 4.75 V to 5.25 V.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V, V_{IN} = 0.8 V, V_{EN} = 2.4 V	—	<1.0	100	µA
		V_{OUT} = 50 V, V_{IN} = 2.4 V, V_{EN} = 0.8 V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = 1.8 A, L = 3.0 mH	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 600 mA, V_{IN} = V_{EN} = 2.4 V	—	0.9	1.0	V
		I_{OUT} = 1.0 A, V_{IN} = V_{EN} = 2.4 V	—	1.0	1.2	V
		I_{OUT} = 1.8 A, V_{IN} = V_{EN} = 2.4 V	—	1.3	1.6	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.4	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.4 V	—	—	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	—	-100	µA
Total Supply Current	I_{CC}	V_{IN}* = V_{EN} = 2.4 V, V_{CC} = 5.0 V, Outputs Open	—	14	20	mA
		V_{IN}* = V_{EN} = 0.8 V, V_{CC} = 5.0 V	—	0.4	2.0	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.3	1.6	V
		I_F = 1.8 A	—	1.6	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	<1.0	100	µA

Typical Data is for design information only.
*All inputs simultaneously, all other tests are performed with each input tested separately.



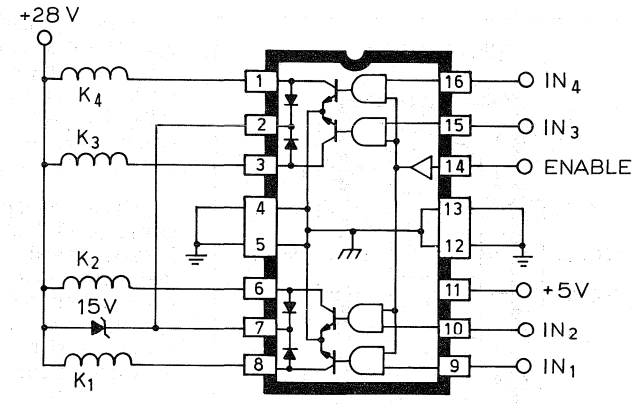
Dwg. GP-004-1

TRUTH TABLE

ENABLE	IN_N	OUT_N
H	H	ON
—	L	OFF
L	X	OFF

X = Don't care.

TYPICAL APPLICATION
(QUAD RELAY DRIVER WITH ZENER FLYBACK)



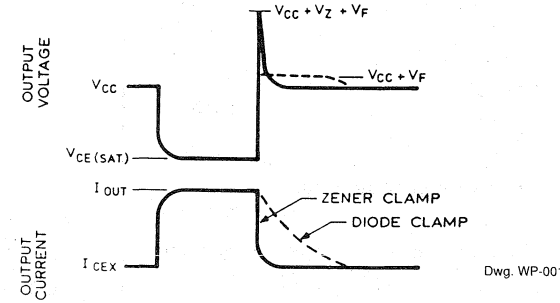
Dwg. EP-016

APPLICATIONS INFORMATION

A typical application is shown for driving four high-current relays, solenoids, or print heads. A Zener diode is used to increase the flyback voltage, providing a much faster inductive load turn-OFF current decay, resulting in faster dropout (reduced relay contact arcing), and improved performance. The maximum Zener voltage, plus the load supply voltage, plus the flyback diode forward voltage must not exceed the device's rated sustaining voltage.

With external control circuitry, the ENABLE input can be used for chopper (PWM) applications. If the ENABLE input is not used, it should be tied high.

All inputs will float high if open circuited.

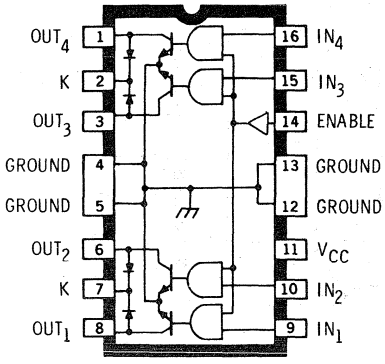


Dwg. WP-001

2543

PROTECTED QUAD POWER DRIVERS

UDN2543B



Dwg. No. A-11,561A

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} . . . . . **60 V**
Over-Current Protected Output Voltage, V_{OUT} . . . . . **25 V**
Output Current, I_{OUT} . . . . . **1.0 A***
Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} or V_{EN} . . . . . **18 V**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

*Outputs are peak current limited at approximately 1.0 A per driver. See Circuit Description and Applications for further information.

Providing interface between low-level signal processing circuits and power loads to 240 W, the UDN2543B and UDN2543EB quad power drivers combine NAND logic gates and high-current bipolar outputs. Each of the four independent outputs can sink up to 700 mA in the ON state. The outputs have a minimum breakdown voltage of 60 V and a sustaining voltage of 35 V. The inputs are compatible with most TTL, DTL, LSTTL, and 5 V CMOS and PMOS logic systems.

Over-current protection has been designed into each channel of the UDN2543B/EB and typically occurs at 1 A. It protects any one channel from output short circuits with supply voltages up to 25 V. When the maximum output current is reached, that output stage is driven linearly. If the over-current condition continues, that output's thermal limiting will operate, limiting that output's power dissipation. The outputs also include transient suppression diodes for use with inductive loads such as relays, solenoids, or dc stepping motors.

The UDN2543B is supplied in a 16-pin power DIP while the UDN2543EB is a 28-lead power PLCC for surface-mount applications. Both packages are of batwing construction to provide for maximum package power dissipation. They are rated for continuous operation over the temperature range of -20°C to +85°C. Similar devices for use in automotive applications, or over an extended temperature range, are available as the UDQ2543B and UDQ2543EB.

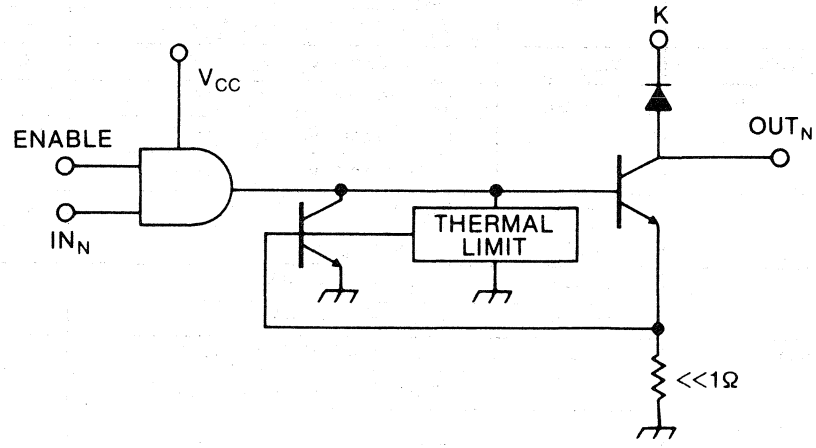
FEATURES

- 700 mA Output Current per Channel
- Output Voltage to 60 V
- Low Output-Saturation Voltage
- Integral Output Transient-Suppression Diodes
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- Independent Over-Current Protection for Each Output

Always order by complete part number:

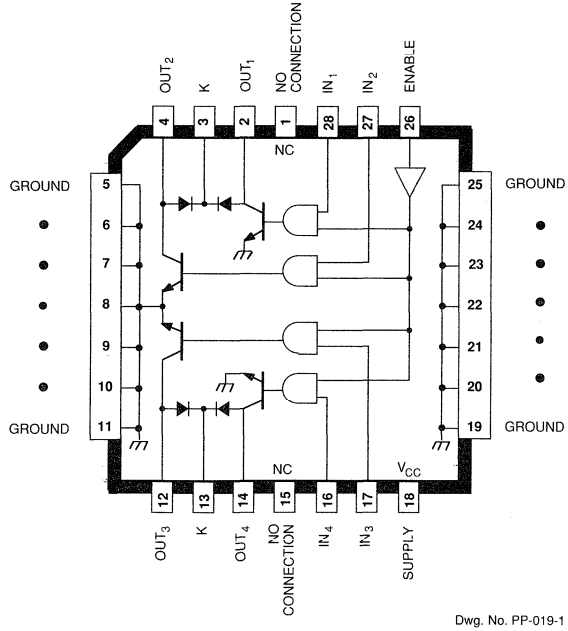
Part Number	Package
UDN2543B	16-Pin DIP
UDN2543EB	28-Lead PLCC

FUNCTIONAL BLOCK DIAGRAM
(1 OF 4 CHANNELS)

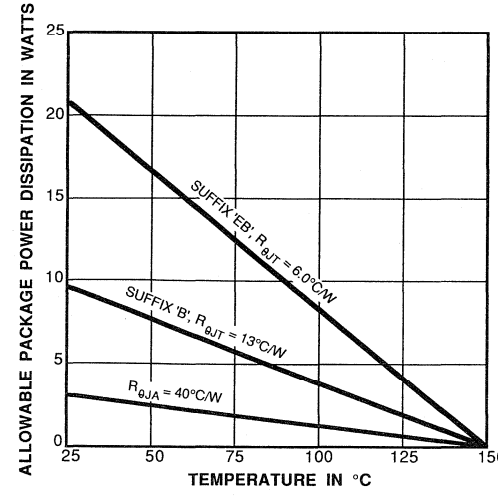


Dwg. No. D-1005

UDN2543EB



Dwg. No. PP-019-1



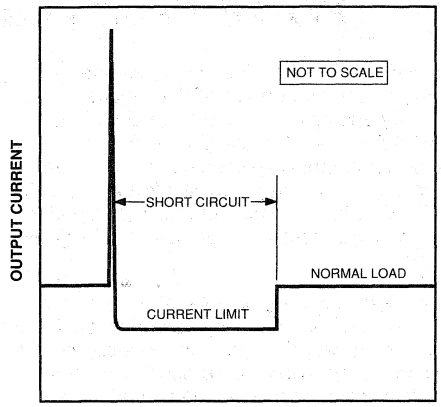
Dwg. GP-010A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.75 V to 5.25 V

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{EN} = 2.0 V	—	100	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{EN} = 0.8 V	—	100	µA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 0.8 V	35	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 2.0 V	—	200	mV
		I_{OUT} = 400 mA, V_{IN} = V_{EN} = 2.0 V	—	400	mV
		I_{OUT} = 700 mA, V_{IN} = V_{EN} = 2.0 V	—	600	mV
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.0 V	—	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	-10	µA
Total Supply Current	I_{CC}	I_{OUT} = 700 mA, V_{IN}* = V_{EN} = 2.0 V	—	65	mA
		Outputs Open, V_{IN}* = 0.8 V, V_{EN} = 2.0 V	—	15	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.6	V
		I_F = 1.5 A	—	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 60 V, V_{IN} = V_{EN} = 2.0 V, $D_1 + D_2$ or $D_3 + D_4$	—	50	µA

* All inputs simultaneously, all other tests are performed with each input tested separately.

TYPICAL OUTPUT BEHAVIOR



Dwg. WP-013

CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON/in-rush currents can destroy semiconductor lamp drivers and contribute to poor lamp reliability. However, lamps with steady-state current ratings up to 500 mA can be driven with the UDN2543B/EB without the need for warming or current-limiting resistors.

When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current. With the UDN2543B/EB, during turn-ON, the high in-rush current is sensed by the internal low-value sense resistor. Drive current to the output stage is then diverted by the shunting transistor and the load current is momentarily limited to approximately 1.0 A. During this transition period, the output stage is driven in a linear fashion. During lamp warmup, the filament resistance increases to its maximum value, the output stage goes into saturation and applies full supply voltage to the lamp.

INDUCTIVE LOAD DRIVER

Bifilar (unipolar) stepper motors, relays, or solenoids can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes which occur when turning OFF an inductive load.

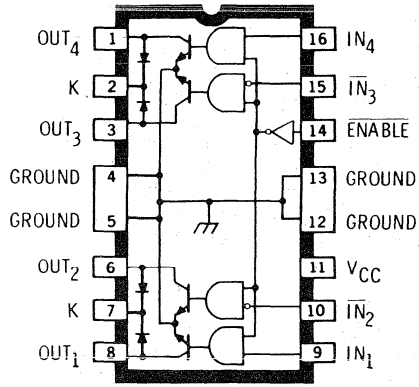
FAULT CONDITIONS

In the event of a shorted load, the load current will attempt to increase. As described above, the drive current to the affected output stage is diverted, causing the output stage to go linear, limiting the peak output current to approximately 1 A. As the power dissipation of that output stage increases, a thermal gradient sensing circuit will become operational, further decreasing the drive current to the affected output stage and reducing the output current to a value dependent on supply voltage and load resistance. If the fault condition is corrected, the output stage will return to its normal saturated condition.

Due to the independent operation of the four channels, only a single channel should be shorted at a time. Multiple overload conditions may be tolerated provided rated package power dissipation is not exceeded.

2544

QUAD DARLINGTON POWER DRIVER



Dwg. No. PP-017

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} . . . . . **50 V**
Output Current, I_{OUT}
(Peak) . . . . . **2.5 A**
(Continuous) . . . . . **1.8 A**
Logic Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} . . . . . **7.0 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Combining logic gates and high-current bipolar outputs, the UDN2544B quad Darlington power driver provides an interface between low-level logic circuitry and high-power loads. Each of the four outputs can sink up to 1.8 A in the ON state with peak inrush currents to 2.5 A. The four power outputs are each comprised of an open-collector Darlington driver and an internal flyback/clamp diode for switching inductive loads. They feature a minimum breakdown and sustaining voltage of 50 V. The logic inputs are compatible with TTL and 5 V CMOS logic systems.

This device is particularly well-suited for unipolar stepper motor drive applications. With complementary control inputs and an active-low ENABLE, the UDN2544B makes it easy to implement full stepping of a stepper motor with only two microcontroller/microprocessor control lines. Other typical applications include relay or solenoid driving and incandescent or LED lamp driving.

The UDN2544B is supplied in a 16-pin batwing power DIP. The batwing construction provides for maximum package power dissipation in a standard DIP construction. At 25°C, and with only 1 sq. in. of copper foil at the ground tabs, the package is capable of safely dissipating 3.8 W.

FEATURES

- 1.8 A Continuous Output Current
- Output Voltage to 50 V
- Inputs Configured for Unipolar Stepper Motors
- Active-Low Output Enable
- TTL and 5 V CMOS Compatible Inputs
- Integral Transient-Suppression Diodes

Always order by complete part number: **UDN2544B** .

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ 150°C, V_{CC} = 4.75 V to 5.25 V.

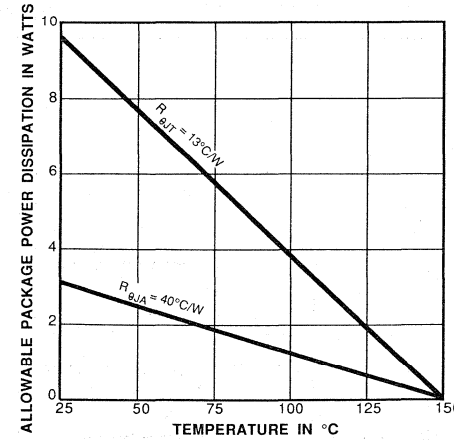
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = 1.8 A, L = 3.0 mH	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 600 mA	—	0.9	1.0	V
		I_{OUT} = 1.0 A	—	1.0	1.2	V
		I_{OUT} = 1.8 A	—	1.3	1.6	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.4	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.4 V	—	—	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	—	-100	µA
Total Supply Current	I_{CC}	All Outputs ON, Outputs Open	—	14	20	mA
		All Outputs OFF	—	0.4	2.0	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.3	1.6	V
		I_F = 1.8 A	—	1.6	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	< 1.0	100	µA

Typical Data is for design information only

TRUTH TABLE

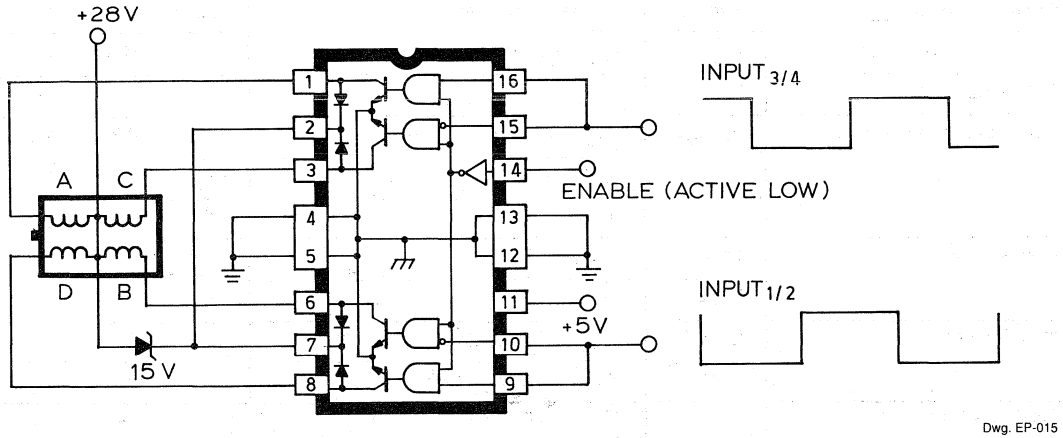
ENABLE	IN_1	OUT_1	IN_2	OUT_2	IN_3	OUT_3	IN_4	OUT_4
L	H	ON	H	OFF	H	OFF	H	ON
	L	OFF	L	ON	L	ON	L	OFF
H	X	OFF	X	OFF	X	OFF	X	OFF

X = Don't care



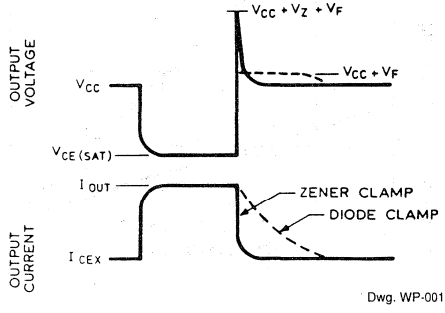
DWG. GP-004-1

TYPICAL APPLICATION
(UNIPOLAR STEPPER MOTOR WITH ZENER FLYBACK)



TRUTH TABLE

INPUTS		WINDINGS			
1/2	3/4	A	B	C	D
L	H	ON	ON	OFF	OFF
L	L	OFF	ON	ON	OFF
H	L	OFF	OFF	ON	ON
H	H	ON	OFF	OFF	ON



APPLICATIONS INFORMATION

A typical application is shown driving a four-phase unipolar stepper motor. Note that with the complimentary control inputs, only two logic signals are needed to drive the motor in the two-phase format. The two phase drive format illustrated, energizes two adjacent phases in each detent position (AB, BC, CD, DA) to provide an improved torque-speed product and greater detent torque.

A Zener diode can be used to increase the flyback voltage. The increased flyback voltage gives a much faster inductive load turn-OFF current decay resulting in improved motor performance. The maximum Zener voltage, plus the load supply voltage, plus the flyback diode forward voltage must not exceed the device's rated sustaining voltage.

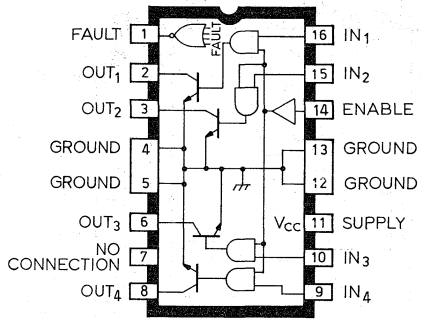
With external control circuitry, the ENABLE input (active low) can be used for chopper (PWM) applications. If the ENABLE input is not used, it should be tied low.

All inputs will float high if open circuited.

2547

PROTECTED QUAD POWER DRIVERS

UDN2547B



Dwg. PP-018

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} . . . . . **60 V**
Over-Current Protected Output Voltage, V_{OUT} . . . . . **25 V**
Output Current, I_{OUT} . . . . . **1.3 A***
FAULT Output Voltage, V_F . . . . . **40 V**
Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} or V_{EN} . . . . . **7.0 V**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-20°C to + 85°C**
Storage Temperature Range, T_S . . . . . **-55°C to + 150°C**

*Outputs are current limited at approximately 1.3 A per driver and junction temperature limited if current in excess of 1.3 A is attempted. See Circuit Description and Application for further information.

Always order by complete part number:

Part Number	Package
UDN2547B	16-Pin DIP
UDN2547EB	28-Lead PLCC

Providing interface between low-level signal processing circuits and power loads, the UDN2547B and UDN2547EB quad power drivers combine logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 600 mA in the ON state. The outputs have a minimum breakdown voltage of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems and include internal pull-down resistors to insure that the outputs remain OFF if the inputs are open-circuited.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1.3 A. It protects each output from short circuits with supply voltages up to 25 V. When a maximum driver output current is reached, that output drive is reduced linearly, maintaining a constant load current. If the over-current or short circuit condition continues, each channel has an independent thermal limit circuit which will sense the rise in junction temperature and turn OFF the individual channel that is at fault. Foldback circuitry decreases the output current if excessive voltage is present across the output and assists in keeping the device within its SOA (safe operating area).

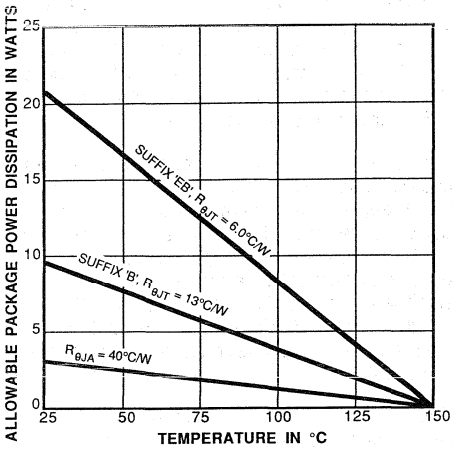
Each output also includes diagnostics for increased device protection. If any output is shorted or opened, the diagnostics can signal the controlling circuitry through a common FAULT pin.

The UDN2547B/EB can be used to drive various resistive loads including incandescent lamps (without warming or limiting resistors). With the addition of external output clamp diodes, the UDN2547B/EB can be used to drive inductive loads such as relays, solenoids, or dc stepping motors.

The UDN2547B is a 16-lead power DIP while the UDN2547EB is a 28-lead power PLCC for surface-mount applications. Both packages are of batwing construction to provide for maximum package power dissipation. They are rated for continuous operation over the temperature range of -20°C to + 85°C. Similar devices for use in automotive applications, or over an extended temperature range, are available as the UDQ2547B and UDQ2547EB.

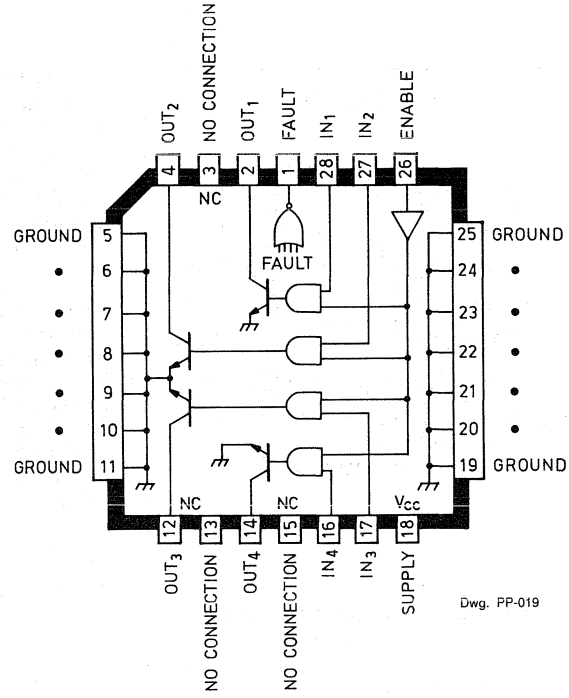
FEATURES

- 600 mA Output Current per Channel
- Independent Over-Current Protection for Each Driver
- Independent Thermal Protection for Each Driver
- Output Voltage to 60 V
- Output SOA Protection
- Low Output-Saturation Voltage
- TTL and 5 V CMOS Compatible Inputs
- Diagnostic FAULT Output



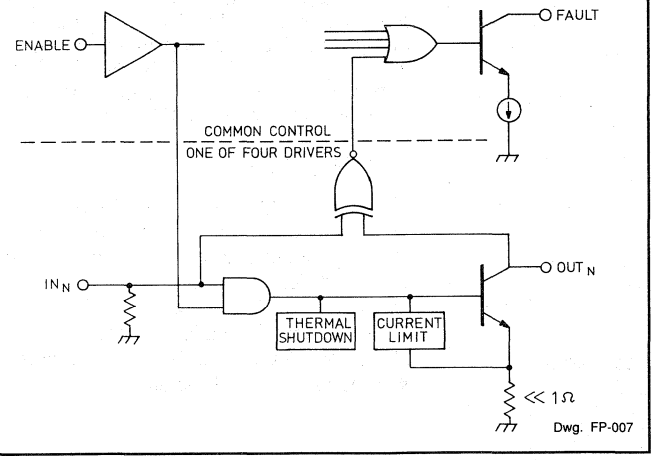
Dwg. GP-010A

UDN2547EB



Dwg. PP-019

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-007

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{CC} = 4.75 V to 5.5 V

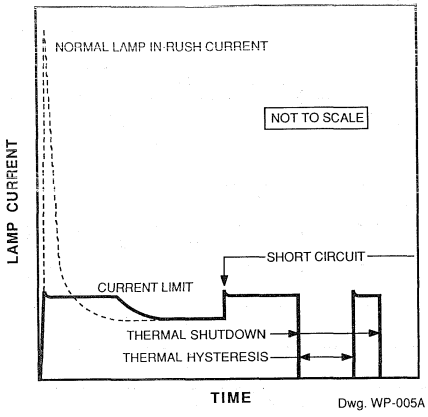
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{OUT}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{EN} = 2.0 V	—	30	100	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{EN} = 0.8 V	—	30	100	µA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA, V_{IN} = 0.8 V, V_{CC}= Open	40	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 400 mA	—	—	300	mV
		I_{OUT} = 500 mA	—	—	400	mV
		I_{OUT} = 600 mA	—	—	550	mV
Over-Current Limit	I_{OUT}	5 ms PulseTest, V_{OUT} = 5.0 V	—	1. 3	1.7	A
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.0 V	—	—	60	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	10	—	—	µA
Fault Output Leakage Current	I_F	V_F = 40 V	—	<1.0	2.0	µA
Fault Output Current	I_F	V_F = 40 V, Driver Outputs Open, V_{IN} = 0.8 V, V_{EN} = 2.0 V	40	60	80	µA
Fault Output Saturation Voltage	$V_{F(SAT)}$	I_F = 30 µA	—	0.1	0.4	V
Total Supply Current	I_{CC}	All Outputs ON	—	45	50	mA
		All Outputs OFF	—	6.0	10	mA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Hysteresis	ΔT_J		—	15	—	°C

Typical Data is for design information only.

TRUTH TABLE

STATUS	IN_N	ENABLE	OUT_N	FAULT
Normal Load	H	H	L	H
	L	H	H	H
	X	L	H	H
Over-Current or Short to Supply	H	H	R	L
Thermal Fault	H	H	H	L
Open Load or Short to Ground	L	H	L	L

X = Don't care.
R = Linear drive, current limited.



CIRCUIT DESCRIPTION AND APPLICATION

The UDN2547B or UDN2547EB monitors its outputs for open or shorted conditions. Both conditions are sensed by comparing the input and output states. Note that the FAULT output is operational only if the ENABLE input is high. When a fault condition is sensed, the FAULT output will go to a low state. An external FAULT output filter capacitor is recommended to eliminate erroneous switching.

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON/in-rush currents can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warming or current-limiting resistors protect both driver and lamp but use significant power either when the lamp is OFF or when the lamp is ON, respectively. Lamps with steady-state current ratings up to 600 mA can be driven by the UDN2547B/EB without the need for warming or current-limiting resistors.

When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current. With the UDN2547B/EB drivers, during turn-ON, the high in-rush current is sensed by the internal low-value sense resistor, drive current to the output stage is diverted by the shunting transistor, and the load current is limited to approximately 1.3 A. During this short transition period, the ouput driver is driven in a linear fashion. During lamp warmup, the filament resistance increases to its maximum value, the output driver goes into saturation and applies maximum rated voltage to the lamp.

INDUCTIVE LOAD DRIVER

With the addition of external clamp diodes, bifilar (unipolar) stepper motors and other inductive loads can be driven directly. The external diodes prevent damage to the output transistors by suppressing the high-voltage spikes which occur when turning OFF an inductive load.

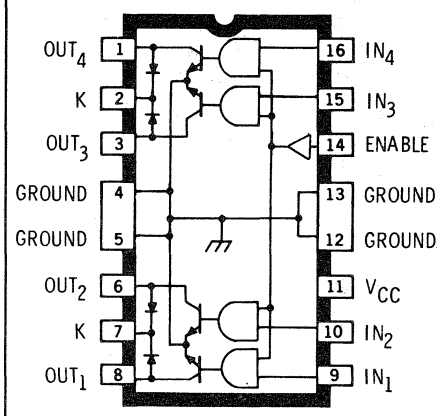
OVER-CURRENT CONDITIONS

In the event of a shorted load, or stalled motor, the load current will attempt to increase. As described above, the drive current to the affected output stage is linearly reduced (limiting the load current to about 1.3 A), causing the output stage to go linear. As the junction temperature of the output stage increases, the thermal shutdown circuit will shut OFF the affected output. If the fault condition is corrected, the output driver will return to its normal saturated condition.

2549

PROTECTED QUAD POWER DRIVERS

UDN2549B



Dwg. No. A-11,561A

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} . . . . . **60 V**
Over-Current Protected Output Voltage, V_{OUT} . . . . . **25 V**
Output Current, I_{OUT} . . . . . **1.0 A***
Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} or V_{EN} . . . . . **7.0 V**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

*Outputs are peak current limited at approximately 1.0 A per driver. See Circuit Description and Applications for further information.

Providing improved output current limiting, the UDN2549B and UDN2549EB quad power drivers combine NAND logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 600 mA in the ON state. The outputs have a minimum breakdown voltage of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1 A. It protects each output from short circuits with supply voltages up to 25 V. When an output current trip point is reached, that output stage is driven linearly resulting in a reduced output current level. If an over-current or short circuit condition continues, the thermal limiting circuits will first sense the rise in junction temperature and then the rise in chip temperature, further decreasing the output current. Under worst-case conditions, the UDN2549B/EB will tolerate short-circuits on all outputs, simultaneously.

These devices can be used to drive various loads including incandescent lamps (without warming or limiting resistors) or inductive loads such as relays, solenoids, or dc stepping motors.

The UDN2549B is a 16-pin power DIP while the UDN2549EB is a 28-lead power PLCC for surface-mount applications. Both packages are of batwing construction to provide for maximum package power dissipation. They are rated for continuous operation over the temperature range of -20°C to +85°C. Similar devices for use in automotive applications, or over an extended temperature range, are available as the UDQ2549B and UDQ2549EB.

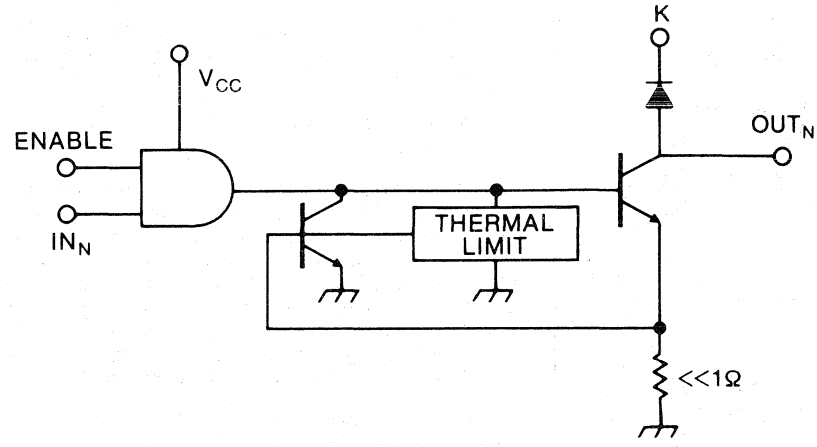
FEATURES

- 600 mA Output Current per Channel
- Independent Over-Current Protection for Each Driver
- Thermal Protection for Device and Each Driver
- Output Voltage to 60 V
- Low Output-Saturation Voltage
- Integral Output Flyback Diodes
- TTL and 5 V CMOS Compatible Inputs
- Pin-Compatible With UDN2543B/EB

Always order by complete part number:

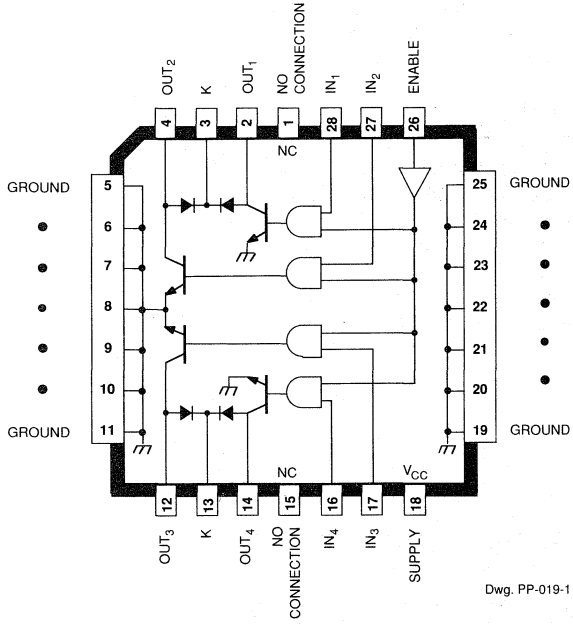
Part Number	Package
UDN2549B	16-Pin DIP
UDN2549EB	28-Lead PLCC

FUNCTIONAL BLOCK DIAGRAM
(1 of 4 Channels)

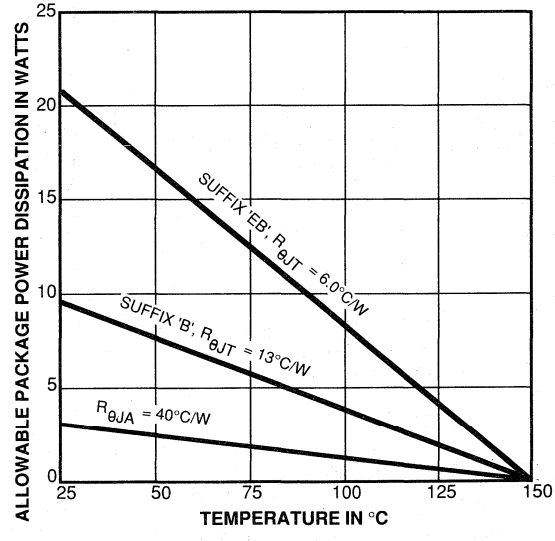


Dwg. No. D-1005

UDN2549EB



Dwg. PP-019-1



Dwg. GP-010A

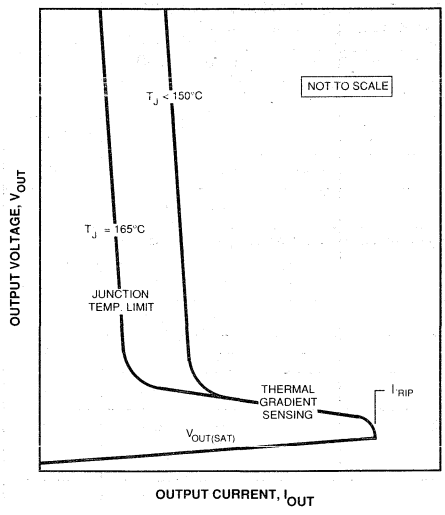
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.75 V to 5.25 V

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{EN} = 2.0 V	—	<1.0	100	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{EN} = 0.8 V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 0.8 V	40	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 100 mA	—	—	200	mV
		I_{OUT} = 400 mA	—	—	400	mV
		I_{OUT} = 600 mA	—	—	600	mV
Over-Current Trip	I_{TRIP}		—	1.0	—	A
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.0 V	—	—	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	—	-10	µA
Total Supply Current	I_{CC}	I_{OUT} = 600 mA, V_{IN}* = V_{EN} = 2.0 V	—	—	65	mA
		All Outputs OFF	—	—	15	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	—	1.7	V
Clamp Diode Leakage Current	I_R	V_R = 60 V, D_1 + D_2 or D_3 + D_4	—	—	50	µA
Thermal Limit	T_J		—	165	—	°C

Typical Data is for design information only.

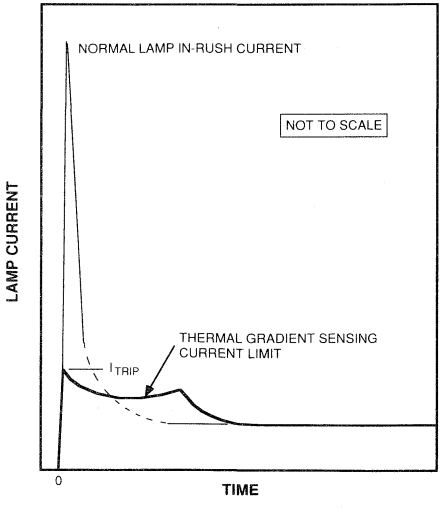
* All inputs simultaneously, all other tests are performed with each input tested separately.

TYPICAL OUTPUT CHARACTERISTIC



Dwg. GP-013

TYPICAL OUTPUT BEHAVIOR



Dwg. WP-008

CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON/in-rush currents can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warming or current-limiting resistors protect both driver and lamp but use significant power either when the lamp is OFF or when the lamp is ON, respectively. Lamps with steady-state current ratings up to 600 mA can be driven by the UDN2549B/EB without the need for warming or current-limiting resistors.

When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current. With the UDN2549B/EB drivers, during turn-ON, the high in-rush current is sensed by the internal low-value sense resistor. Drive current to the output stage is then diverted by the shunting transistor, and the load current is momentarily limited to approximately 1.0 A. During this short transition period, the output current is reduced to a value dependent on supply voltage and filament resistance. During lamp warmup, the filament resistance increases to its maximum value, the output stage goes into saturation and applies maximum rated voltage to the lamp.

INDUCTIVE LOAD DRIVER

Bifilar (unipolar) stepper motors, relays, or solenoids can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes which occur when turning OFF an inductive load.

FAULT CONDITIONS

In the event of a shorted load, the load current will attempt to increase. As described above, the drive current to the affected output stage is reduced, causing the output stage to go linear, limiting the peak output current to approximately 1 A. As the power dissipation of that output stage increases, a thermal gradient sensing circuit will become operational, further decreasing the drive current to the affected output stage and reducing the output current to a value dependent on supply voltage and load resistance.

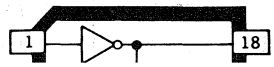
Continuous or multiple overload conditions causing the chip temperature to reach approximately 165°C will result in an additional reduction in output current to maintain a safe level.

If the fault condition is corrected, the output stage will return to its normal saturated condition.

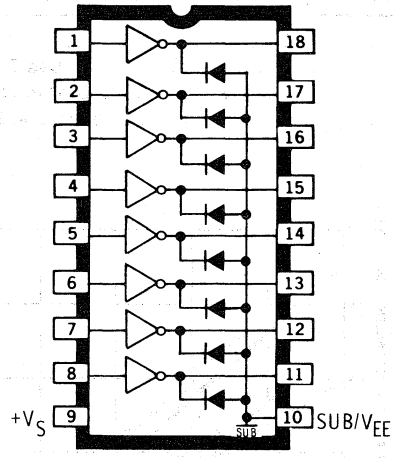
SERIES 2580

8-CHANNEL SOURCE DRIVERS

UDN2580/85LW



UDN2580/85A



Dwg. No. A-11,359

Note that the UDN2580/85A (dual in-line packages) and UND 2580/85LW (small-outline IC packages are electrically identical and share a common pin number assignment.

This versatile family of integrated circuits will work with many combinations of logic- and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers. Series UDN2580A/LW source drivers can drive incandescent, LED, or vacuum fluorescent displays. Internal transient-suppression diodes permit the drivers to be used with inductive loads such as relays, solenoids, dc and stepping motors, and magnetic print hammers.

The Type UDN2580A and UDN2580LW are high-current source drivers used to switch the ground ends of loads that are directly connected to a -50 V supply. Selected devices (UDN2580A-1) may be operated to -80 V. Typical loads are telephone relays, PIN diodes, and LEDs.

The UDN2585A and UDN2585LW are drivers designed for applications requiring low output saturation voltages. Typical loads are low-voltage LEDs and incandescent displays. The eight non-Darlington, 25 V outputs will simultaneously sustain continuous load currents of -120 mA at ambient temperatures to +70°C.

The UDN2588A has separate logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, PMOS) or negative logic (NMOS) and either negative or split-load supplies to -45 V. Selected devices (UDN2588A-1) may be operated to -65 V.

These drivers are packaged in plastic DIPs (suffix A) or surface-mountable wide-body SOICs (suffix LW), and are rated for operation over the temperature range of -20°C to +85°C.

FEATURES

- TTL, CMOS, PMOS, NMOS Compatible
- High Output Current Rating
- Internal Transient Suppression
- Efficient Input/Output Structure

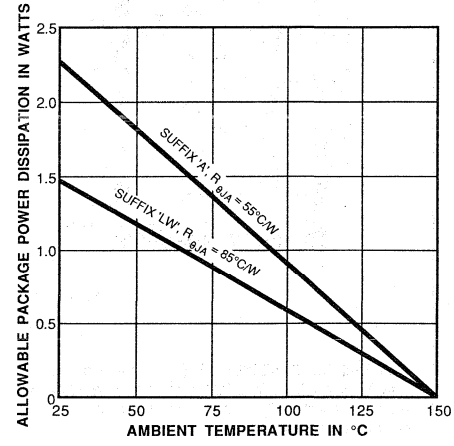
Always order by complete part number: **UDN2580A/LW** .

ABSOLUTE MAXIMUM RATINGS

at 25°C Free-Air Temperature for any one driver (unless otherwise noted).

	UDN2580A/LW	UDN2580A-1	UDN2585A/LW	UDN2588A	UDN2588A-1
Output Voltage, V_{CE}	50 V	80 V	25 V	50 V	80 V
Supply Voltage, V_S (ref. sub.)	50 V	80 V	25 V	50 V	80 V
Supply Voltage, V_{CC} (ref. sub.)	—	—	—	50 V	80 V
Input Voltage, V_{IN} (ref. V_S)	-30 V	-30 V	-20 V	-30 V	-30 V
Total Output Current, ($I_C + I_S$)	-500 mA	-500 mA	-250 mA	-500 mA	-500 mA
Substrate Current I_{SUB}	3.0 A	3.0 A	2.0 A	3.0 A	3.0 A

Package Power Dissipation, P_D (single output) ..... **1.0 W**
(total package) ..... **See Graph**
Operating Temperature Range, T_A ..... **-20°C to +85°C**
Storage Temperature Range, T_S ..... **-55°C to +150°C**



Dwg. GP-018A

For simplification, these devices are characterized on the following pages with specific voltages for inputs, logic supply (V_S), load supply (V_{EE}), and collector supply (V_{CC}). Typical use of the UDN2580A/LW and UDN2580A-1 is with negative referenced logic. The more common application of the UDN2585A/LW, UDN2588A, and UDN2588A-1 is with positive referenced logic supplies. In application, the devices are capable of operation over a wide range of logic and supply voltage levels:

TYPICAL OPERATING VOLTAGES

V_S	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
0 V	-15 V to -3.6 V	-0.5 V to 0 V	NA	-25 V	UDN2585A/LW
				-50 V	UDN2580A/LW
				-80 V	UDN2580A-1
+5 V	0 V to +1.4 V	+4.5 V to +5 V	NA	-20 V	UDN2585A/LW
				-45 V	UDN2580A/LW
				-75 V	UDN2580A-1
			≤ 5 V	-45 V	UDN2588A
				-75 V	UDN2588A-1
+12 V	0 V to +8.4 V	+11.5 V to +12 V	NA	-13 V	UDN2585A/LW
				-38 V	UDN2580A/LW
				-68 V	UDN2580A-1
			≤12 V	-38 V	UDN2588A
				-68 V	UDN2588A-1
+15 V	0 V to +11.4 V	+14.5 V to +15 V	NA	-10 V	UDN2585A/LW
				-35 V	UDN2580A/LW
				-65 V	UDN2580A-1
			≤15 V	-35 V	UDN2588A
				-65 V	UDN2588A-1

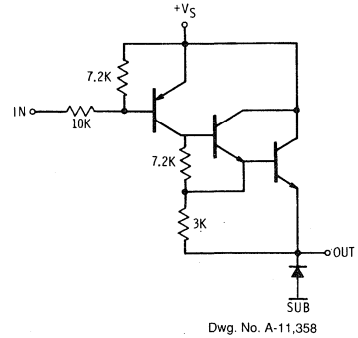
NOTE: The substrate must be tied to the most negative point in the external circuit to maintain isolation between drivers and to provide for normal circuit operation.

UDN2580A, UDN2580LW, AND UDN2580A-1
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 0 V, V_{EE} = -45 V (unless otherwise noted).

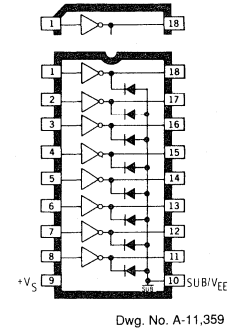
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	UDN2580A/LW	V_{IN} = -0.5 V, V_{OUT} = V_{EE} = -50 V	—	50	µA
			V_{IN} = -0.4 V, V_{OUT} = V_{EE} = -50 V, T_A = 70°C	—	100	µA
		UDN2580A-1	V_{IN} = -0.5 V, V_{OUT} = V_{EE} = -80 V	—	50	µA
			V_{IN} = -0.4 V, V_{OUT} = V_{EE} = -80 V, T_A = 70°C	—	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN2580A/LW	V_{IN} = -0.4 V, I_{OUT} = -25 mA, Note 1	35	—	V
		UDN2580A-1	V_{IN} = -0.4 V, V_{EE} = -75 V, I_{OUT} = -25 mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	ALL	V_{IN} = -2.4 V, I_{OUT} = -100 mA	—	1.8	V
			V_{IN} = -3.0 V, I_{OUT} = -225 mA	—	1.9	V
			V_{IN} = -3.6 V, I_{OUT} = -350 mA	—	2.0	V
Input Current	$I_{IN(ON)}$	ALL	V_{IN} = -3.6 V, I_{OUT} = -350 mA	—	-500	µA
			V_{IN} = -15 V, I_{OUT} = -350 mA	—	-2.1	mA
	$I_{IN(OFF)}$	ALL	I_{OUT} = -500 µA, T_A = 70°C, Note 3	-50	—	µA
Input Voltage	$V_{IN(ON)}$	ALL	I_{OUT} = -100 mA, V_{CE} ≤1.8 V, Note 4	—	-2.4	V
			I_{OUT} = -225 mA, V_{CE} ≤1.9 V, Note 4	—	-3.0	V
			I_{OUT} = -350 mA, V_{CE} ≤2.0 V, Note 4	—	-3.6	V
	$V_{IN(OFF)}$	ALL	I_{OUT} = -500 µA, T_A = 70°C	-0.2	—	V
Clamp Diode Leakage Current	I_R	UDN2580A/LW	V_R = 50 V, T_A = 70°C	—	50	µA
		UDN2580A-1	V_R = 80 V, T_A = 70°C	—	50	µA
Clamp Diode Forward Voltage	V_F	ALL	I_F = 350 mA	—	2.0	V
Input Capacitance	C_{IN}	ALL		—	25	pF
Turn-On Delay	t_{PHL}	ALL	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs
Turn-Off Delay	t_{PLH}	ALL	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs

NOTES: 1. Pulsed test, t_p ≤ 300 µs, duty cycle ≤ 2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

PARTIAL SCHEMATIC



Dwg. No. A-11,358



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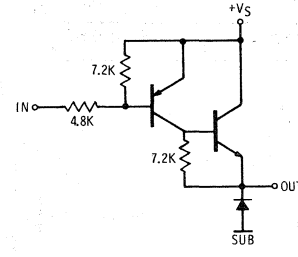
UDN2585A AND UDN2585LW
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 0 V, V_{EE} = -20 V (unless otherwise noted)

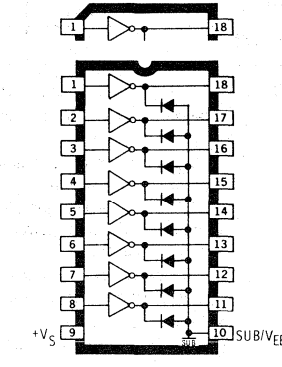
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{IN} = -0.5 V, V_{OUT} = V_{EE} = -25 V	—	50	µA
		V_{IN} = -0.4 V, V_{OUT} = V_{EE} = -25 V, T_A = 70°C	—	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	V_{IN} = -0.4 V, I_{OUT} = -25 mA, Note 1	15	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = -4.6 V, I_{OUT} = -60 mA	—	1.1	V
		V_{IN} = -4.6 V, I_{OUT} = -120 mA	—	1.2	V
Input Current	$I_{IN(ON)}$	V_{IN} = -4.6 V, I_{OUT} = -120 mA	—	-1.6	mA
		V_{IN} = -14.6 V, I_{OUT} = -120 mA	—	-5.0	mA
Input Voltage	$V_{IN(ON)}$	I_{OUT} = -120 mA, V_{CE} ≤1.2 V, Note 3	—	-4.6	V
	$V_{IN(OFF)}$	I_{OUT} = -100 µA, T_A = 70°C	-0.4	—	V
Clamp Diode Leakage Current	I_R	V_R = 25 V, T_A = 70°C	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 120 mA	—	2.0	V
Input Capacitance	C_{IN}		—	25	pF
Turn-On Delay	t_{PHL}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs
Turn-Off Delay	t_{PLH}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs

NOTES: 1. Pulsed test, t_p ≤ 300 µs, duty cycle ≤ 2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
4. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

PARTIAL SCHEMATIC



Dwg. No. A-11,360



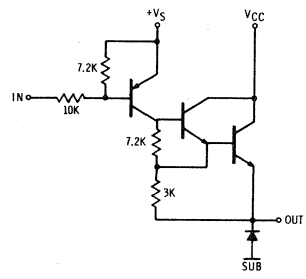
Dwg. No. A-11,359

UDN2588A AND UDN2588A-1
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 5.0 V, V_{CC} = 5.0 V, V_{EE} = -40 V (unless otherwise noted).

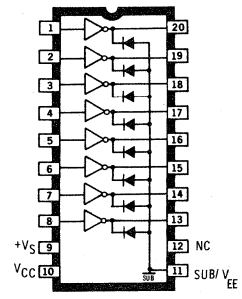
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UDN2588A	$V_{IN} \geq 4.5$ V, $V_{OUT} = V_{EE} = -45$ V	—	50	µA
			$V_{IN} \geq 4.6$ V, $V_{OUT} = V_{EE} = -45$ V, $T_A = 70$°C	—	100	µA
		UDN2588A-1	$V_{IN} \geq 4.5$ V, $V_{OUT} = V_{EE} = -75$ V	—	50	µA
			$V_{IN} \geq 4.6$ V, $V_{OUT} = V_{EE} = -75$ V, $T_A = 70$°C	—	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN2588A	$V_{IN} \geq 4.6$ V, $I_{OUT} = -25$ mA, Note 1	35	—	V
		UDN2588A-1	$V_{IN} \geq 4.6$ V, $V_{EE} = -70$ V, $I_{OUT} = -25$ mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Both	$V_{IN} = 2.6$ V, $I_{OUT} = -100$ mA, Ref. V_{CC}	—	1.8	V
			$V_{IN} = 2.0$ V, $I_{OUT} = -225$ mA, Ref. V_{CC}	—	1.9	V
			$V_{IN} = 1.4$ V, $I_{OUT} = -350$ mA, Ref. V_{CC}	—	2.0	V
Input Current	$I_{IN(ON)}$	Both	$V_{IN} = 1.4$ V, $I_{OUT} = -350$ mA	—	-500	µA
			$V_S = 15$ V, $V_{EE} = -30$ V, $V_{IN} = 0$ V, $I_{OUT} = -350$ mA	—	-2.1	mA
	$I_{IN(OFF)}$	Both	$I_{OUT} = -500$ µA, $T_A = 70$°C, Note 3	-50	—	µA
Input Voltage	$V_{IN(ON)}$	Both	$I_{OUT} = -100$ mA, $V_{CE} \leq 1.8$ V, Note 4	—	2.6	V
			$I_{OUT} = -225$ mA, $V_{CE} \leq 1.9$ V, Note 4	—	2.0	V
			$I_{OUT} = -350$ mA, $V_{CE} \leq 2.0$ V, Note 4	—	1.4	V
	$V_{IN(OFF)}$	Both	$I_{OUT} = -500$ µA, $T_A = 70$°C	4.8	—	V
Clamp Diode Leakage Current	I_R	UDN2588A	$V_R = 50$ V, $T_A = 70$°C	—	50	µA
		UDN2588A-1	$V_R = 80$ V, $T_A = 70$°C	—	50	µA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 350$ mA	—	2.0	V
Input Capacitance	C_{IN}	Both		—	25	pF
Turn-On Delay	t_{PHL}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs
Turn-Off Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs

NOTES:
1. Pulsed test, $t_p \leq 300$ µs, duty cycle ≤ 2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.
6. V_{CC} must be more positive than V_S.

PARTIAL SCHEMATIC

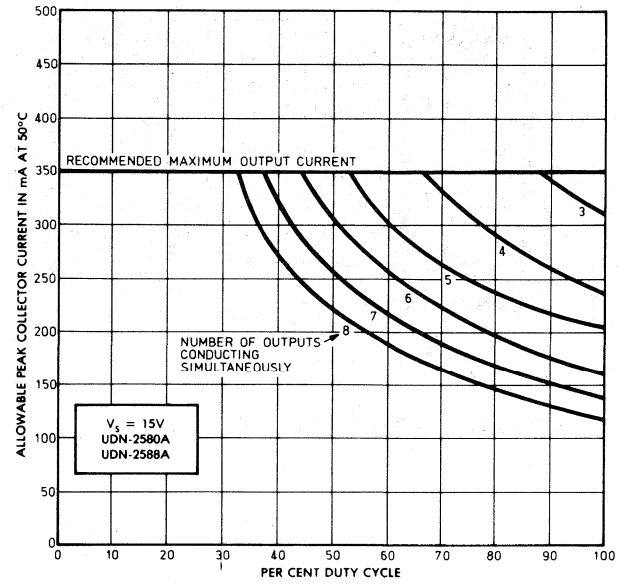


Dwg. No. A-11,361



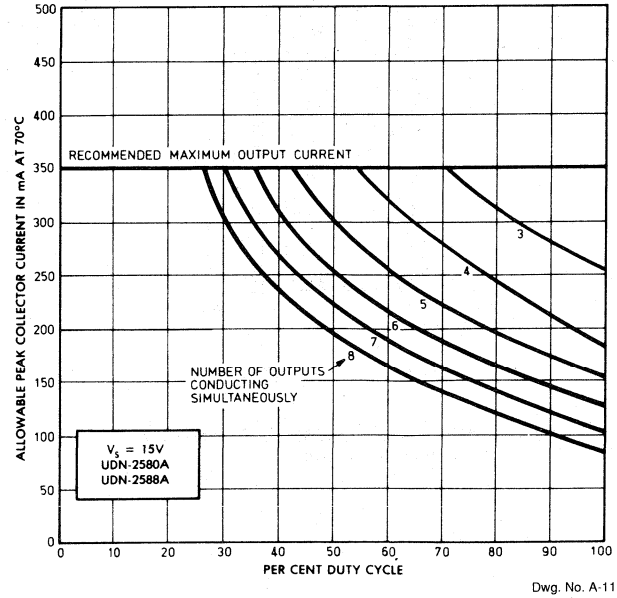
Dwg. No. A-11,357

ALLOWABLE PEAK COLLECTOR CURRENT AT 50°C AS A FUNCTION OF DUTY CYCLE



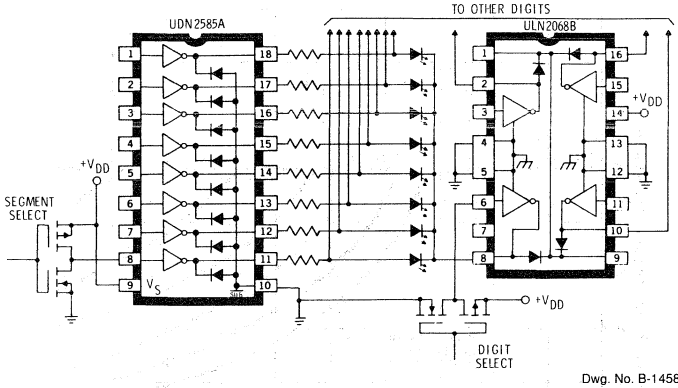
Dwg. No. A-11,107B

ALLOWABLE PEAK COLLECTOR CURRENT AT 70°C AS A FUNCTION OF DUTY CYCLE



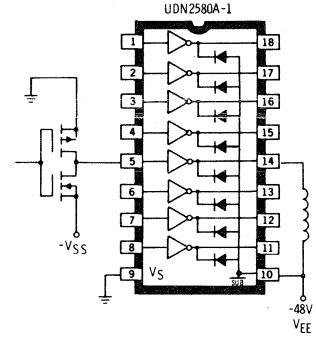
Dwg. No. A-11,108B

TYPICAL APPLICATIONS



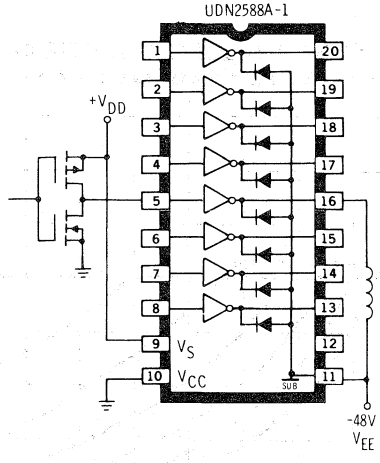
Dwg. No. B-1458A

COMMON-CATHODE LED DRIVER



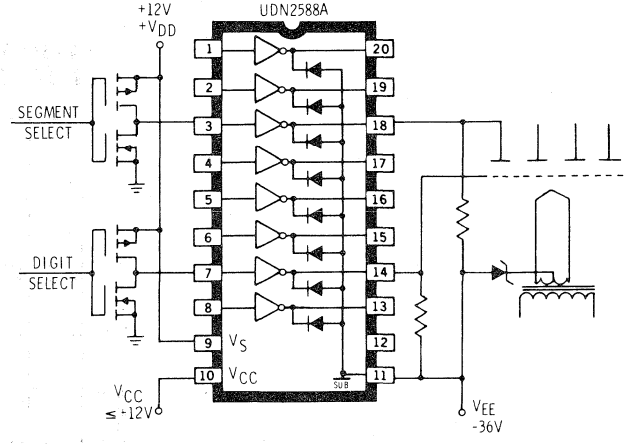
Dwg. No. A-11,356

TELECOMMUNICATIONS RELAY DRIVER
(Negative Logic)



Dwg. No. A-11,362

TELECOMMUNICATIONS RELAY DRIVER
(Positive Logic)



Dwg. No. A-11,363

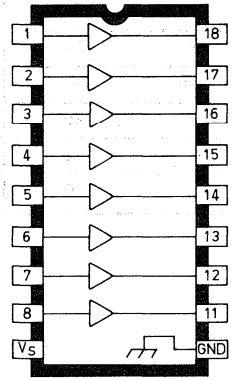
VACUUM-FLUORESCENT DISPLAY DRIVER
(Split Supply)

2595

8-CHANNEL SATURATED SINK DRIVERS

UDN2595LW

UDN2595A



Dwg. No. A-11,407

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature
for any one driver
(unless otherwise noted)

Output Voltage, V_{CE}
(UDN2595A/LW) . . . . . **20 V**
(UDN2595A-1) . . . . . **40 V**
Supply Voltage, V_S . . . . . **20 V**
Input Voltage, V_{IN} . . . . . **20 V**
Output Current, I_C . . . . . **200 mA**
Ground Terminal Current, I_{GND} . . . . . **1.6 A**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Note that the UDN2595A (dual in-line package) and UDN2595LW (small-outline IC package) are electrically identical and share a common pin number assignment.

Developed for use with low-voltage LED and incandescent displays requiring low output saturation voltage, the UDN2595A and UDN2595LW meet many interface needs, including those exceeding the capabilities of standard logic buffers. The eight non-Darlington outputs of each driver can continuously and simultaneously sink load currents of 100 mA at ambient temperatures of up to +75°C. Selected devices (UDN2595A-1) have maximum output ratings of 40 V and 200 mA per driver. In all other respects, it is identical to the 20 V UDN2595A.

The eight-channel driver's active-low inputs can be driven directly from TTL, Schottky TTL, DTL, 5 to 16 V CMOS, and NMOS logic. All input connections are on one side of the package, output connections on the other, for simplified printed wiring board layouts.

These drivers are packaged in plastic DIPs (suffix A) or surface-mountable wide-body SOICs (suffix LW), and are rated for operation over the temperature range of -20°C to +85°C. A hermetically sealed version for operation over the full military temperature range is also available.

FEATURES

- 200 mA Current Rating
- Low Saturation Voltage
- TTL, CMOS, NMOS Compatible
- Efficient Input/Output Pin Format
- DIP or SOIC Packaging

Always order by complete part number:

Part Number	Package
UDN2595A	18-Pin DIP
UDN2595LW	18-Lead Wide-Body SOIC

2595
8-CHANNEL SATURATED SINK DRIVERS

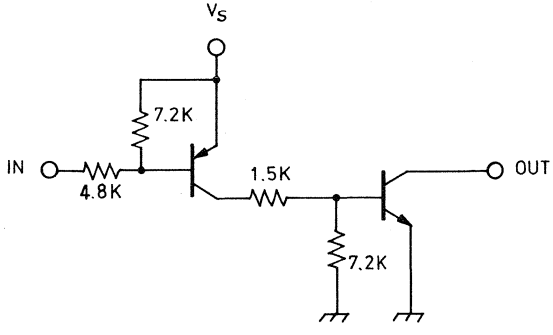
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{IN} \geq 4.5$ V, V_{OUT} = 20 V*, T_A = 25°C	—	50	µA
		$V_{IN} \geq 4.6$ V, V_{OUT} = 20 V*, T_A = 70°C	—	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = 0.4 V, I_{OUT} = 50 mA	—	0.5	V
		V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	0.6	V
Input Current	$I_{IN(ON)}$	V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	-1.6	mA
		V_{IN} = 0.4 V, I_{OUT} = 100 mA, V_S = 15 V	—	-5.0	mA
Input Voltage	$V_{IN(ON)}$	I_{OUT} = 100 mA, $V_{OUT} \leq$ 0.6 V	—	0.4	V
	$V_{IN(OFF)}$	I_{OUT} = 100 µA, T_A = 70°C	4.6	—	V
Input Capacitance	C_{IN}		—	25	pF
Supply Current	I_S	V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	6.0	mA
		V_{IN} = 0.4 V, I_{OUT} = 100 mA, V_S = 15 V	—	20	mA

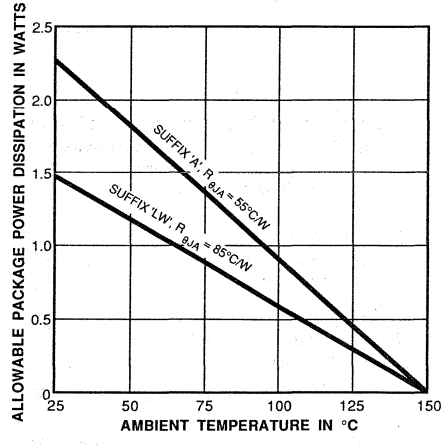
*V_{OUT} = 40 V for UDN2595A-1.

NOTES: 1. Negative current is defined as coming out of the specified device pin.
2. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified conditions.
3. I_S is measured with any one of eight drivers turned ON.

ONE OF EIGHT DRIVERS



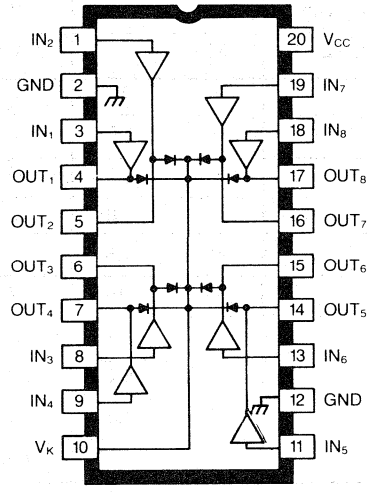
Dwg. No. A-11,408



Dwg. GP-018A

2596 AND 2597

8-CHANNEL SATURATED SINK DRIVERS



Dwg. No. W-100

ABSOLUTE MAXIMUM RATINGS at T_A = + 25°C

Output Voltage, V_{CE} ..... **50 V**
Output Current, I_{OUT}
(UDN2596A) ..... **500 mA**
(UDN2597A) ..... **1.0 A**
Supply Voltage, V_{CC} ..... **7.0 V**
Input Voltage, V_{IN} ..... **7.0 V**
Package Power Dissipation,
P_D ..... **2.27 W***
Operating Temperature Range,
T_A ..... **-20°C to + 85°C**
Storage Temperature Range,
T_S ..... **-65°C to + 150°C**

*Derate at the rate of 18.2 mW/°C above T_A = 25°C

Low output saturation voltages at high load currents are provided by UDN2596A and UDN2597A sink driver ICs. These devices can be used as interface buffers between standard low-power digital logic (particularly MOS) and high-power loads such as relays, solenoids, stepping motors, and LED or incandescent displays. The eight saturated sink drivers in each device feature high-voltage, high-current open-collector outputs. Transient suppression clamp diodes and a minimum 35 V output sustaining voltage allow their use with many inductive loads.

The saturated (non-Darlington) NPN outputs provide low collector-emitter voltage drops as well as improved turn-off times due to an active pull-down function within the output predrive section. The UDN2596A is for use with output loads to 500 mA while the UDN2597A is for use with loads to 1 A. Adjacent outputs may be paralleled for higher load currents.

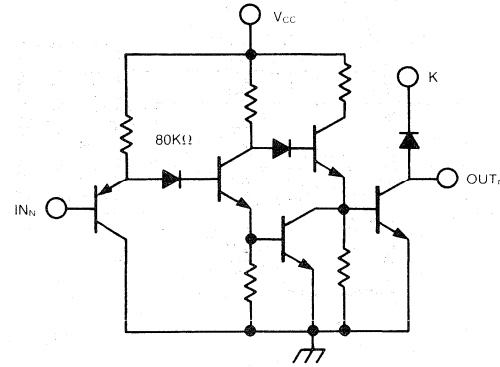
Inputs require very low input current and are activated by a low logic level consistent with the much greater sinking capability associated with NMOS, CMOS, and TTL logic. The UDN2596A and UDN2597A are rated for use with 5 V logic levels.

Both devices are furnished in 20-pin DIP packages with copper leadframes for improved thermal characteristics.

FEATURES

- Low Output ON Voltages
- Up to 1.0 A Sink Capability
- 50 V Min. Output Breakdown
- Output Transient-Suppression Diodes
- Output Pull-Down for Fast Turn-Off
- TTL, CMOS Compatible Inputs

ONE OF EIGHT DRIVERS

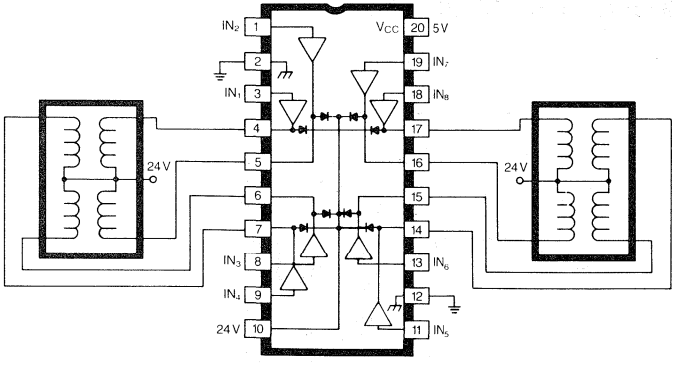


Dwg. No. W-101

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{CC} = 5.0 V

Characteristics	Symbol	Applicable Devices	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	Both	V_{OUT} = 50 V, V_{IN} = 2.4 V	—	10	µA
Output Sustaining Voltage	$V_{CE(sus)}$	UDN2596A	I_{OUT} = 300 mA, L = 2 mH	35	—	V
		UDN2597A	I_{OUT} = 750 mA, L = 2 mH	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	UDN2596A	I_{OUT} = 300 mA	—	0.5	V
		UDN2597A	I_{OUT} = 750 mA	—	1.0	V
Clamp Diode Leakage Current	I_R	Both	V_R = 50 V	—	10	µA
Clamp Diode Forward Voltage	V_F	UDN2596A	I_F = 300 mA	—	1.8	V
		UDN2597A	I_F = 750 mA	—	1.8	V
Logic Input Current	$I_{IN(0)}$	Both	V_{IN} = 0.8 V	—	-15	µA
	$I_{IN(1)}$	Both	V_{IN} = 2.4 V	—	10	µA
Supply Current (per driver)	$i_{CC(ON)}$	UDN2596A	V_{IN} = 0.8 V	—	6.0	mA
		UDN2597A	V_{IN} = 0.8 V	—	22	mA
	$I_{CC(OFF)}$	Both	V_{IN} = 2.4 V	—	1.3	mA
Turn-On Delay	t_{pd0}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	3.0	µs
Turn-Off Delay	t_{pd1}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	2.0	µs

TYPICAL APPLICATION
DUAL STEPPER MOTOR DRIVE



Dwg. No. W-102A

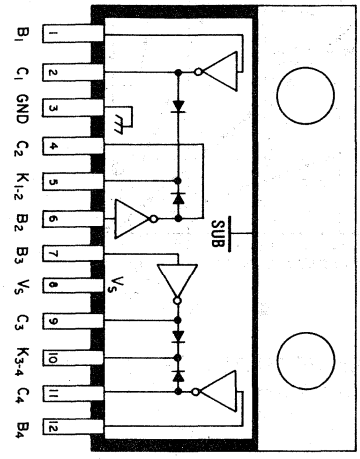
RECOMMENDED OPERATING CONDITIONS

Type Number	Logic	I_{OUT}
UDN2596A	5.0 V	300 mA
UDN2597A	5.0 V	750 mA

Note: Pins 2 and 12 must both be connected to power ground.

2878 AND 2879

QUAD HIGH-CURRENT DARLINGTON SWITCHES



Dwg. No. A-11,974

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for any driver (unless otherwise noted)

Output Voltage, V_{CEX}
(UDN2878W & UDN2878W-2) . . . . . **50 V**
(UDN2879W & UDN2879W-2) . . . . . **80 V**
Output Current, I_C
(UDN2878W & UDN2879W) . . . . . **5.0 A**
(UDN2878W-2 & UDN2979W-2) . . . . . **4.0 A**
Input Voltage, V_{IN} . . . . . **15 V**
Input Current, I_{IN} . . . . . **25 mA**
Supply Voltage, V_S . . . . . **10 V**
Total Package Power Dissipation, P_D . . . . . **See Graph**
Operating Ambient Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

These quad Darlington arrays are designed to serve as interface between low-level logic and peripheral power devices such as solenoids, motors, incandescent displays, heaters, and similar loads of up to 320 W per channel. Both integrated circuits include transient-suppression diodes that enable use with inductive loads. The input logic is compatible with most TTL, DTL, LSTTL, and 5 V CMOS logic.

Type UDN2878W and UDN2879W 4 A arrays are identical except for output-voltage ratings. The former is rated for operation to 50 V (35 V sustaining), while the latter has a minimum output breakdown rating of 80 V (50 V sustaining). The economical UDN2878W-2 and UDN2879W-2 are recommended for applications requiring load currents of 3 A or less. These less expensive devices are identical to the basic parts except for the maximum allowable load-current rating.

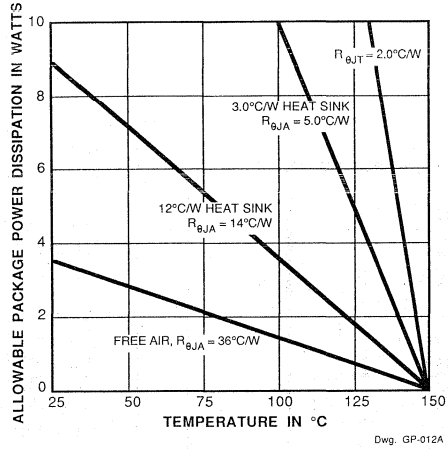
For maximum power-handling capability, all drivers are supplied in a 12-pin single in-line power-tab package. The tab needs no insulation. External heat sinks are usually required for proper operation of these devices.

FEATURES

- Output Currents to 4 A
- Output Voltages to 80 V
- Loads to 1280 W
- TTL, DTL, or CMOS Compatible Inputs
- Internal Clamp Diodes
- Plastic Single In-Line Package
- Heat-Sink Tab

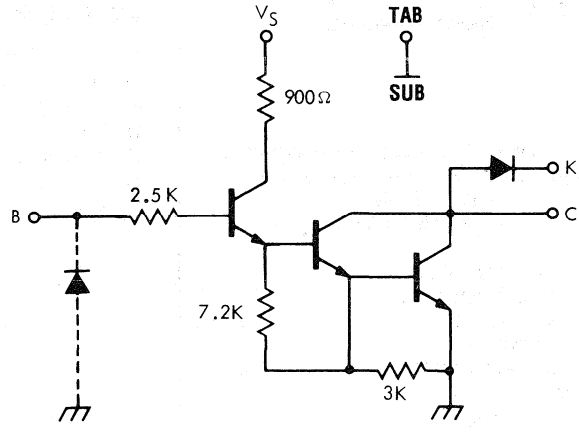
Always order by complete part number:

Part Numbers	Max. I_C	Max. V_{CEX}
UDN2878W	5.0 A	50 V
UDN2878W-2	4.0 A	50 V
UDN2879W	5.0 A	80 V
UDN2879W-2	4.0 A	80 V



Dwg. GP-012A

PARTIAL SCHEMATIC
One of 4 Drivers



Dwg. No. A-12,037

NOTE: Pin 3 must be connected to ground for proper operation.

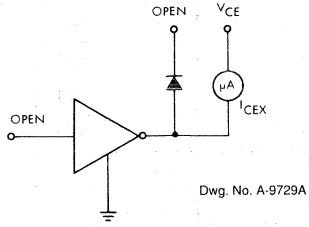
Device	Output Voltage	Sustaining Voltage	Output Current
UDN2878W	50 V	35 V	4 A
UDN2878W-2	50 V	35 V	3 A
UDN2879W	80 V	50 V	4 A
UDN2879W-2	80 V	50 V	3 A

ELECTRICAL CHARACTERISTICS at V_S = 5.0 V, T_A = +25°C (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	UDN2878W/W-2	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = +70°C	—	500	µA
			UDN2879W/W-2	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = +70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(sus)}$	—	UDN2878W	I_C = 4 A, L = 10 mH	35	—	V
			UDN2878W-2	I_C = 3 A, L = 10 mH	35	—	V
			UDN2879W	I_C = 4 A, L = 10 mH	50	—	V
			UDN2879W-2	I_C = 3 A, L = 10 mH	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 500 mA, V_{IN} = 2.75 V	—	1.1	V
				I_C = 1.0 A, V_{IN} = 2.75 V	—	1.3	V
				I_C = 2.0 A, V_{IN} = 2.75 V	—	1.5	V
				I_C = 3.0 A, V_{IN} = 2.75 V	—	1.9	V
			UDN2878/79W	I_C = 4.0 A, V_{IN} = 2.75 V	—	2.4	V
Input Current	I_{IN}	3	All	V_{IN} = 2.75 V	—	550	µA
				V_{IN} = 3.75 V	—	1000	µA
Input Voltage	$V_{IN(ON)}$	4	All	V_{CE} = 2.2 V, I_C = 3.0 A	—	2.75	V
			UDN2878/79W	V_{CE} = 2.2 V, I_C = 4.0 A	—	2.75	V
Supply Current per Driver	I_S	7	All	I_C = 500 mA, V_{IN} = 2.75 V	—	6.0	mA
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}, I_C = 3.0 A	—	1.5	µs
Clamp Diode Leakage Current	I_R	5	All	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = +70°C	—	100	µA
			UDN2879W/W-2	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = +70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	6	All	I_F = 3.0 A	—	2.5	V
			UDN2878/79W	I_F = 4.0 A	—	3.0	V

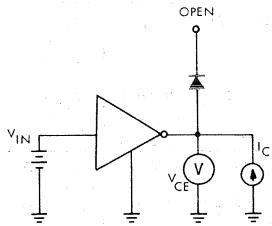
Caution: High-current tests are pulse tests or require heat sinking.

TEST FIGURES



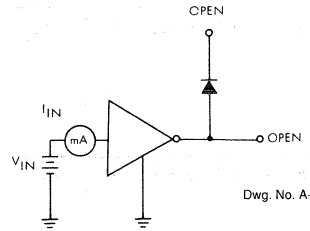
Dwg. No. A-9729A

FIGURE 1



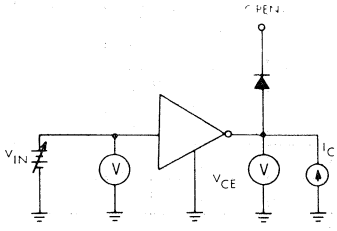
Dwg. No. A-10,350

FIGURE 2



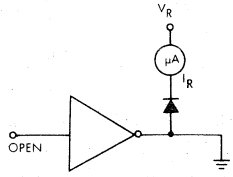
Dwg. No. A-9732

FIGURE 3



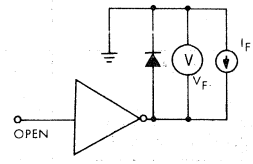
Dwg. No. A-9734A

FIGURE 4



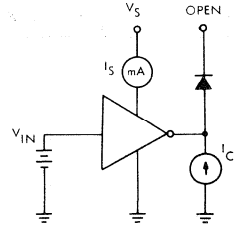
Dwg. No. A-9735A

FIGURE 5



Dwg. No. A-9736

FIGURE 6



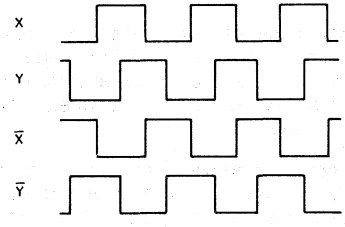
Dwg. No. A-10,351

FIGURE 7

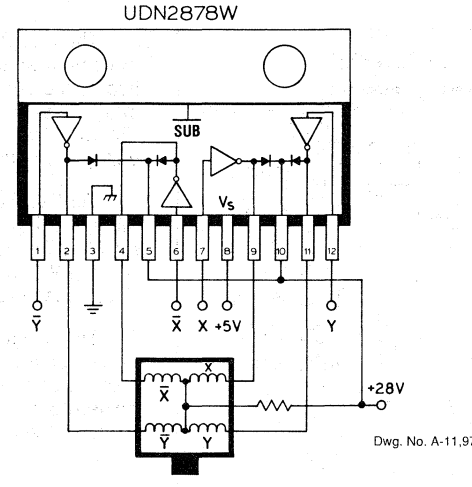
TYPICAL APPLICATIONS

STEPPER-MOTOR DRIVER

INPUT WAVEFORMS

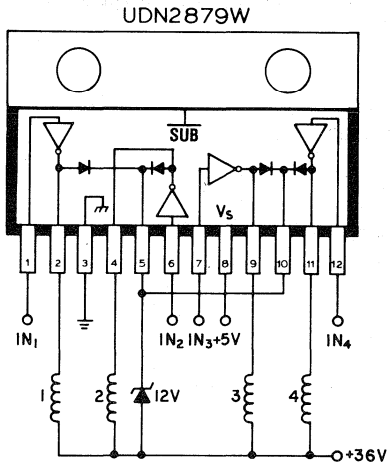


Dwg. No. A-11,795



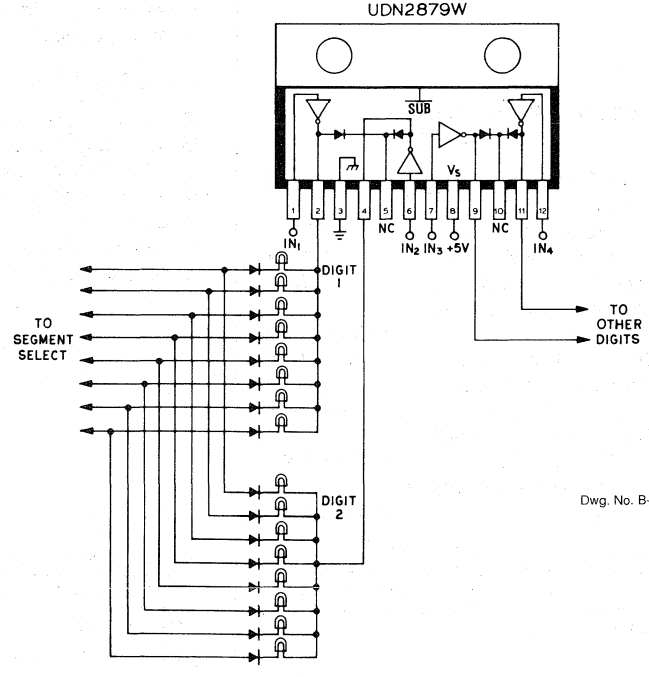
Dwg. No. A-11,975

PRINT-HAMMER DRIVER



Dwg. No. A-11,976

DIGIT DRIVER FOR MULTIPLEXED INCANDESCENT LAMP DISPLAY

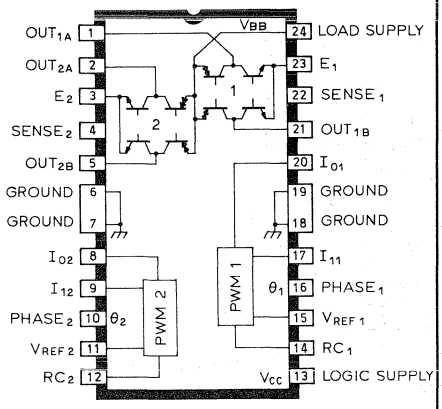


Dwg. No. B-1512

2916

DUAL FULL-BRIDGE PWM MOTOR DRIVERS

UDN2916B



Dwg. PP-005

ABSOLUTE MAXIMUM RATINGS at $T_J \leq 150°C$

Motor Supply Voltage, V_{BB} . . . . . **45 V**
Output Current, I_{OUT}
(Peak, $t_w \leq 20$ µs) . . . . . **±1.0 A**
(Continuous) . . . . . **±750 mA**
Logic Supply Voltage, V_{CC} . . . . . **7.0 V**
Logic Input Voltage Range,
V_{IN} . . . . . **-0.3 V to +7.0 V**
Output Emitter Voltage, V_E . . . . . **1.5 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The UDN2916B and UDN2916EB motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output saturation voltage drop (less than 1.8 V total source plus sink at 500 mA).

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0, 33, 67, or 100% of the maximum level. A phase input to each bridge determines load current direction.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

The UDN2916B is supplied in a 24-pin dual in-line plastic batwing package with a copper lead-frame and heat sinkable tabs for improved power dissipation capabilities. The UDN2916EB is supplied in a 44-lead power PLCC for surface mount applications. Its batwing construction provides for maximum package power dissipation in the smallest possible construction.

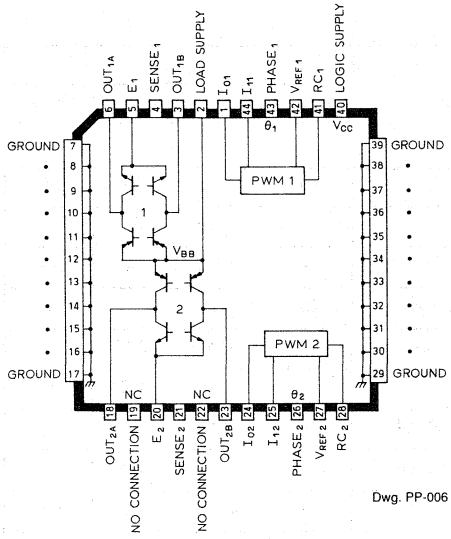
FEATURES

- 750 mA Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Internal PWM Current Control
- Low Output Saturation Voltage
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3717, UC3770

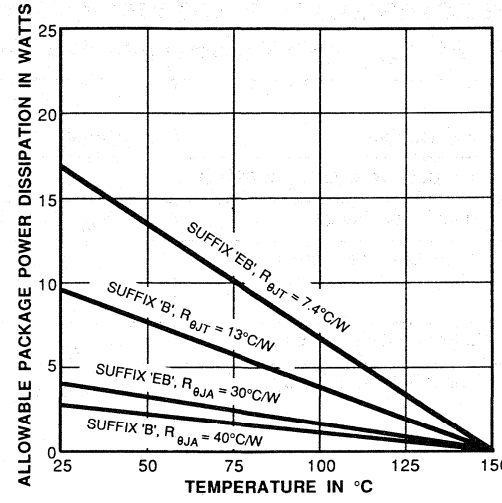
Always order by complete part number:

Part Number	Package
UDN2916B	14-Pin DIP
UDN2916EB	44-Lead PLCC

UDN2916EB

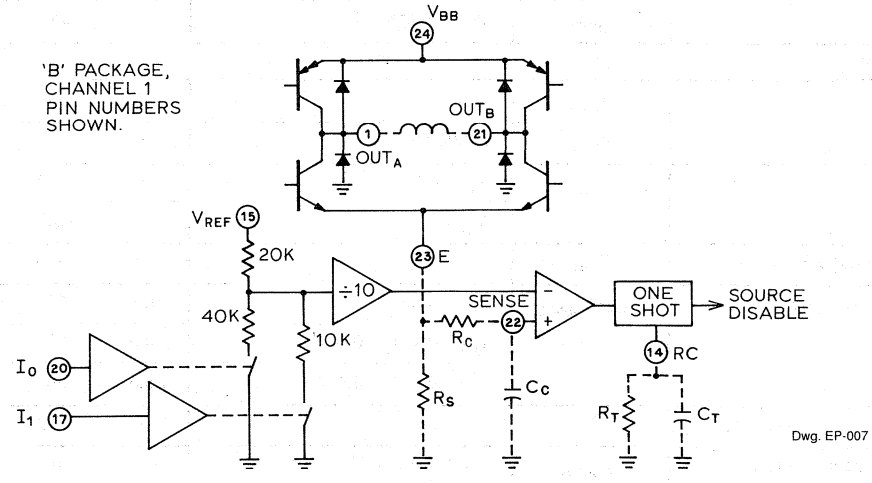


Dwg. PP-006



Dwg. GP-005A

PWM CURRENT-CONTROL CIRCUITRY



Dwg. EP-007

TRUTH TABLE

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ 150°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, V_{REF} = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers (OUT_A or OUT_B)						
MotorSupply Range	V_{BB}		10	—	45	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	< 1.0	50	µA
		$V_{OUT} = 0$	—	<-1.0	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±750 mA, L = 3.0 mH	45	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Sink Driver, I_{OUT} = +500 mA	—	0.4	0.6	V
		Sink Driver, I_{OUT} = +750 mA	—	1.0	1.2	V
		Source Driver, I_{OUT} = -500 mA	—	1.0	1.2	V
		Source Driver, I_{OUT} = -750 mA	—	1.3	1.5	V
Clamp Diode Leakage Current	I_R	V_R = 45 V	—	< 1.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 750 mA	—	1.6	2.0	V
Driver Supply Current	$I_{BB(ON)}$	Both Bridges ON, No Load	—	20	25	mA
	$I_{BB(OFF)}$	Both Bridges OFF	—	5.0	10	mA
Control Logic						
Input Voltage	$V_{IN(1)}$	All inputs	2.4	—	—	V
	$V_{IN(0)}$	All inputs	—	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
		V_{IN} = 0.8 V	—	- 3.0	-200	µA
Reference Voltage Range	V_{REF}	Operating	1.5	—	7.5	V
Current Limit Threshold (at trip point)	V_{REF}/V_{SENSE}	$I_0 = I_1$ = 0.8 V	9.5	10	10.5	—
		I_0 = 2.4 V, I_1 = 0.8 V	13.5	15	16.5	—
		I_0 = 0.8 V, I_1 = 2.4 V	25.5	30	34.5	—
Thermal Shutdown Temperature	T_J		—	170	—	°C
Total Logic Supply Current	$I_{CC(ON)}$	$I_0 = I_1$ = 8.0 V, No Load	—	40	50	mA
	$I_{CC(OFF)}$	$I_0 = I_1$ = 2.4 V, No Load	—	10	12	mA

APPLICATIONS INFORMATION

PWM CURRENT CONTROL:

The UDN2916B/EB dual bridges are designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor (R_S), internal comparator, and monostable multivibrator.

When the bridge is turned ON, current increases in the motor winding and it is sensed by the external sense resistor until the sense voltage (V_{SENSE}) reaches the level set at the comparator's input:

$$I_{TRIP} = V_{REF}/10\ R_S$$

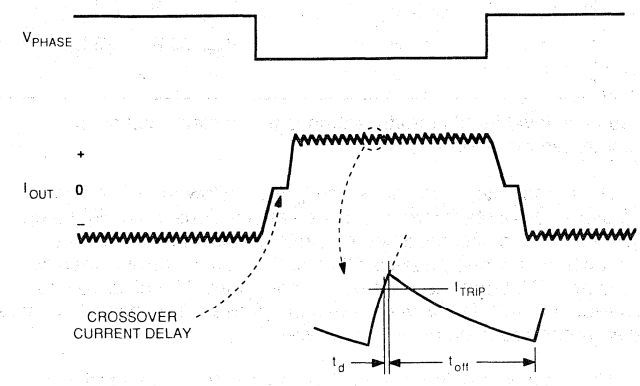
The comparator then triggers the monostable which turns OFF the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 µs. After turn-off, the motor current decays, circulating through the ground-clamp diode and sink transistor. The source driver's OFF time (and therefore the magnitude of the current decrease) is determined by the monostable's external RC timing components, where $t_{off} = R_TC_T$ within the range of 20 kΩ to 100 kΩ and 100 pF to 1,000 pF.

When the source driver is re-enabled, the winding current (the sense voltage) is again allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

Special circuitry has been included to prevent runaway current control when the fixed OFF time (t_{off}) is set too short. This circuitry prevents the source driver from being re-enabled until the load current has decayed to below the I_{TRIP} level.

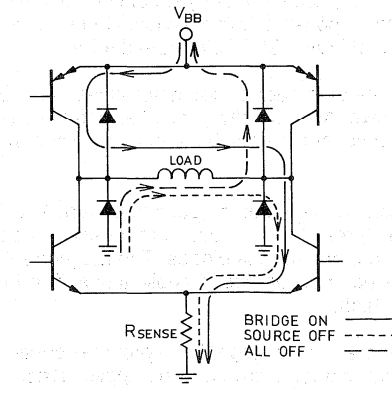
Loads with high distributed capacitances may result in high turn-ON current peaks. This peak (appearing across R_S) will attempt to trip the comparator, resulting in erroneous current control or high-frequency oscillations. An internal low-pass filter is used to reduce this undesirable effect for turn-ON spikes of less than 1.5 µs. An external R_CC_C time delay can be used to further delay the action of the comparator. Depending on load type, many applications will not require these external components (SENSE connected to E).

PWM OUTPUT CURRENT WAVE FORM



Dwg. WM-003-1

LOAD CURRENT PATHS



Dwg. EP-006-1

LOGIC CONTROL OF OUTPUT CURRENT:

Two logic level inputs (I_0 and I_1) allow digital selection of the motor winding current at 100%, 67%, 33%, or 0% of the maximum level per the table. The 0% output current condition turns OFF all drivers in the bridge and can be used as an OUTPUT ENABLE function.

CURRENT-CONTROL TRUTH TABLE

I_0	I_1	Output Current
L	L	$V_{REF}/10\ R_S = I_{TRIP}$
H	L	$V_{REF}/15\ R_S = 2/3\ I_{TRIP}$
L	H	$V_{REF}/30\ R_S = 1/3\ I_{TRIP}$
H	H	0

These logic level inputs greatly enhance the implementation of μP-controlled drive formats.

During half-step operations, the I_0 and I_1 allow the μP to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 100% drive current when only one phase is ON and 67% drive current when two phases are ON. Logic highs on both I_0 and I_1 turn OFF all drivers to allow rapid current decay when switching phases. This helps to ensure proper motor operation at high step rates.

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for 'hold' conditions and/or increased current (and available torque) for start-up conditions.

GENERAL:

To avoid excessive voltage spikes on the LOAD SUPPLY pin (V_{BB}), a large-value capacitor (≥22 μF) should be connected from V_{BB} to ground as close as possible to the device. Under no circumstances should the voltage at LOAD SUPPLY exceed 45 V.

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime (approximately 2 μs) prevents crossover currents that can occur when switching the PHASE input.

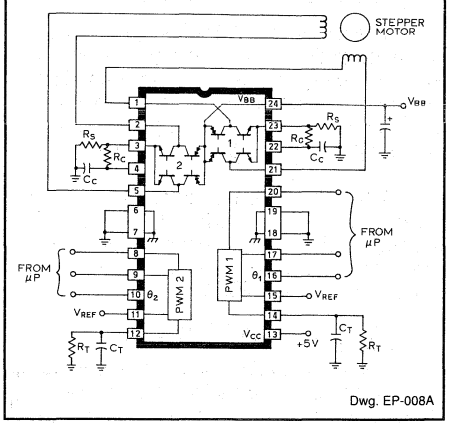
All four drivers in the bridge output can be turned OFF between steps ($I_0 = I_1 \geq 2.4$ V) resulting in a fast current decay through the internal output clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. The PHASE, I_0, and I_1 inputs float high.

Varying the reference voltage (V_{REF}) provides continuous control of the peak load current for micro-stepping applications.

Thermal protection circuitry turns OFF all drivers when the junction temperature reaches +170°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +145°C.

The UDN2916B/EB output drivers are optimized for low output saturation voltages—less than 1.8 V total (source plus sink) at 500 mA. Under normal operating conditions, when combined with the excellent thermal properties of the batwing package design, this allows continuous operation of both bridges simultaneously at 500 mA.

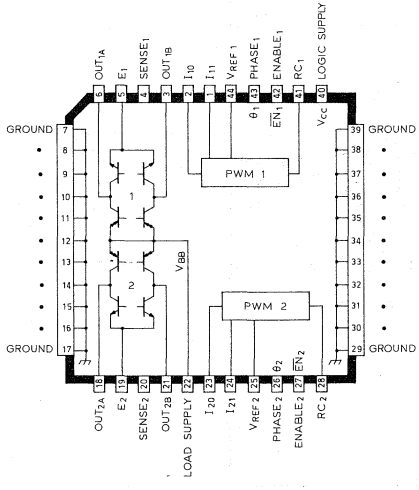
TYPICAL APPLICATION



Dwg. EP-008A

2917

DUAL FULL-BRIDGE PWM MOTOR DRIVER



Dwg. PP-021

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Motor Supply Voltage, V_{BB} . . . . . **45 V**
Output Current, I_{OUT} ($t_w \leq 20\ \mu s$) . . . **±1.75 A**
(Continuous) . . . . . **±1.5 A**
Logic Supply Voltage, V_{CC} . . . . . **7.0 V**
Logic Input Voltage Range,
V_{IN} . . . . . **-0.3 V to +7.0 V**
Output Emitter Voltage, V_E . . . . . **1.5 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The UDN2917EB motor driver is designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 1.5 A.

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0, 33%, 67%, or 100% of the maximum level. A PHASE input to each bridge determines load current direction. Active-low ENABLE inputs control the four drivers in each bridge.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

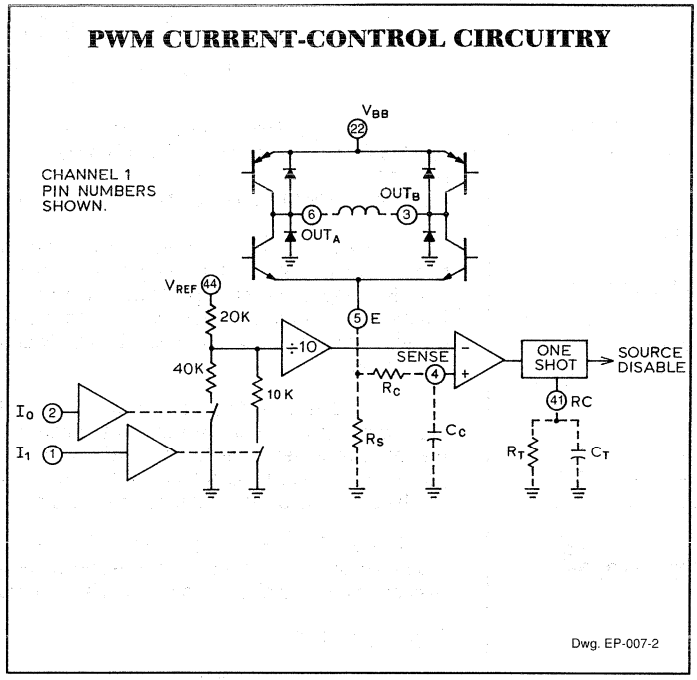
The UDN2917EB is supplied in a 44-lead power PLCC for surface-mount applications. Its batwing construction provides for maximum package power dissipation in the smallest possible construction.

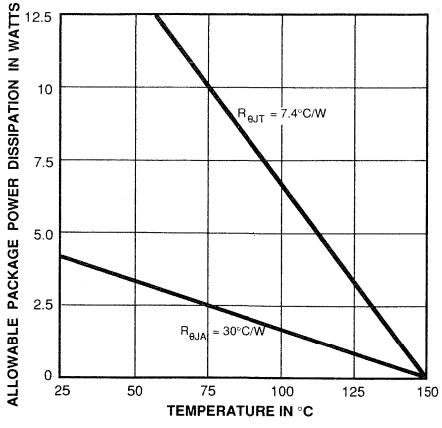
FEATURES

- 1.5 A Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Digital Control of Output Current
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3770

Always order by complete part number: **UDN2917EB** .

PWM CURRENT-CONTROL CIRCUITRY





Dwg. GP-020A

TRUTH TABLE

Enable	Phase	Out_A	Out_B
L	H	H	L
L	L	L	H
H	X	Z	Z

X = Don't care
Z = High impedance

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, V_{REF} = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Drivers (OUT_A or OUT_B)						
Motor Supply Range	V_{BB}		10	—	45	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	<1.0	50	µA
		$V_{OUT} = 0$	—	<-1.0	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±1.5 A, L = 3.5 mH	45	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Sink Driver, I_{OUT} = +1.0 A	—	0.5	0.7	V
		Sink Driver, I_{OUT} = +1.5 A	—	0.8	1.0	V
		Source Driver, I_{OUT} = -1.0 A	—	1.8	1.9	V
		Source Driver, I_{OUT} = -1.5 A	—	1.9	2.1	V
Clamp Diode Leakage Current	I_R	V_R = 45 V	—	<1.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 1.5 A	—	1.6	2.0	V
Driver Supply Current	$I_{BB(ON)}$	Both Bridges ON, No Load	—	9.0	12	mA
	$I_{BB(OFF)}$	Both Bridges OFF	—	4.0	6.0	mA
Control Logic						
Input Voltage	$V_{IN(1)}$	All Inputs	2.4	—	—	V
	$V_{IN(0)}$	All Inputs	—	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-3.0	-200	µA
Reference Voltage Range	V_{REF}	Operating	1.5	—	7.5	V
Current Limit Threshold (at trip point)	V_{REF}/V_{SENSE}	$I_0 = I_1$ = 0.8 V	9.5	10	10.5	—
		I_0 = 2.4 V, I_1 = 0.8 V	13.5	15	16.5	—
		I_0 = 0.8 V, I_1 = 2.4 V	25.5	30	34.5	—
Thermal Shutdown Temp.	T_J		—	170	—	°C
Total Logic Supply Current	$I_{CC(ON)}$	$I_0 = I_1 = V_{EN}$ = 0.8 V, No Load	—	90	105	mA
	$I_{CC(OFF)}$	$I_0 = I_1$ = 2.4 V, No Load	—	10	12	mA

Negative current is defined as coming out of (sourcing) the specified device pin.
Typical Data is for design information only.

APPLICATIONS INFORMATION

PWM CURRENT CONTROL:

The UDN2917EB dual bridge is designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor (R_S), internal comparator, and monostable multivibrator.

When the bridge is turned ON, current increases in the motor winding and it is sensed by the external sense resistor until the sense voltage (V_{SENSE}) reaches the level set at the comparator's input:

$$I_{TRIP} = V_{REF}/10\ R_S$$

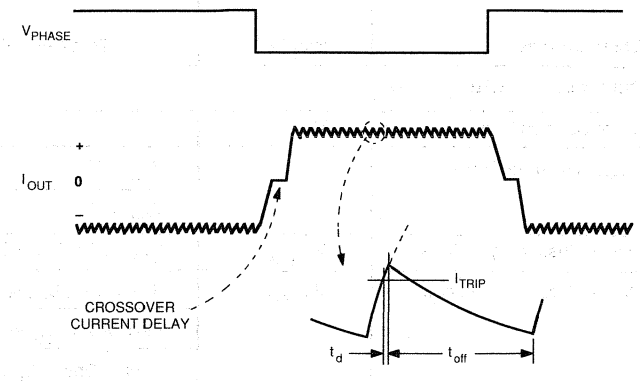
The comparator then triggers the monostable which turns OFF the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 µs. After turn-off, the motor current decays, circulating through the ground clamp diode and sink transistor. The source driver's OFF time (and therefore the magnitude of the current decrease) is determined by the monostable's external RC timing components, where $t_{off} = R_TC_T$ within the range of 20 kΩ to 100 kΩ and 200 pF to 500 pF.

When the source driver is re-enabled, the winding current (the sense voltage) is again allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

Special circuitry has been included to prevent runaway current control when the fixed OFF time (t_{off}) is set too short. This circuitry prevents the source driver from being re-enabled until the load current has decayed to below the I_{TRIP} level.

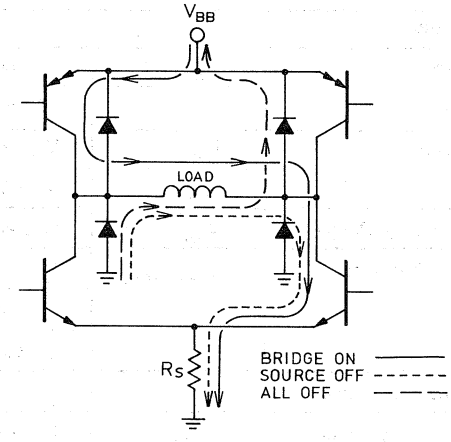
Loads with high distributed capacitances may result in high turn-ON current peaks. This peak (appearing across R_S) will attempt to trip the comparator, resulting in erroneous current control or high-frequency oscillations. An external R_CC_C low-pass filter may be needed to delay the action of the comparator.

PWM OUTPUT CURRENT WAVEFORM



Dwg. WM-003-1

LOAD CURRENT PATHS



Dwg. EP-006-1

CURRENT-CONTROL TRUTH TABLE

I_0	I_1	Output Current
L	L	$V_{REF}/10\ R_S = I_{TRIP}$
H	L	$V_{REF}/15\ R_S = 2/3\ I_{TRIP}$
L	H	$V_{REF}/30\ R_S = 1/3\ I_{TRIP}$
H	H	0

LOGIC CONTROL OF OUTPUT CURRENT:

Two logic level inputs (I_0 and I_1) allow digital selection of the motor winding current at 100%, 67%, 33%, or 0% of the maximum level per the table. The 0% output current condition turns OFF all drivers in the bridge and can be used as an output enable function. These logic level inputs greatly enhance the implementation of µP-controlled drive formats.

During half-step operations, the I_0 and I_1 inputs allow the µP to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 100% drive current when only one phase is ON and 67% drive current when two phases are ON.

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for 'hold' conditions and/or increased current (and available torque) for start-up conditions.

GENERAL:

To avoid excessive voltage spikes on the LOAD SUPPLY pin (V_{BB}), a large-value capacitor (≥47 µF) should be connected from V_{BB} to ground as close as possible to the device. Under no circumstances should the voltage at LOAD SUPPLY exceed 45 V.

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime (approximately 2 µs) prevents crossover currents that can occur when switching the PHASE input.

All four drivers in the bridge output can be turned OFF ($V_{EN} \geq 2.4$ V or $I_0 = I_1 \geq 2.4$ V), resulting in a fast current decay through the internal output clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. All logic inputs float high; the ENABLE input must be tied low if it is not used.

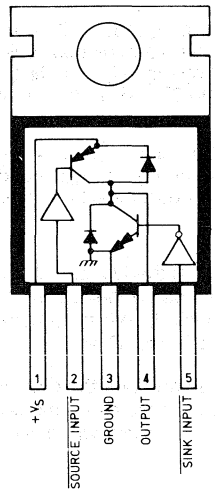
Varying the reference voltage (V_{REF}) provides continuous control of the peak load current for micro-stepping applications.

Thermal protection circuitry turns OFF all drivers when the junction temperature reaches +170°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +145°C.

2935 AND 2950

BIPOLAR HALF-BRIDGE MOTOR DRIVERS

UDN2935Z



Dwg. No. A-12,116

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range,
V_S . . . . . **8.0 V to 35 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to +7.0 V**
Peak Output Current (100 ms, 10% d-c),
I_{OP} . . . . . **±3.5 A**
Continuous Output Current,
I_{OUT} . . . . . **±2.0 A**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Both Type UDN2935Z and UDN2950Z integrated circuits are designed for servo-motor applications using pulse-width modulation. These two high-current, monolithic half-bridge motor drivers combine a sink-and-source driver with diode transient protection, input gain, level shifting, logic stages, and a voltage regulator for single-supply operation.

The UDN2935Z output goes high with an active low input at pin 2; it is especially desirable in NMOS microprocessor applications. The UDN2950Z output goes high with an active high input at pin 2; its inputs can be tied together for single-wire control. The input circuitry of both devices is compatible with TTL and low-voltage CMOS, PMOS, and NMOS logic. Both ICs have logic lockout (tri-state output) that prevents source and sink drivers from turning ON simultaneously.

In typical applications, the chopper-drive mode is characterized by low power-dissipation levels, low saturation voltages, and short chopper-storage times for the sink drivers. The motor drivers can be used in pairs for full-bridge operation, or as triplets in three-phase brushless d-c motor-drive applications. They can also be teamed with stepper motor translator/drivers for bipolar d-c stepper motor control.

The motor drivers' single-chip construction and power-tab TO-220 package enable cost-effective and reliable system designs supported by excellent power-dissipation ratings, minimum size, and ease of installation; because the package's heat tab is at ground potential, several devices can share a common heat sink without insulating hardware.

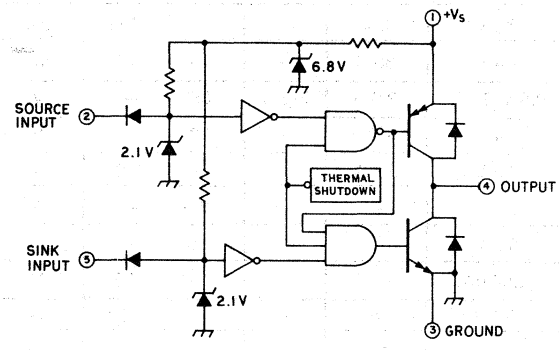
FEATURES

- 3.5 A Peak Output
- 37 V Minimum Output Breakdown
- Output Transient Protection
- Tri-State Outputs
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- Internal Thermal Shutdown
- High-Speed Chopper (to 100 kHz)
- UDN2935Z Replaces SG3635P
- UDN2950Z Replaces UDN2949Z, SN75605
- TO-220 Style Packages

Always order by complete part number, e.g., **UDN2935Z**.
See Truth Table.

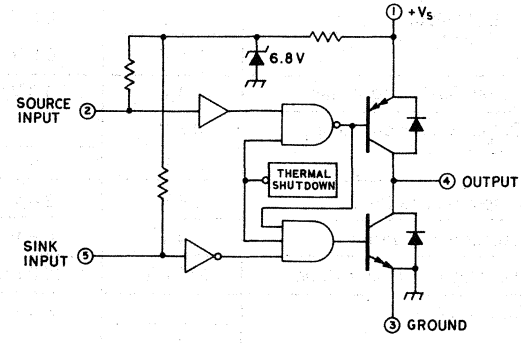
FUNCTIONAL BLOCK DIAGRAMS

UDN2935Z



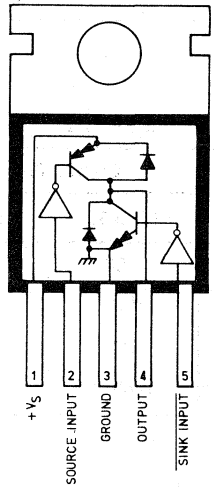
Dwg. No. A-12,113

UDN2950Z

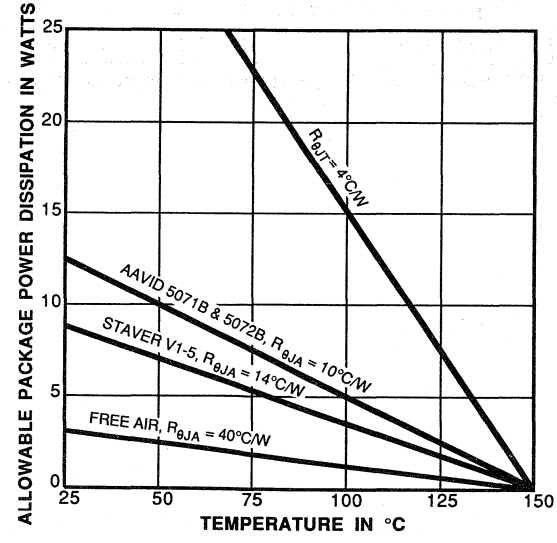


Dwg. No. 12,112

UDN2950Z



Dwg. No. A-11,177



Dwg. GP-014

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_S = 35 V (unless otherwise noted).

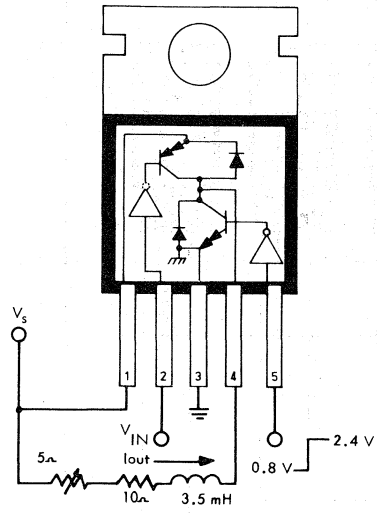
Characteristic	Source Driver Input, Pin 2		Sink Driver Input, Pin 5	Output, Pin 4	Other	Limits		
	UDN2935Z	UDN2950Z				Min.	Max.	Units
Output Leakage Current	2.4 V	0.8 V	2.4 V	0 V	—	—	-500	µA
	2.4 V	0.8 V	2.4 V	35 V	—	—	500	µA
Output Sustaining Voltage	2.4 V	0.8 V	0.8 to 2.4 V	2.0 A	Fig. 1	35	—	V
Output Saturation Voltage	0.8 V	2.4 V	2.4 V	-2.0 A	—	33	—	V
	2.4 V	0.8 V	0.8 V	2.0 A	—	—	2.0	V
Output Source Current	0.8 V	2.4 V	2.4 V	—	—	-2.0	—	A
Output Sink Current	2.4 V	0.8 V	0.8 V	—	—	2.0	—	A
Input Open-Circuit Voltage	-250 µA	-250 µA	-250 µA	—	—	—	7.5	V
Input Current	—	2.4 V	2.4 V	NC	—	—	-700	µA
	2.4 V	—	2.4 V	NC	—	—	10	µA
	0.8 V	0.8 V	0.8 V	NC	—	—	-1.6	mA
Propagation Delay	2.4 V	0.8 V	0.8 to 2.4 V	2.0 A	—	—	750	ns
	0.8 to 2.4 V	2.4 to 0.8 V	2.4 V	2.0 A	—	—	2.0	µs
Clamp Diode Forward Voltage	NC	NC	NC	2.0 A	Fig. 2	—	2.2	V
Supply Current	0.8 V	2.4 V	NC	NC	—	—	35	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TRUTH TABLE

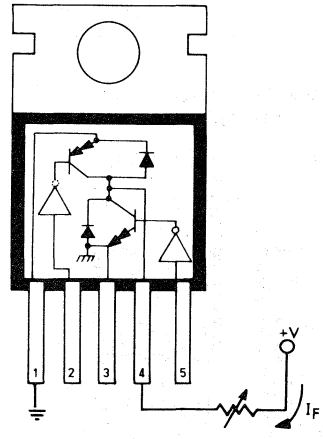
Source Driver, Pin 2	Sink Driver, Pin 5	Output, Pin 4	
		UDN2935Z	UDN2950Z
Low	Low	High	Low
Low	High	High	High Z
High	Low	Low	High
High	High	High Z	High

TEST FIGURE 1



Dwg. No. A-12,117

TEST FIGURE 2



Dwg. No. A-12,118

APPLICATION NOTES

It should be noted that an additional power dissipation component may arise from crossover currents flowing from supply to ground when current direction through the load is reversed. This is due to differences in the switching speeds between the source and sink drivers. Although the internal logic lockout protects these devices from catastrophic failure, the crossover power component can cause device operation at substantially higher junction temperatures.

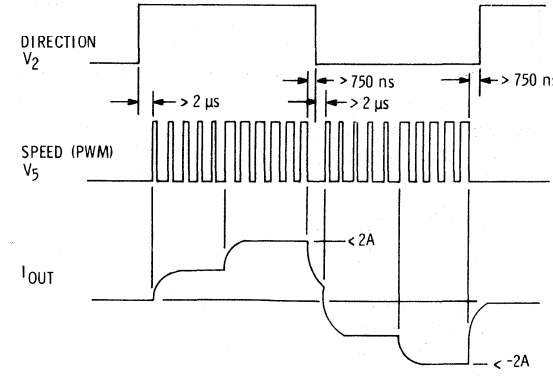
If timing conditions are ignored, the magnitude of this power can be approximated as:

$$P_D = V_S \times I_C \times t \times f$$

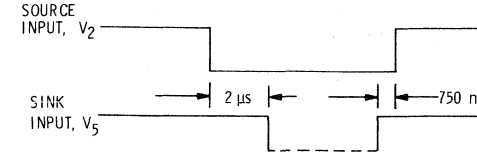
where V_S = *supply voltage*.
I_C = *crossover current (≈ 3.5 A max.)*
t = *crossover current duration (≈1 µs)*
f = *frequency of direction change*

In some applications (high switching speeds or high package power dissipation), it is recommended that the inputs be driven separately, and that the sink driver not be turned ON for at least 2 µs (maximum source t_{PD}) after the source driver input is turned OFF. The sink driver should be turned OFF at least 750 ns (maximum sink t_{PD}) before the source driver is turned ON.

RECOMMENDED TIMING CONDITIONS
(UDN2950Z Shown)



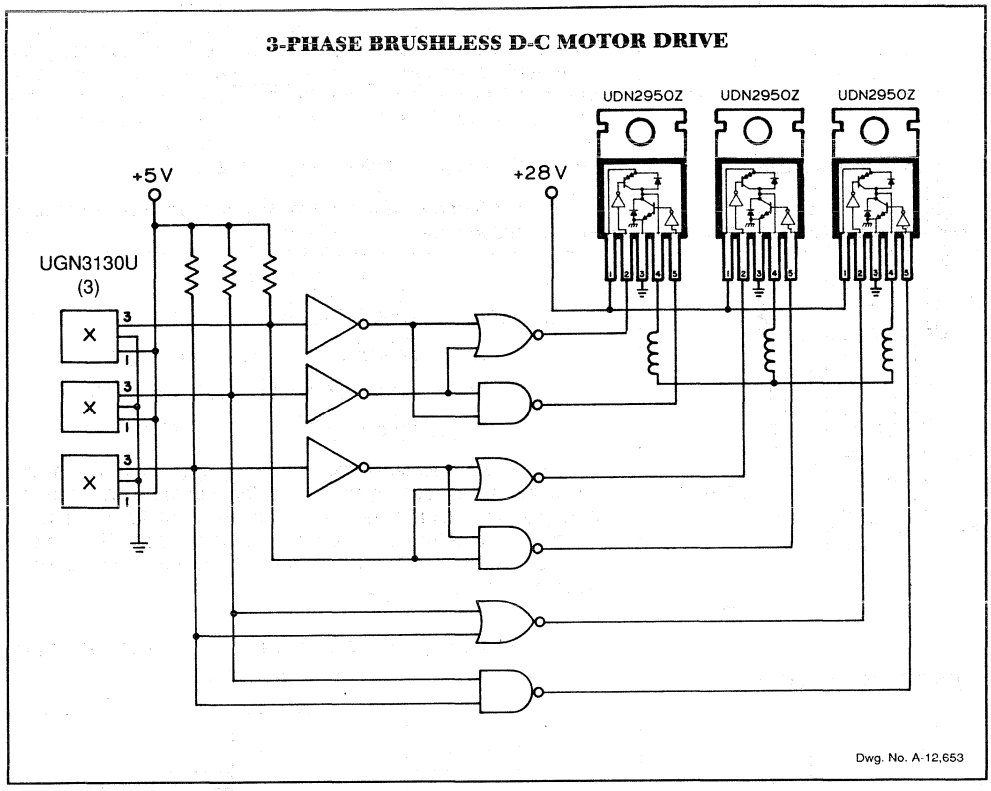
Dwg. No. A-12,120



Dwg. No. A-12,119

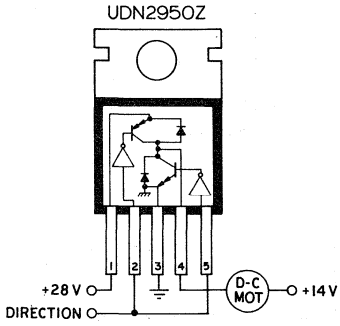
TYPICAL APPLICATIONS

3-PHASE BRUSHLESS D-C MOTOR DRIVE



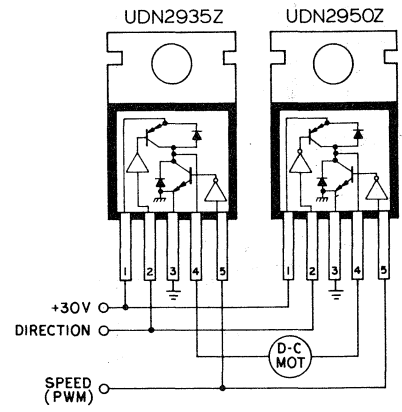
Dwg. No. A-12,653

SINGLE-WINDING D-C OR STEPPER MOTOR DRIVE



Dwg. No. A-12,114

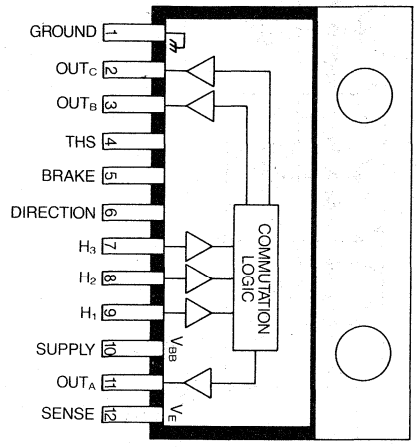
FULL-BRIDGE D-C SERVO MOTOR DRIVE



Dwg. No. A-12,115

2936

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS



Dwg. No W-188

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Supply Voltage, V_{BB} . . . . . **45 V**
Output Current, I_{OUT}
(continuous) . . . . . **±2.0 A**
(peak) . . . . . **±3.0 A**
Input Voltage Range, V_{IN} . . . . **-0.3 V to 15 V**
Threshold Voltage, V_{THS} . . . . . **15 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Note: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

Combining logic and power, the UDN2936W and UDN2936W-120 provide commutation and drive for three-phase brushless dc motors. Each of the three outputs are rated at 45 V and ±2 A (±3 A peak), and include internal ground clamp and flyback diodes. These drivers also feature internal commutation logic, PWM current control, and thermal shutdown protection.

The UDN2936W and UDN2936W-120 are compatible with single-ended digital or linear Hall effect sensors. The commutating logic is programmed for 60° (UDN2936W) or 120° (UDN2936W-120) electrical separation. Current control is accomplished by sensing current through an external sense resistor and pulse-width modulating the source drivers. Voltage thresholds and hysteresis can be externally set by the user. If desired, internal threshold and hysteresis defaults (300 mV, 7.5 percent) can be used. The UDN2936W/W-120 also include braking and direction control. Internal protection circuitry prevents crossover current when braking or changing direction.

For maximum power-handling capability, the UDN2936W and UDN2936W-120 are supplied in 12-pin single in-line power tab packages. An external heat sink may be required for high-current applications. The tab is at ground potential and needs no insulation.

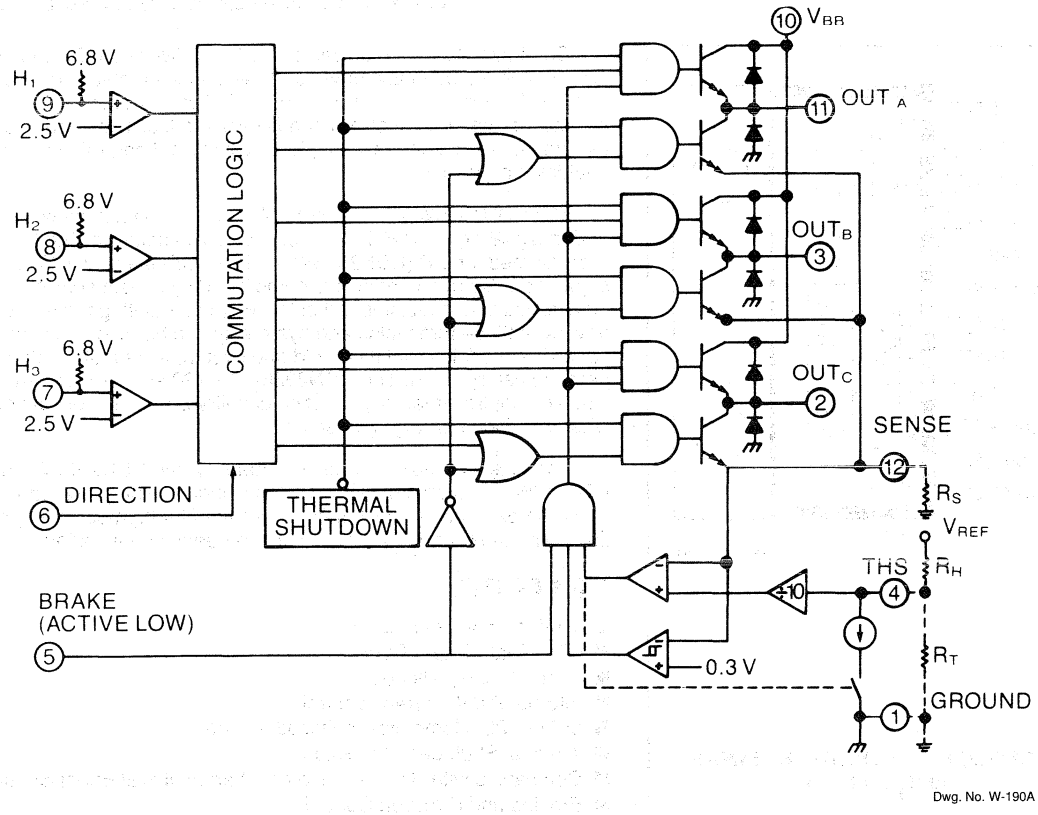
FEATURES

- 10 V to 45 V Operation
- ±3 A Peak Output Current
- Internal Clamp Diodes
- Internal PWM Current Control
- 60° or 120° Commutation Decoding Logic
- Thermal Shutdown Protection
- Compatible with Single-Ended or Differential Hall Effect Sensors
- Braking and Direction Control

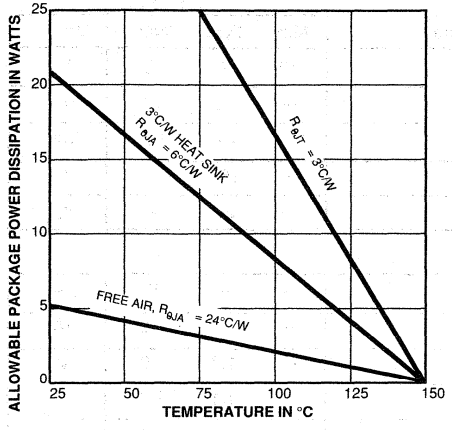
Always order by complete part number:

Part Number	Sensor Inputs
UDN2936W	Single-Ended, 60° Separation
UDN2936W-120	Single-Ended, 120° Separation

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. W-190A



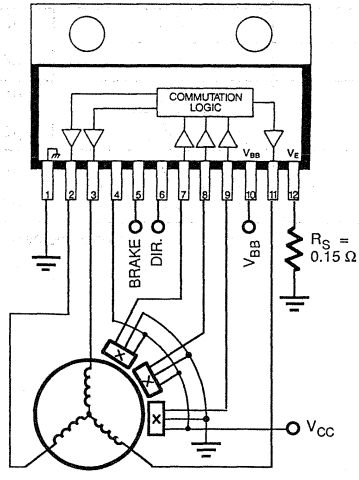
Dwg. GP-012

COMMUTATION TRUTH TABLE
UDN2936W

Hall Sensor Inputs					Outputs		
H_1	H_2	H_3	DIRECTION	BRAKE	OUT_A	OUT_B	OUT_C
High	High	High	Low	High	Z	Low	High
High	High	Low	Low	High	High	Low	Z
High	Low	Low	Low	High	High	Z	Low
Low	Low	Low	Low	High	Z	High	Low
Low	Low	High	Low	High	Low	High	Z
Low	High	High	Low	High	Low	Z	High
High	High	High	High	High	Z	High	Low
High	High	Low	High	High	Low	High	Z
High	Low	Low	High	High	Low	Z	High
Low	Low	Low	High	High	Z	Low	High
Low	Low	High	High	High	High	Low	Z
Low	High	High	High	High	High	Z	Low
X	X	X	X	Low	Low	Low	Low

X= Irrelevant
Z = High Impedance

TYPICAL APPLICATION



Dwg. EP-033

COMMUTATION TRUTH TABLE
UDN2936W-120

Hall Sensor Inputs					Outputs		
H_1	H_2	H_3	DIRECTION	BRAKE	OUT_A	OUT_B	OUT_C
High	Low	High	Low	High	Z	Low	High
High	Low	Low	Low	High	High	Low	Z
High	High	Low	Low	High	High	Z	Low
Low	High	Low	Low	High	Z	High	Low
Low	High	High	Low	High	Low	High	Z
Low	Low	High	Low	High	Low	Z	High
High	Low	High	High	High	Z	High	Low
High	Low	Low	High	High	Low	High	Z
High	High	Low	High	High	Low	Z	High
Low	High	Low	High	High	Z	Low	High
Low	High	High	High	High	High	Low	Z
Low	Low	High	High	High	High	Z	Low
X	X	X	X	Low	Low	Low	Low

X= Irrelevant
Z = High Impedance

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_j \leq$ +150°C, V_{BB} = 45 V

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	V_{BB}	Operating	10	—	45	V
Supply Current	I_{BB}	Outputs Open	—	32	40	mA
		V_{BRAKE} = 0.8 V	—	42	50	mA
Thermal Shutdown Temperature	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	25	—	°C
Output Drivers						
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	—	50	µA
		V_{OUT} = 0 V	—	—	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = -1 A	—	1.7	1.9	V
		I_{OUT} = +1 A	—	1.1	1.3	V
		I_{OUT} = -2 A	—	1.9	2.1	V
		I_{OUT} = +2 A	—	1.4	1.6	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±2 A, L = 2 mH	45	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	1.8	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 45 V	—	—	50	µA
Output Switching Time	t_r	I_{OUT} = ±2 A, Resistive Load	—	2.0	—	µs
	t_f	I_{OUT} = ±2 A, Resistive Load	—	2.0	—	µs
Turn-ON Delay (Resistive Load)	t_{on}	Source Drivers, 0 to -2 A	—	1.25	—	µs
		Sink Drivers, 0 to +2 A	—	1.9	—	µs
Turn-OFF Delay (Resistive Load)	t_{off}	Source Drivers, -2 A to 0	—	1.7	—	µs
		Sink Drivers, +2 A to 0	—	0.9	—	µs

Continued next page...

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{BB} = 45 V continued

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Logic						
Logic Input Voltage	$V_{IN(1)}$	V_{DIR} or V_{BRAKE}	2.0	—	—	V
	$V_{IN(0)}$	V_{DIR} or V_{BRAKE}	—	—	0.8	V
Sensor Input Voltage Threshold	V_{IN}	H_1, H_2, or H_3	—	2.5	—	V
Input Current	$I_{IN(1)}$	V_{DIR} = 2 V	—	150	200	µA
		V_{BRAKE} = 2 V	—	<1.0	5.0	µA
		V_H = 5 V	—	-190	-220	µA
	$I_{IN(0)}$	V_{DIR} = 0.8 V	—	35	50	µA
		V_{BRAKE} = 0.8 V	—	-5.0	-20	µA
		V_H = 0.8 V	—	-0.64	-1.0	mA
	I_{THS}	$V_{THS} \geq$ 3.0 V	—	-8.0	-15	µA
		V_{THS} < 3.0 V, $V_{SENSE} < V_{THS}/10.5$	—	-15	-30	µA
		V_{THS} < 3.0 V, $V_{SENSE} > V_{THS}/9.5$	190	250	310	µA
Current Limit Threshold		V_{THS}/V_{SENSE} at trip point, V_{THS} < 3.0 V	9.5	10	10.5	
Default Sense Trip Voltage	V_{SENSE}	$V_{THS} \geq$ 3.0 V	270	300	330	mV
Default Hysteresis		$V_{THS} \geq$ 3.0 V	—	7.5	—	%
Deadtime	t_d	BRAKE or DIRECTION	—	2.0	—	µs

APPLICATIONS INFORMATION

The UDN2936W and UDN2936W-120 power drivers provide commutation logic and power outputs to drive three-phase brushless dc motors.

The UDN2936W and UDN2936W-120 are designed to interface with single-ended linear or digital Hall effect devices (HEDs). Internal pull-up resistors allow for direct use with open-collector digital HEDs. The H_N inputs have 2.5 V thresholds.

The commutation logic provides decoding for HEDs with 60° (UDN2936W) or 120° (UDN2936W-120) electrical separation. At any one step in the logic sequencing, one half-bridge driver is sourcing current, one driver is sinking current, and one driver is in a high-impedance state (see Truth Table).

A logic low on the BRAKE pin turns ON the three sink drivers and turns OFF the three source drivers, essentially shorting the motor windings to ground. During braking, the back-electromotive force generated by the motor produces a current which dynamically brakes the motor. Depending upon the rotational velocity of the motor, this current can approach the locked rotor current level (which is limited only by the motor winding resistance). During braking the output current limiting circuitry is disabled and care should be taken to ensure that the back-EMF generated brake current does not exceed the maximum rating (3 A peak) of the sink drivers and ground clamp diodes.

Changing the logic level of the DIRECTION pin inverts the output states, thus reversing the direction of the motor. Changing the direction of a rotating motor produces a back-EMF current similar to when braking the motor. The load current should not be allowed to exceed the maximum rating (±3 A peak) of the drivers.

An internally generated dead time (t_d) of approximately 2 µs prevents potentially destructive crossover currents that can occur when changing direction or braking.

Motor current is internally controlled by pulse-width modulating the source drivers with a preset hysteresis format. Load current through an external sense resistor (R_S) is constantly monitored. When the current reaches the set trip point (determined by an external reference voltage or internal default), the source driver is disabled. Current recirculates through the ground clamp diode, motor winding, and sink driver. An internal constant-current sink reduces the trip point (hysteresis). When the decaying current reaches this lower threshold, the source driver is enabled again and the cycle repeats.

Thresholds and hysteresis can be set with external resistors or internal defaults can be used. With $V_{THS} > 3.0$ V, the trip point is internally set at 300 mV with 7.5% hysteresis. Load current is then determined by the equation:

$$I_{TRIP} = 0.3 / R_S$$

With V_{THS} < 3.0 V, the threshold, hysteresis percentage, and peak current are set with external resistors according to the equations:

$$\text{Threshold Voltage } (V_{THS}) = V_{REF} \bullet R_T / (R_H + R_T)$$

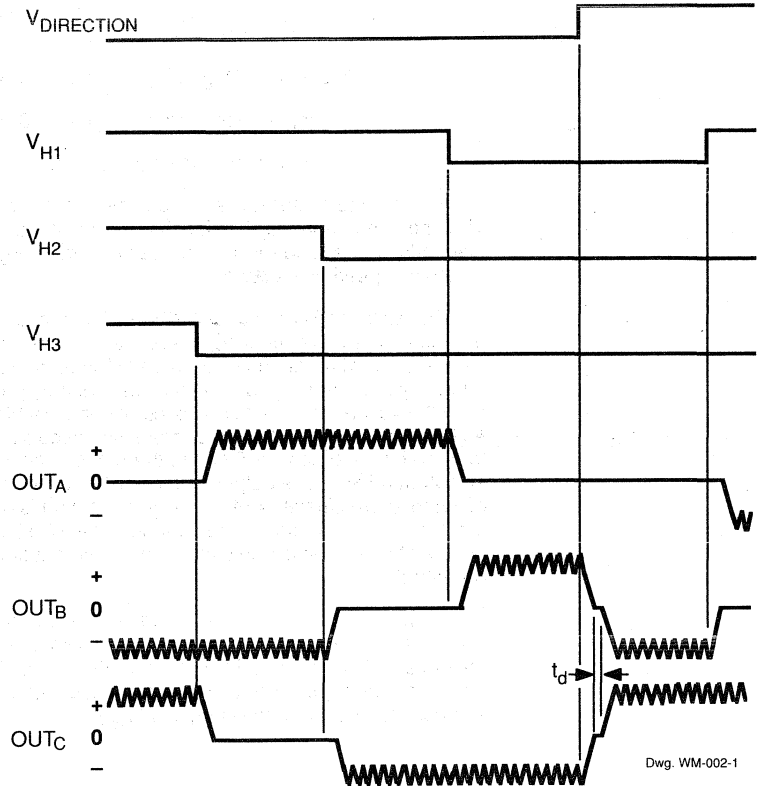
$$\text{Hysteresis Percentage} = R_H / 50\ V_{REF}$$

$$\text{Load Trip Current } (I_{TRIP}) = V_{THS} / 10\ R_S$$

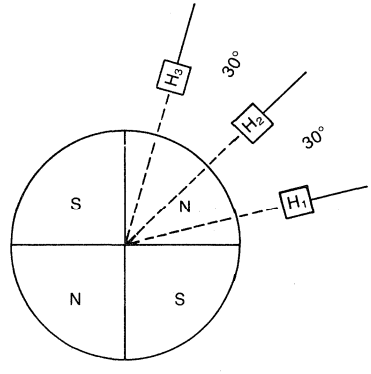
Percentage hysteresis is a fixed value independent of load current. The chopping frequency is a function of circuit parameters including load inductance, load resistance, supply voltage, hysteresis, and switching speed of the drivers.

The UDN2936W and UDN2936W-120 outputs are rated for normal operating currents of up to ±2 A and startup currents to ±3 A (see cautions above regarding braking and changing of motor direction). Internal power ground clamp and flyback diodes protect the outputs from the voltage transients that occur when switching inductive loads. All devices also feature thermal protection circuitry. If the junction temperature reaches +165°C, the thermal shutdown circuitry turns OFF all output drivers. The outputs are re-enabled when the junction cools down to approximately +140°C. This protection is only intended to protect the device from failures due to excessive junction temperature or loss of heat sinking and should not imply that output short circuits are permitted.

As with all high-power integrated circuits, the printed wiring board should utilize a heavy ground plane. For optimum performance, the drivers should be soldered directly into the board. The power supply should be decoupled with an electrolytic capacitorb (>10 μF) as close as possible to the device supply pin (V_{BB}).



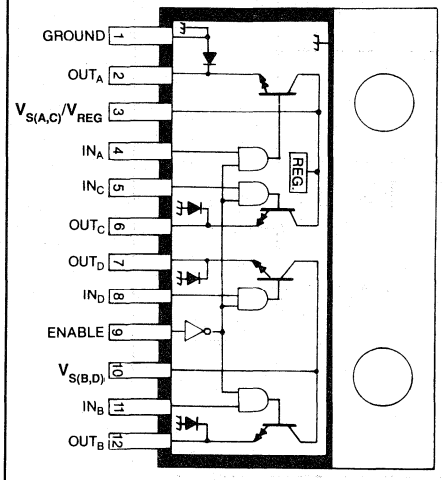
TYPICAL HALL EFFECT SENSOR LOCATIONS



Dwg. No. W-193

2944

QUAD HIGH-CURRENT, HIGH-VOLTAGE SOURCE DRIVER



Dwg. No. A-13,054

Capable of driving loads to 4 A at supply voltages to 60 V (inductive loads to 35 V), the UDN2944W is a quad high-current, high-voltage source driver. Each of the four power drivers can provide space- and cost-saving interface between low-level signal-processing circuits and high-power loads in harsh environments.

Individual supply lines have been provided for each pair of drivers so that different supplies can be used to drive multiple loads. The controlling inputs are TTL or CMOS compatible. The outputs include transient-suppression diodes for inductive loads.

This quad Darlington array is designed to serve as an interface between low-level circuitry and peripheral-power loads such as solenoids, motors, incandescent displays, heaters, and similar loads of up to 240 W per channel. The UDN2944W is an ideal complement to the UDN2878W quad 4 A sink driver.

For maximum power-handling capability, the UDN2944W driver is supplied in a 12-pin single in-line, power-tab package that allows efficient attachment of an external heat sink for maximum allowable package power dissipation. An external heat sink is usually required for proper operation of this device. The tab is at ground potential and needs no insulation.

FEATURES

- Output Current to 4 A
- Output Voltage to 60 V
- Loads to 960 W
- Integral Output Suppression Diodes
- TTL and CMOS Compatible Inputs
- Plastic Single In-Line Package
- Heat-Sink Tab

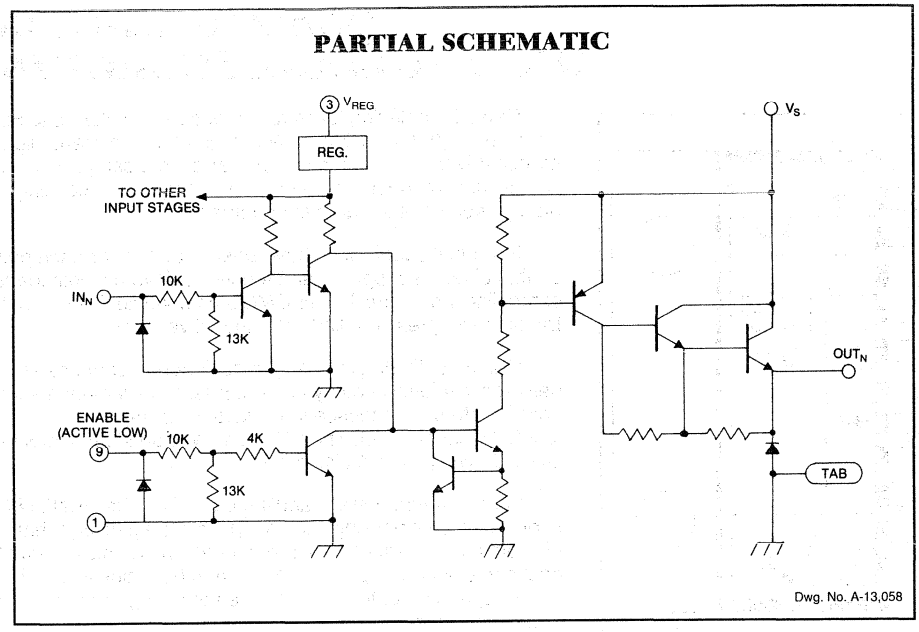
ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Supply Voltage Range, V_S . . . . **10 V to 60 V**
Output Current, I_{OUT} (dc) . . . . . **-4 A**
(peak) . . . . . **-5 A**
Input Voltage, V_{IN} . . . . . **15 V**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

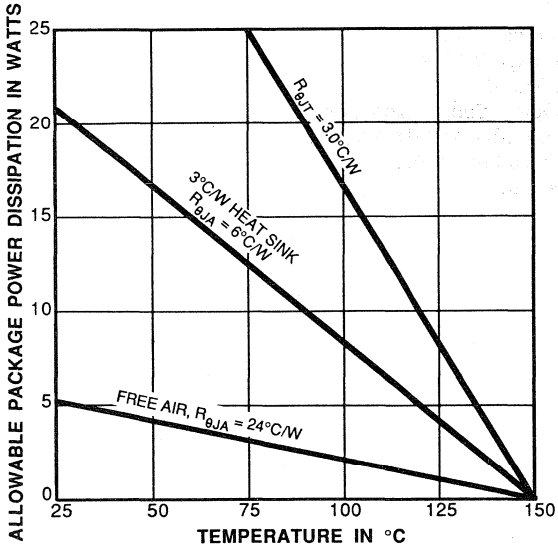
Output current rating will be limited by ambient temperature, duty cycle, heat sinking, air flow, and number of outputs conducting. Under any set of conditions, do not exceed the -5.0 A peak current and a junction temperature of +150°C.

Always order by complete part number: **UDN2944W** .

PARTIAL SCHEMATIC



Dwg. No. A-13,058



Dwg. GP-012

TRUTH TABLE

INPUT	ENABLE	OUTPUT
L	L	L
H	L	H
L	H	L
H	H	L

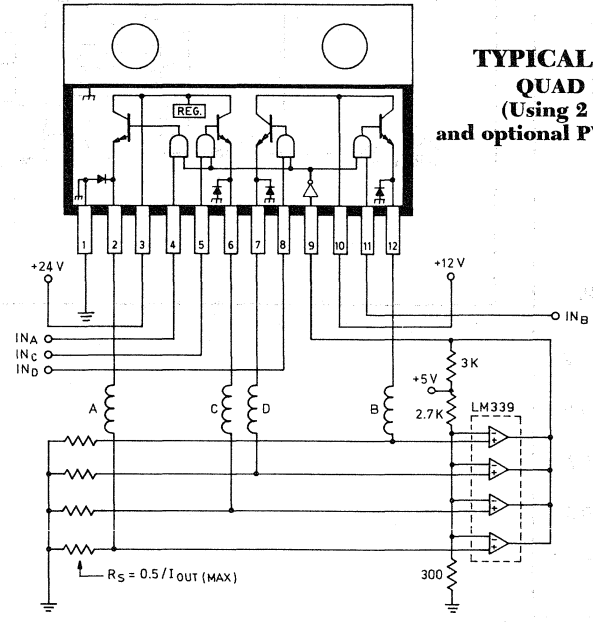
NOTE: Pin 3 must be connected to V_S for operation of input logic gates.

2944
QUAD HIGH-CURRENT, HIGH-VOLTAGE SOURCE DRIVER

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_S = 60 V, V_{ENABLE} = 0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Supply Voltage Range	V_S		10	60	V
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, V_{ENABLE} = 2.4 V	—	50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = -4 A, L = 3 mH	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = -1 A, V_{IN} = 2.4 V	—	1.8	V
		I_{OUT} = -4 A, V_{IN} = 2.4 V	—	2.5	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$	2.0	—	V
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 2.4 V	—	220	µA
		$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 12 V	—	1.5	mA
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$ = 0.8 V	—	50	µA
Total Supply Current	I_S	All drivers ON, All outputs open	—	25	mA
Clamp Diode Leakage Current	I_R	V_R = 60 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 4 A	—	2.2	V
Turn-On Delay	t_{ON}	0.5 E_{in} to 0.5 E_{out}, R_L = 15Ω	—	2.0	µs
Turn-Off Delay	t_{OFF}	0.5 E_{in} to 0.5 E_{out}, R_L = 15Ω	—	10	µs

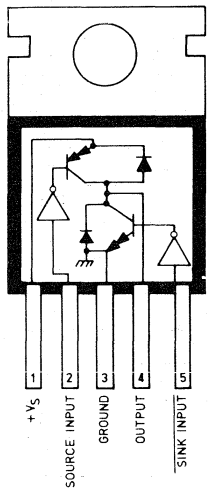
NOTE: Negative current is defined as coming out of (sourcing) the device being tested.



TYPICAL APPLICATION
QUAD RELAY DRIVE
(Using 2 Voltage Sources and optional PWM Current Limiting)

2950

BIPOLAR HALF-BRIDGE MOTOR DRIVER



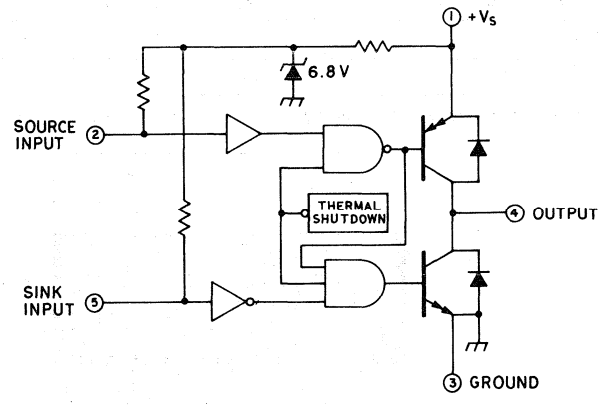
Dwg. No. A-11,177

Complete technical information for the UDN2950Z is included with the UDN2935Z.

FEATURES

- 3.5 A Peak Output
- 37 V Min. Output Breakdown
- Output Transient Protection
- Tri-State Outputs
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- Internal Thermal Shutdown
- High-Speed Chopper (to 100 kHz)
- Replaces UDN2949Z, SN75605

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. 12,112

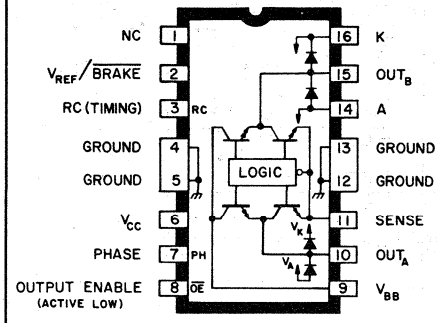
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range,
V_S . . . . . **8.0 V to 35 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to +7.0 V**
Peak Output Current (100 ms, 10% d-c),
I_{OP} . . . . . **±3.5 A**
Continuous Output Current,
I_{OUT} . . . . . **±2.0 A**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**

2953 AND 2954

FULL-BRIDGE PWM MOTOR DRIVERS

UDN2953B



Dwg. No. A-13,024

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Motor Supply Voltage, V_{BB} . . . . . **50 V**
Output Current, I_{OUT}
(Peak) . . . . . **±3.5 A**
(Continuous) . . . . . **±2.0 A**
Flyback Diode Voltage, V_K . . . . . **V_{BB}**
Minimum Clamp Diode Voltage, V_A . . . . . **Ground**
Logic Supply Voltage, V_{CC} . . . . . **7.0 V**
Logic Input Voltage, V_{PHASE}, V_{ENABLE} . . . . . **V_{BB}**
Sense Voltage, V_{SENSE} . . . . . **1.5 V**
Reference Voltage, V_{REF}/BRAKE . . . . . **15 V**
Package Power Dissipation, P_D . . . . . **See Graphs**
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

The UDN2953B and UDN2954W are designed for bidirectional control of dc or stepper motors with continuous output currents to 2 A and peak start-up currents as high as 3.5 A. For pulse-width modulated (chopped-mode) operation, the output current is determined by the user's selection of a reference voltage and sensing resistor while the OFF pulse duration is set by an external RC timing network. PWM operation is characterized by maximum efficiency and low power-dissipation levels. Extensive internal circuit protection includes thermal shutdown with hysteresis, transient-suppression diodes, and crossover current protection.

When the V_{REF}/BRAKE pin is low (<0.8 V), the braking function is enabled. This turns both sink drivers OFF and the source drivers are turned ON. When V_{REF}/BRAKE is set above 2.4 V, that voltage (and the current sensing resistor) determines the load current trip point. An RC TIMING pin is available to use for an internal one-shot to control load current decay time.

The UDN2953B driver is supplied in a 16-pin dual-in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. The UDN2954W, for higher package power dissipation requirements, is supplied in a 12-pin single in-line power tab package. In both package styles, the heat sink is at ground potential and needs no insulation.

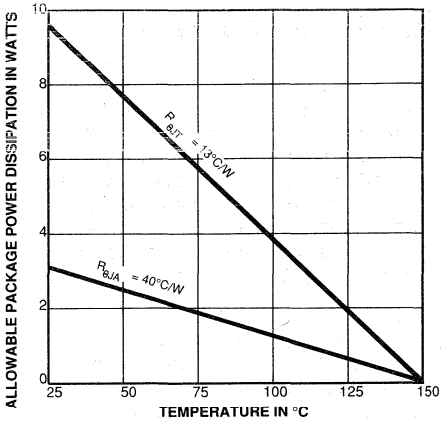
FEATURES

- 50 V Output Voltage Rating
- 2 A Continuous Output Rating
- Internal Flyback Diodes
- Thermal Shutdown
- Crossover Current Protection
- BRAKE, ENABLE, and Current-Limit Functions

Always order by complete part number:

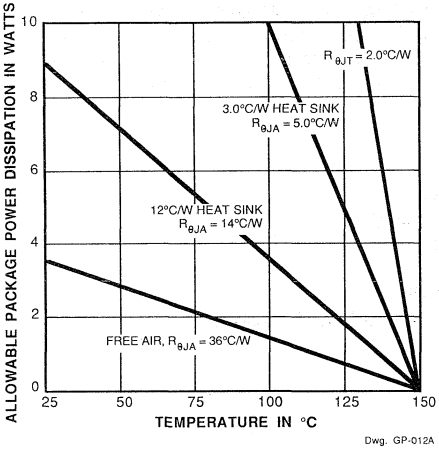
Part Number	Package
UDN2953B	16-Pin DIP
UDN2954W	12-Pin Power-Tab SIP

UDN2953B



Dwg. GP-004-1

UDN2954W



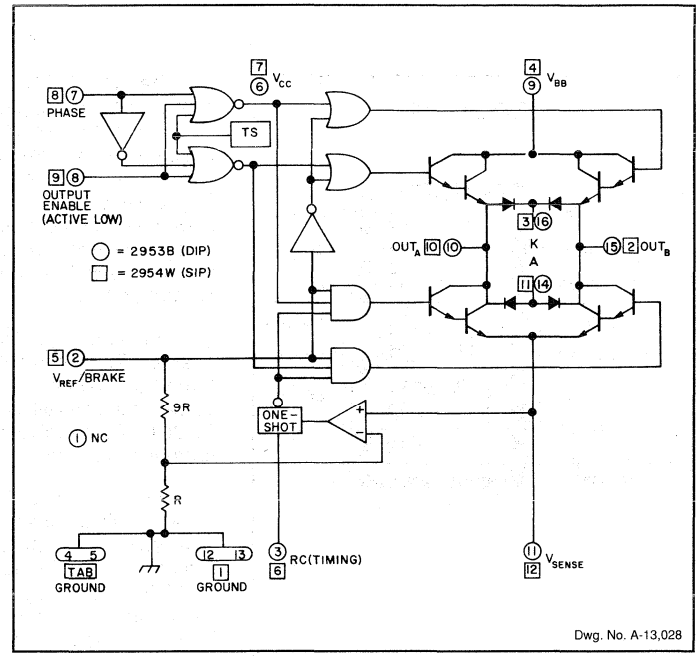
Dwg. GP-012A

TRUTH TABLE

Output Enable	Phase	V_{REF}/BRAKE	Out_A	Out_B
Low	High	> 2.4 V	High	Low
Low	Low	> 2.4 V	Low	High
High	X	> 2.4 V	Open	Open
X	X	< 0.8 V	High	High

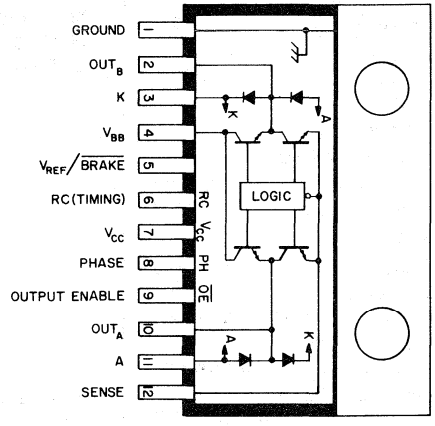
X = Irrelevant

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,028

UDN2954W



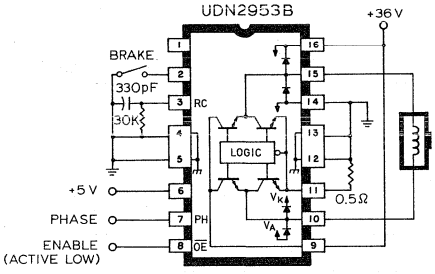
Dwg. No. A-13,023

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{BB} = 50 V, V_{CC} = 5 V, V_{SENSE} = 0 V, RC = 20 kΩ/470 pF to Ground.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers (OUT_A or OUT_B)						
Output Supply Range	V_{BB}		6.5	—	50	V
Output Leakage Current	I_{CEX}	V_{ENABLE} = 5 V, V_{OUT} = V_{BB}, (note)	—	—	50	µA
		V_{ENABLE} = 5 V, V_{OUT} = 0 V, (note)	—	—	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±2 A, L = 2 mH	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{ENABLE} = 0 V, I_{OUT} = ±0.5 A	—	1.0	1.2	V
		V_{ENABLE} = 0 V, I_{OUT} = ±1.0 A	—	1.2	1.4	V
		V_{ENABLE} = 0 V, I_{OUT} = ± 2.0 A	—	1.5	1.8	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	1.8	2.2	V
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V, V_{REF} = 2.4 V, No Load	—	20	30	mA
	$I_{BB(OFF)}$	V_{ENABLE} = V_{REF} = 2.4 V, No Load	—	2.5	3.5	mA
		V_{ENABLE} = 5 V, V_{REF} = 0.8 V, No Load	—	40	60	mA
Control Logic						
Logic Supply Range	V_{CC}		4.5	5.0	5.5	V
Logic Input Current	$I_{IN(1)}$	All Inputs = 2.4 V	—	<-1.0	-10	µA
	$I_{IN(0)}$	All Inputs = 0.8 V	—	-50	-200	µA
Logic Input Voltage	$V_{IN(1)}$	All Inputs	2.4	—	—	V
	$V_{IN(0)}$	All Inputs	—	—	0.8	V
V_{REF} Open-Circuit Voltage	$V_{REF(OPEN)}$	I_{REF} = 0	—	$V_{CC}/2$	—	V
Current Limit Threshold		V_{REF}/V_{SENSE} at Trip Point	9.5	10	10.5	—
Turn-On Delay	t_{on}	All Drivers	—	1.0	—	µs
Turn-Off Delay	t_{off}	All Drivers	—	1.0	—	µs
Thermal Shutdown Temp.	T_J		—	165	—	°C
Logic Supply Current	I_{CC}	V_{ENABLE} = V_{REF} = 2.4 V	—	15	20	mA
		V_{ENABLE} = 0.8 V, V_{REF} = 2.4 V	—	22	30	mA

NOTE: Tests performed at OUT_B with V_{PHASE} = 0.8 V and at OUT_A with V_{PHASE} = 2.4 V

TYPICAL APPLICATION



Dwg. No. A-12,649B

NOTE: Pin 3 must be connected to an RC network as shown, or to V_{CC}. It must **NOT** be left unconnected.

APPLICATIONS INFORMATION

The UDN2953B and UDN2954W full-bridge motor drivers are ideal for driving bidirectional dc servo, brushless dc, and 2-phase bipolar stepper motors with various current-control formats. Output current can be controlled by using an external sense resistor (R_{SENSE}) and an optional RC network and reference voltage for PWM current control, or by using an external PWM source.

The output current trip point is set by:

$$I_{TRIP} = \frac{V_{REF}}{10\ R_{SENSE}}$$

where the reference voltage (V_{REF}) can be between 2.4 V and 15 V. If left unconnected, V_{REF} defaults to $V_{CC}/2$ (see Figure 1).

When the bridge is turned ON, current increases in the motor and is sensed by the external sense resistor. When the current through the sense resistor reaches the trip point, the internal comparator triggers a monostable which turns OFF the sink drivers. As shown in Figure 2, the actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 µs.

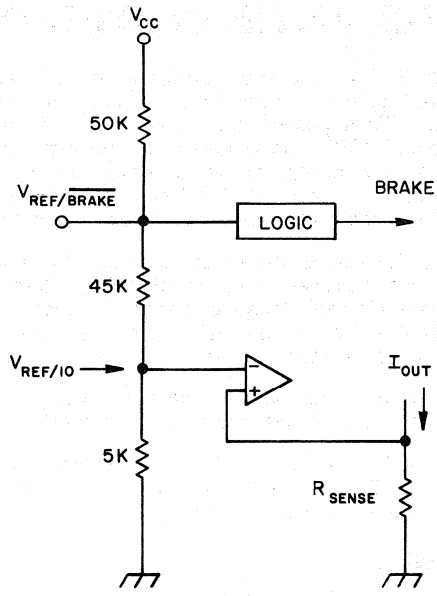
After the sink drivers turn OFF, the motor current decays, circulating through the source driver and flyback diode. The sink driver's OFF time (and therefore the magnitude of the current decrease) is determined by the monostable's external RC timing components, where t_{off} = RC within the range of 20 kΩ to 100 kΩ and 200 pF to 500 pF. If the RC pin is tied to V_{CC}, internal timing circuitry is activated, allowing current control without an external RC network. The internally generated t_{off} is approximately 12 µs at V_{CC} = 5 V and T_A = +25°C, increasing slightly with increasing temperatures. With RC tied to V_{CC}, I_{CC} will increase by approximately 6 mA.

When the sink driver is re-enabled, the motor current is again allowed to rise to the trip point. This cycle repeats itself, maintaining the average motor current at the desired level.

Average motor current can also be controlled with external current control logic by using the OUTPUT ENABLE pin. Toggling the OUTPUT ENABLE pin shuts OFF both the source and sink drivers. Both the flyback and ground-clamp diodes conduct during turn-OFF (anodes (A pin) connected to ground and cathodes (K pin) connected to V_{BB}), resulting in a very fast current decay. If the internal current control circuitry is not used, the RC pin should be connected to ground through a 20 kΩ (minimum) resistor.

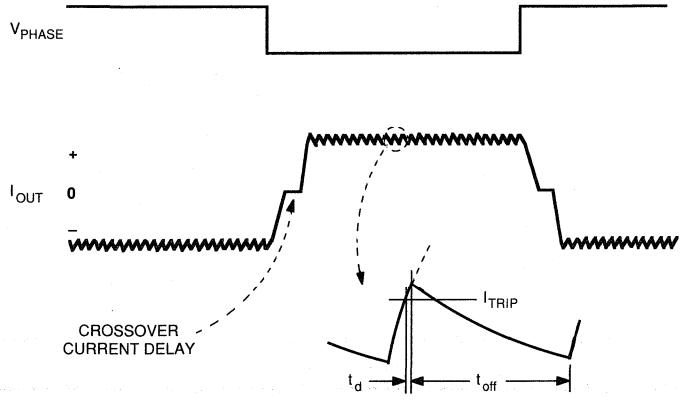
A logic low at the V_{REF}/BRAKE pin turns ON both source drivers and turns OFF both sink drivers, essentially shorting both ends of the motor winding to the motor supply. In this condition, the back-electromotive force (back-EMF) generated by the motor produces a current which dynamically brakes the motor. Depending upon the rotational velocity of the motor, this current level can approach that of a locked-rotor condition (which is limited only by the resistance of the motor winding). The internal current control circuitry is not operational when the brake function is used. Therefore, care should be exercised when braking to

FIGURE 1



Dwg. No. A-13,025

FIGURE 2



Dwg. No. WM-003-1

ensure that the current generated by the back-EMF never exceeds the absolute maximum rating of the drivers.

With bidirectional dc servo motors, the PHASE pin can be used for direction control. Similar to dynamically braking a motor, changing the direction of a rotating motor produces a current generated by the back-EMF. Again, this current should not be allowed to exceed the absolute maximum rating.

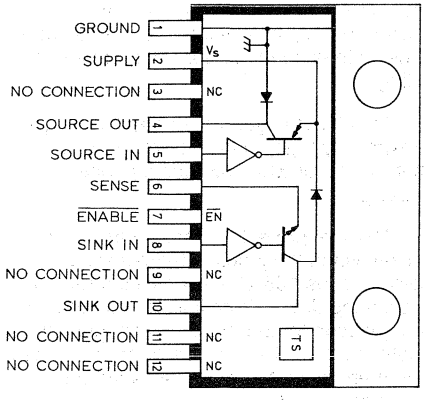
An internally generated deadtime (approximately 3 µs) prevents crossover currents that can occur when switching phases or braking.

Thermal protection circuitry turns OFF all drivers when the junction temperature typically reaches 165°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The thermal shutdown has a hysteresis of approximately 8°C.

The printed wiring board should utilize a heavy ground plane. For optimum performance, the driver should be soldered directly into the board. The load supply (V_{BB}) should be decoupled with an electrolytic capacitor (≥10 µF) as close as possible to the driver.

2955–2

HIGH-CURRENT HALF-BRIDGE POWER DRIVER



Dwg. PP-023

The UDN2955W–2 half-bridge power driver combines a high-current, half-bridge power driver with low-level control and protection circuitry. For PWM applications there are provisions for output current sensing and an ENABLE (active low) input. The output can source or sink up to 6 A continuously. This device features a minimum breakdown and sustaining voltage of 40 V. It can be used in pairs for full-bridge operation or in triplets for 3-phase brushless dc motors.

Protection is included which shuts down the device during over-temperature conditions caused by loss of cooling; internal flyback and clamp diodes are included for switching inductive loads. Internal logic lockout and delays prevent potentially destructive crossover currents. The logic inputs are compatible with TTL and 5 V CMOS logic systems.

A similar device, excluding the ENABLE and output current sensing provision, in a 5-lead TO-220 style package, is the UDN2951Z-2.

The UDN2955W–2 is supplied in a 12-lead power-tab single in-line plastic package. The tab is at ground potential, allowing multiple devices to share a common heat sink.

FEATURES

- ± 6 A Continuous Output Current
- Output Voltage to 40 V
- Internal Thermal Shutdown
- TTL and 5 V CMOS Compatible Inputs
- Integral Transient-Suppression Diodes

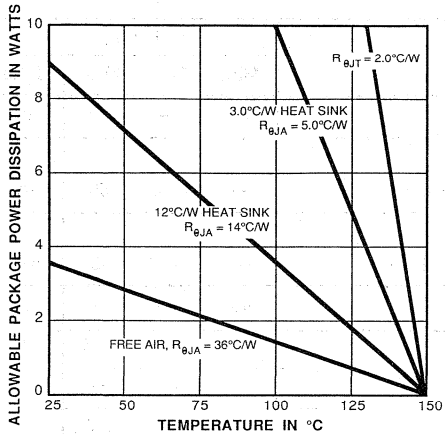
ABSOLUTE MAXIMUM RATINGS at $T_J \leq 150°C$

Supply Voltage, V_S . . . . . **40 V**
Output Current, I_{OUT} . . . . . **±6.0 A**
Input Voltage, V_{IN} . . . . . **7.0 V**
Sense Voltage, V_{SENSE} . . . . . **1.5 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to + 85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to + 150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified output current rating or a junction temperature of +150°C.

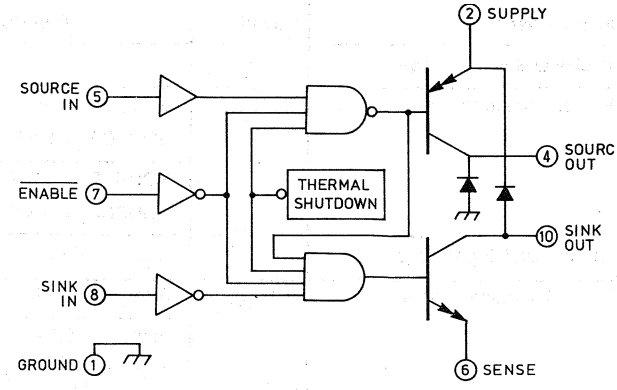
Always order by complete part number: **UDN2955W–2** .

2955-2
HIGH-CURRENT HALF-BRIDGE POWER DRIVER



Dwg. GP-012A

FUNCTIONAL BLOCK DIAGRAM



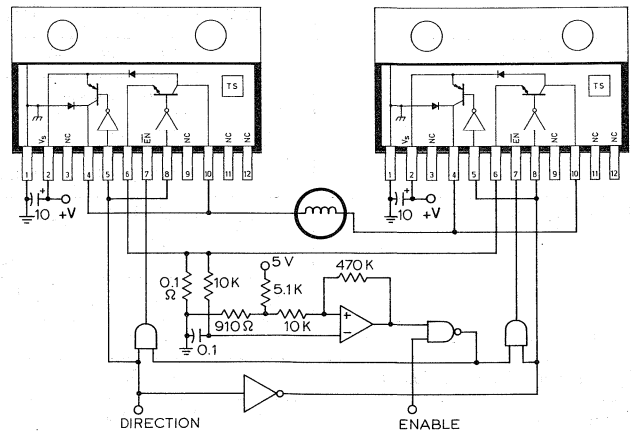
Dwg. FP-009

TRUTH TABLE

INPUTS			OUTPUTS	
ENABLE	SOURCE	SINK	SOURCE	SINK
Low	Low	Low	OFF	ON
Low	Low	High	OFF	OFF
Low	High	X	ON	OFF
High	X	X	OFF	OFF

X = Irrelevant

TYPICAL APPLICATION



The printed wiring board should utilize a heavy ground plane. For optimum performance, the driver should be soldered directly into the board. The power supply (V_S) should be decoupled with an electrolytic capacitor (≥ 10 µF) as close as possible to pin 2.

Dwg. EP-019A

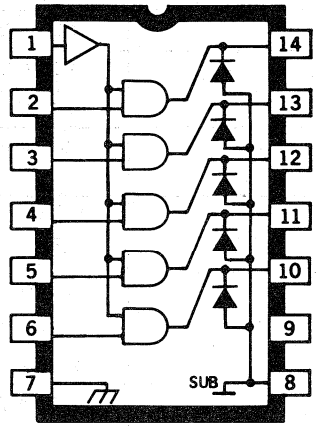
ELECTRICAL CHARACTERISTICS at T_A = + 25°C, $T_J \leq$ + 150°C, V_S = 40 V

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Functional Supply Range	V_S		10	—	40	V
Output Leakage Current	I_{CEX}	$SINK_{OUT}$ = 40 V, $SOURCE_{IN}$ = 0.8 V, $SINK_{IN}$ = 2.0 V	—	<1.0	50	µA
		$SOURCE_{OUT}$ = 0 V, $SOURCE_{IN}$ = 0.8 V, $SINK_{IN}$ = 2.0 V	—	<-1.0	- 50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ± 6.0 A, L =10 mH	40	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$SINK_{OUT}$ = 5.0 A	—	—	1.5	V
		$SINK_{OUT}$ = 6.0 A	—	—	2.0	V
		$SOURCE_{OUT}$ = -5.0 A	—	—	2.0	V
		$SOURCE_{OUT}$ = -6.0 A	—	—	2.5	V
Input Voltage	Logic 1	$SOURCE_{IN}$ or $SINK_{IN}$	2.0	—	—	V
	Logic 0	$SOURCE_{IN}$ or $SINK_{IN}$	—	—	0.8	V
Input Current	Logic 1	$SOURCE_{IN}$ or $SINK_{IN}$ = 2.0 V	—	3.0	10	µA
	Logic 0	$SOURCE_{IN}$ or $SINK_{IN}$ = 0.8 V	—	-1.0	-10	µA
Propagation Delay	t_{PHL}	Sink Driver (includes Turn-On Delay)	—	2.5	—	µs
		Source Driver	—	2.5	—	µs
	t_{PLH}	Sink Driver	—	0.2	—	µs
		Source Driver (includes Turn-On Delay)	—	2.5	—	µs
Supply Current	$I_{S(ON)}$	$SOURCE_{IN}$ = 2.0 V	—	10	15	mA
		$SOURCE_{IN}$ = $SINK_{IN}$ = 0.8 V	—	20	25	mA
	$I_{S(OFF)}$	$SOURCE_{IN}$ = 0.8 V, $SINK_{IN}$ = 2.0 V	—	8.0	10	mA
Flyback Diode Forward Voltage	V_F	I_F = 6.0 A	—	—	2.8	V
Clamp Diode Forward Voltage	V_F	I_F = 6.0 A	—	—	2.1	V
Diode Leakage Current	I_R	Each Diode, V_R = 40 V	—	<1.0	50	µA
Thermal Shutdown	T_J		—	165	—	°C

NOTE: Typical Data is given for circuit design information only.
Negative current is defined as coming out of (sourcing) the specified device pin.

2957

HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVER



Dwg. No. A-10,229A

ABSOLUTE MAXIMUM RATINGS
at + 25°C Free-Air Temperature
(Reference Pin 7)

Output Voltage, V_{OUT} . . . . . **-80 V**
Input Voltage, V_{IN} . . . . . **+10 V**
Output Current, I_{OUT} . . . . . **-500 mA**
Power Dissipation,
P_D (any one driver) . . . . . **1.0 W**
(total package) . . . . . **2.0 W***
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*Derate at the rate of 16.67 mW/°C above 25°C

Comprised of five common-collector NPN Darlington output stages, associated common-base PNP input stages, and a common ENABLE stage, the UDN2957A high-voltage, high-current source driver is used to switch the ground end of loads that are directly connected to a negative supply. Typical loads include telephone relays, PIN diodes, and LEDs.

This device will sustain output OFF voltages of -80 V and will source currents to -500 mA per driver. Under normal operating conditions, it will sustain load currents of -200 mA on each of the five drivers simultaneously at ambient temperatures up to +70°C.

The UDN2957A driver has appropriate input-current limiting resistors for operation from TTL, Schottky TTL, DTL, and 5 V CMOS. The input and ENABLE levels must both be biased towards the positive supply to activate the output load.

Integral transient-suppression diodes allow this device to be used with inductive loads without adding discrete diodes. In order to maintain isolation between drivers, the substrate should be connected to the most negative supply.

Input connections are on one side of the dual in-line package, output connections on the other side to simplify printed wiring board layout.

The UDN2957A high-voltage, high-current driver is supplied in a 14-lead dual in-line package conforming to JEDEC outline TO-116 (MO-001AA).

FEATURES

- 500 mA Output Source Current
- 50 V Output Sustaining Voltage
- Output Transient Protection
- TTL, DTL, 5 V CMOS Input

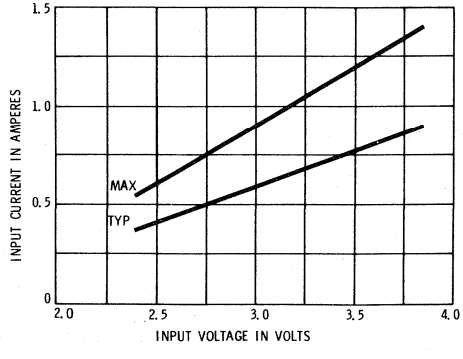
Always order by complete part number: **UDN2957A** .

2957
NEGATIVE SUPPLY, 5-CHANNEL SOURCE DRIVER

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, $V_{ENABLE} = V_{IN}$ (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limit
Output Leakage Current	I_{CEX}	$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70$°C	-200 µA Max.
		$V_{IN} = 0.4$ V, $V_{ENABLE} = 3.85$ V, $V_{OUT} = -80$ V, $T_A = +70$°C	-200 µA Max.
		$V_{IN} = 3.85$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70$°C	-200 µA Max.
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	-1.20 V Max.
		$V_{IN} = 2.7$ V, $I_{OUT} = -175$ mA	-1.35 V Max.
		$V_{IN} = 3.9$ V, $I_{OUT} = -350$ mA	-1.70 V Max.
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{IN} = 0.4$ V, $I_{OUT} = -25$ mA	50 V Min.
Input Current	$I_{IN(ON)}$	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	675 µA Max.
		$V_{IN} = 3.85$ V, $V_{OUT} = -2.0$ V	1.40 mA Max.
	$I_{IN(OFF)}$	$I_{OUT} = -500$ µA, $T_A = +70$°C	50 µA Min.
Output Source Current	I_{OUT}	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	-125 mA Min.
		$V_{IN} = 2.7$ V, $V_{OUT} = -2.0$ V	-200 mA Min.
		$V_{IN} = 3.0$ V, $V_{OUT} = -2.0$ V	-250 mA Min.
		$V_{IN} = 3.3$ V, $V_{OUT} = -2.0$ V	-300 mA Min.
		$V_{IN} = 3.6$ V, $V_{OUT} = -2.0$ V	-350 mA Min.
Clamp Diode Leakage Current	I_R	$V_R = 80$ V	50 µA Max.
Clamp Diode Forward Voltage	V_F	$I_F = 350$ mA	2.0 V Max.
Turn-On Delay	t_{ON}	0.5 E_{IN} to 0.5 E_{OUT}, $R_L = 400\ \Omega$, $C_T = 25$ pF	4.0 µs Max.
Turn-Off Delay	t_{OFF}	0.5 E_{IN} to 0.5 E_{OUT}, $R_L = 400\ \Omega$, $C_T = 25$ pF	10 µs Max.

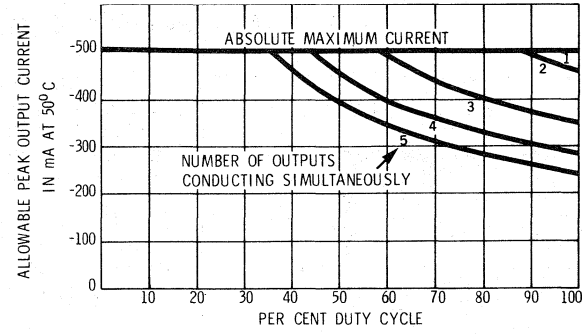
INPUT CURRENT AS A FUNCTION OF VOLTAGE



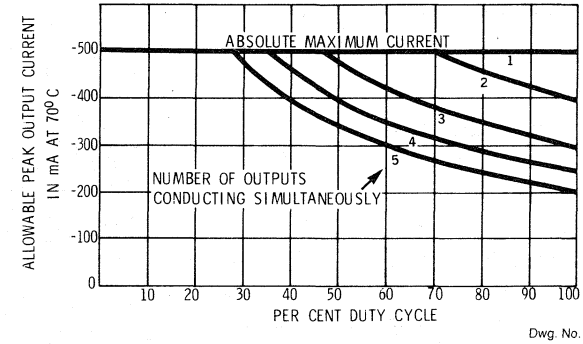
Dwg. No. A-11,061

2957
NEGATIVE SUPPLY, 5-CHANNEL SOURCE DRIVER

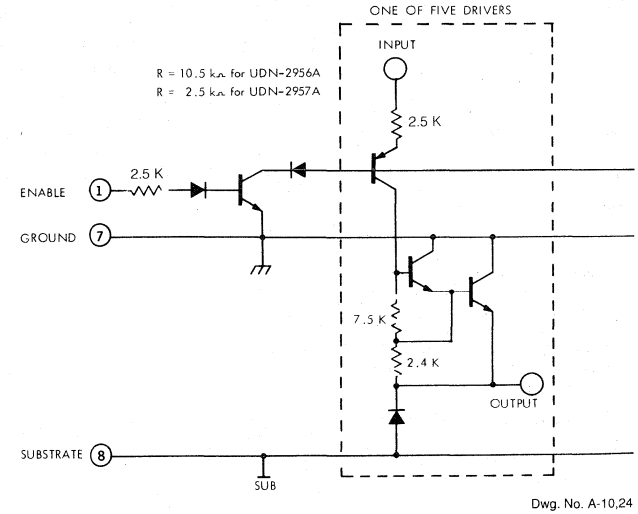
INPUT CURRENT AS A FUNCTION OF VOLTAGE



Dwg. No. A-11,0



Dwg. No. A-11,0

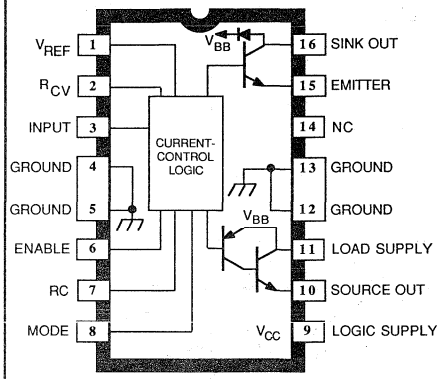


Dwg. No. A-10,24

2961

HIGH-CURRENT HALF-BRIDGE PRINTHEAD/MOTOR DRIVER—WITH INTERNAL CURRENT SENSING AND CONTROL

UDN2961B



Dwg. PP-035

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{BB} . . . . . 45 V
Output Current, I_{OUT} (continuous) . . . ±3.4 A
($t_w \leq 20$ µs, 10% duty cycle) . . . . ±4.0 A
Logic Supply Voltage, V_{CC} . . . . . 7.0 V
Input Voltage Range,
V_{IN} . . . . . -0.3 V to +7.0 V
Package Power Dissipation,
P_D . . . . . See Graph
Operating Temperature Range,
T_A . . . . . -20°C to +85°C
Junction Temperature, T_J . . . . . +150°C*
Storage Temperature Range,
T_S . . . . . -55°C to +150°C

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

The UDN2961B and UDN2961W are 3.4 A half bridges designed specifically for driving solenoid printheads, stepper motors, and dc motors. The UDN2961B/W consists of a power source driver output, a power sink driver output, a flyback recovery diode, internal current sensing circuitry, and a user-selectable fixed off-time chopper circuit.

The output drivers are capable of sustaining 45 V with continuous currents of ±3.4 A and peak currents of ±4 A permitted. The outputs have been optimized for a low output saturation voltage (typically 2.6 V total source plus sink drops at 3.4 A).

For output current control, load current is internally sensed and limited by chopping the output driver(s) in a user-selectable fixed off-time PWM mode. The maximum output current is determined by the user's selection of a reference voltage. The MODE pin determines whether the current control circuitry will chop in a slow current-decay mode (only the source driver switching) or in a fast current-decay mode (source and sink switching). A user-selectable blanking window prevents false triggering of the current control circuitry during chopping.

The UDN2961B is supplied in a 16-pin dual in-line plastic batwing package with a copper lead-frame and heat sinkable tabs for improved power dissipation capabilities. For higher power dissipation requirements, the UDN2961W is supplied in a 12-pin single in-line power tab package.

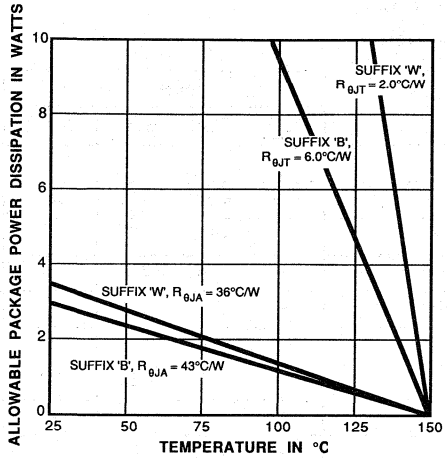
FEATURES

- 3.4 A, 45 V Source and Sink Drivers
- Internal Current Sensing
- User-Selectable Fixed-Off Time PWM Current Control
- Internal Flyback Diode
- Low Output Saturation Voltage
- Chip Enable
- Fast or Slow Current-Decay Modes
- Programmable Blanking Window
- Internal Thermal Shutdown Circuitry

Always order by complete part number:

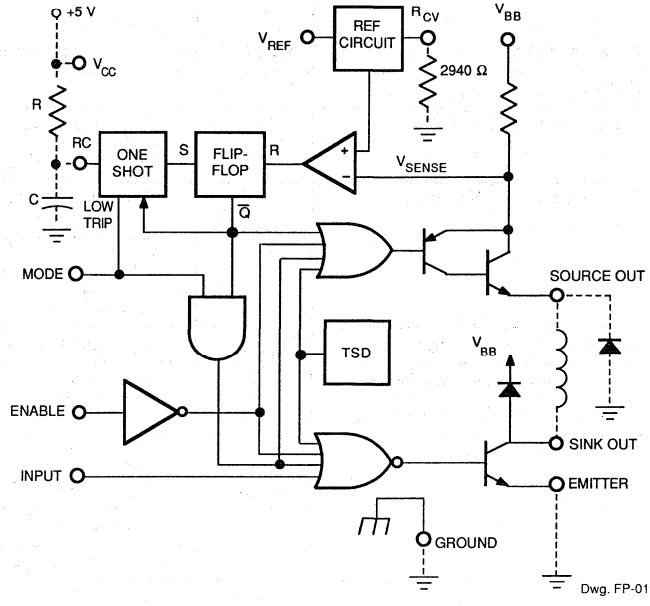
UDN2961B	**16-Pin DIP**
UDN2961W	**12-Pin Power-Tab SIP**

PRELIMINARY



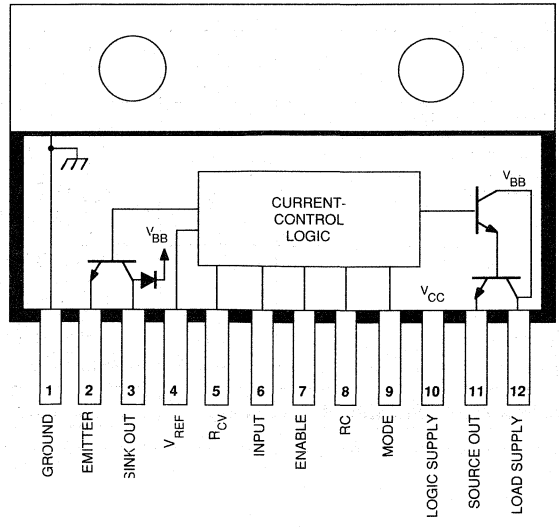
Dwg. GP-032

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-01

UDN2961W



Dwg. PP-03

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, R_{CV} = 2940 Ω (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Output Leakage Current	I_{CEX}	V_{EN} = 0.8 V, V_{SOURCE} = 0 V	—	<-1.0	-100	µA
		V_{EN} = 0.8 V, V_{SINK} = 45 V	—	<1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -3.4 A	—	1.6	2.2	V
		Source Driver, I_{OUT} = -3.0 A	—	1.5	2.0	V
		Sink Driver, I_{OUT} = 3.4 A	—	1.0	1.4	V
		Sink Driver, I_{OUT} = 3.0 A	—	0.9	1.25	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±3.4 A, L = 3 mH	45	—	—	V
Recovery Diode Leakage Current	I_R	V_R = 45 V	—	<1.0	100	µA
Recovery Diode Forward Voltage	V_F	I_F = 3.4 A	—	—	2.0	V
Motor Supply Current	$I_{BB(on)}$	V_{EN} = 2.0 V, V_{IN} = 0.8 V, No Load	—	—	70	mA
	$I_{BB(off)}$	V_{EN} = 0.8 V	—	—	2.0	mA
Output Rise Time	t_r	Source Driver, I_{OUT} = -3.0 A	—	—	600	ns
		Sink Driver, I_{OUT} = 3.0 A	—	—	600	ns
Output Fall Time	t_f	Source Driver, I_{OUT} = -3.0 A	—	—	600	ns
		Sink Driver, I_{OUT} = 3.0 A	—	—	600	ns
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	10	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-1.0	mA
Reference Input Current	I_{REF}	V_{REF} = 5.0 V	—	—	50	µA
Transconductance	I_{TRIP}/V_{REF}	V_{REF} = 0.8 V to 3.4 V	0.9	1.0	1.1	A/V
Logic Supply Current	I_{CC}	V_{EN} = 2.0 V, V_{IN} = 0.8 V, No Load	—	—	160	mA
		V_{EN} = 0.8 V	—	—	15	mA
Turn On Delay	$t_{pd(on)}$	Source Driver	—	—	600	ns
		Sink Driver	—	—	600	ns
Turn Off Delay	$t_{pd(off)}$	Source Driver	—	—	2.0	µs
		Sink Driver	—	—	2.0	µs
Thermal Shutdown Temperature	T_J		—	165	_	°C

Negative current is defined as coming out of (sourcing) the specified device terminal.

APPLICATIONS INFORMATION

The UDN2961B/W is a high current half-bridge designed to drive a number of inductive loads such as printer solenoids, stepper motors, and dc motors. Load current is internally sensed and is controlled by pulse-width modulating (PWM) the output driver(s) in a fixed off-time, variable-frequency format. The peak current level is set by the user's selection of a reference voltage. A slow current-decay mode (chopping only the source driver) or a fast current-decay mode (chopping both the source and sink drivers) can be selected via the MODE pin.

PWM CURRENT CONTROL

A logic low on the MODE pin sets the current-control circuitry into the slow-decay mode. The RS flip-flop is initially set, and both the source driver and the sink driver will be turned ON when the INPUT pin is at a logic low. As current in the load increases, it is sensed by the internal sense resistor until the sense voltage equals the trip voltage of the comparator. At this time, the flip-flop is reset and the source driver is turned OFF. Over the range of V_{REF} = 0.8 V to 3.4 V, the output current trip point transfer function is a direct linear function of the reference voltage:

$$I_{TRIP} = V_{REF}$$

To ensure an accurate chop current level (±10%), an external 2940 Ω ±1% resistor (R_{CV}) is used. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays (typically 1.5 µs). After the source driver turns OFF, the load current decays, circulating through an external ground clamp diode, the load, and the sink transistor. The source driver's OFF time (and therefore the magnitude of the current decrease) is determined by the one-shot's external RC timing components:

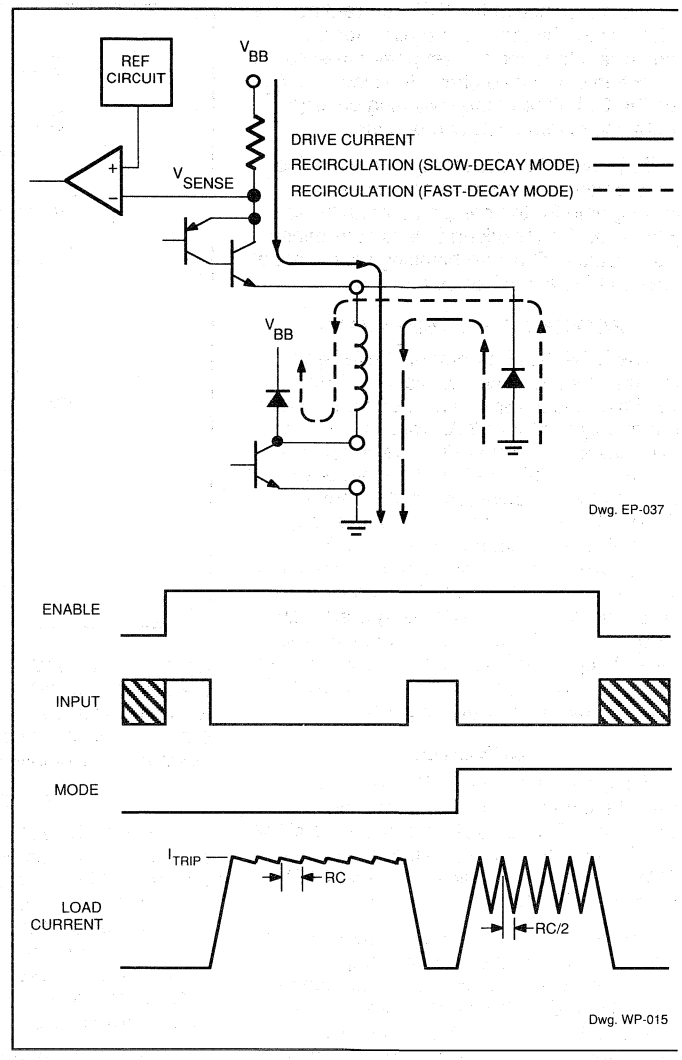
$$t_{OFF} = RC$$

within the range of 20 kΩ to 100 kΩ and 100 pF to 1000 pF. When the one-shot times out, the flip-flop is set again, the source driver is re-enabled, and the load current is again allowed to rise to the set peak value and trip the comparator. This cycle repeats itself, maintaining the average load current at the desired level.

A logic high on the MODE pin sets the current-control circuitry into the fast-decay mode. When the peak current threshold is detected, the flip-flop is reset and both the source driver and the sink driver are turned OFF. Load current quickly decays through the external ground clamp diode, the load, and the internal flyback diode. In the fast-decay mode, the OFF time period will be one-half the time that would be set by the external RC network for the slow-decay mode:

$$t_{OFF} = \frac{RC}{2}$$

The amount of ripple current when chopping in the fast-decay mod will be considerably higher than when chopping in the slow-decay mode.



The frequency of the PWM current control is determined by the time required for the load current to reach the set peak threshold (a function of the load characteristics and V_{BB}) plus the OFF time of the switching driver(s) (set by the external RC components).

To prevent false resetting of the flip-flop due to switching transients and noise, a blanking time for the comparator can be set by the user. The blanking time is determined by the value of C where blanking time is equal to 3600 C (μs and μF or ps and pF).

POWER CONSIDERATIONS

The UDN2961B/W outputs have been optimized for low power dissipation. The sink driver has a maximum saturation voltage drop of only 1.25 V at 3 A, while the source driver has a 2 V drop at -3 A. Device power dissipation is minimized in the slow-decay mode, as the chopping driver (the source driver) is ON for less than 50% of the chop period. When the source driver is OFF during a chop cycle, power is dissipated on chip only by the sink driver; the rest of the power is dissipated through the external ground clamp diode. In the fast-decay mode, the ON time of the chopping drivers (both the source driver and the sink driver) is greater than 50%, and the power dissipation will be greater.

GENERAL

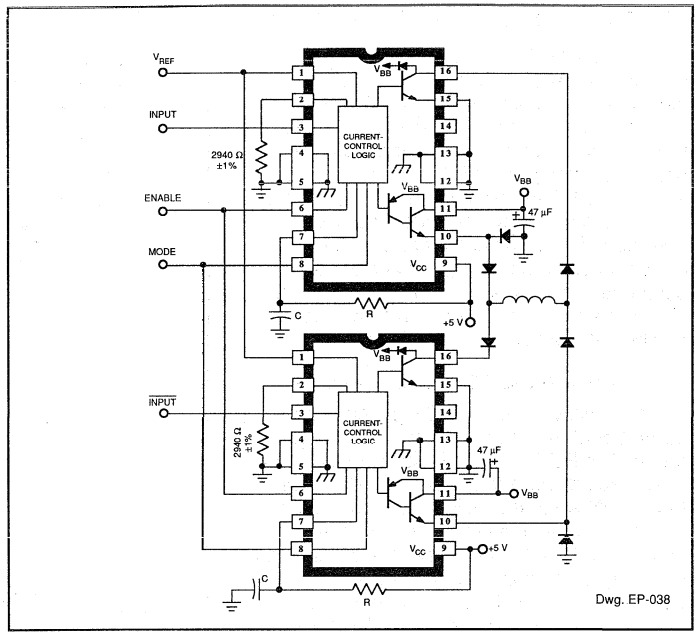
A logic low on the ENABLE pin will prevent the source driver and the sink driver from turning ON, regardless of the state of the INPUT pin or the supply voltages. With the ENABLE pin high, a logic low on the INPUT pin will turn ON the output drivers.

To protect against inductive load voltage transients, an external ground clamp diode is required. A fast-recovery diode is recommended to reduce power dissipation in the UDN2961B/W. The blanking time prevents false triggering of the current sense comparator, which can be caused by the recovery current spike of the ground clamp diode when the chopping source driver turns ON.

The load supply (V_{BB}) should be well decoupled with a capacitor placed as close as possible to the device.

The EMITTER pin should be connected to a high-current power ground.

Thermal shutdown protection circuitry is activated and turns OFF both output drivers at a junction temperature of typically +165°C. It is intended only to protect the device from catastrophic failures due to excessive junction temperatures and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools down to approximately +145°C.



MOTOR DRIVER APPLICATIONS

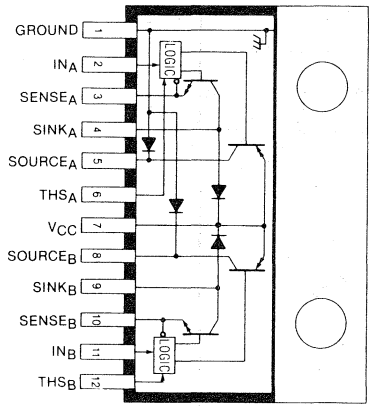
Two UDN2961B/Ws can be cross connected as shown to form a full-bridge driver circuit. Two full-bridge circuits are needed to drive a two-phase bipolar stepper motor. When in a full-bridge configuration, one INPUT signal must be logically inverted from the other INPUT signal to prevent the simultaneous conduction of a source driver from one half-bridge and the sink driver from the other half-bridge. In order to prevent cross-over currents, a turn-ON delay time of 3 μs is needed between the time an INPUT signal for one of the half bridges goes high and the INPUT signal for the other half bridge goes low.

In addition to the two external ground clamp diodes, diodes in series with the load to the SINK OUT are needed in a full-bridge configuration. These series diodes prevent the sink drivers from conducting on the inverse mode, which can occur when the opposite half-bridge ground clamp diode is conducting and forces the sink driver collector below ground.

If fast current decay is used (MODE = logic high) or pulse width modulation of the load-current direction is used, diodes in series with the load to the SOURCE OUT are needed. These series diodes prevent the SOURCE OUT from inverse conducting during the recirculation period and thereby prevent shoot-through currents from occuring as the drivers turn back ON.

2962

DUAL SOLENOID/MOTOR DRIVE
—PULSE-WIDTH MODULATED CURRENT CONTRO



Dwg. No. D-1001

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Supply Voltage, V_{CC} . . . . . **45 V**
Peak Output Current, I_{OUT} . . . . . **±4 A**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to +7.0 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

NOTE: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

Using PWM to minimize power dissipation and maximize load efficiency, the UDN2962W dual driver is recommended for impact printer solenoids and stepper motors. It is comprised of two source/sin driver pairs rated for continuous operation to ±3 A. It can be connecte to drive two independent loads or a single load in the full-bridge configuration. Both drivers include output clamp/flyback diodes, input gain and level shifting, a voltage regulator for single-supply operation, and pulse-width modulated output-current control circuitry. Inputs are compatible with most TTL, DTL, LSTTL, and low-voltage CMOS or PMOS logic.

The peak output current and hysteresis for each source/sink pair is set independently. Output current, threshold voltage, and hysteresis are set by the user's selection of external resistors. At the specified output-current trip level, the source driver turns OFF. The internal clamp diode then allows current to flow without additional input from the power supply. When the lower current trip point is reached, the source driver turns back ON.

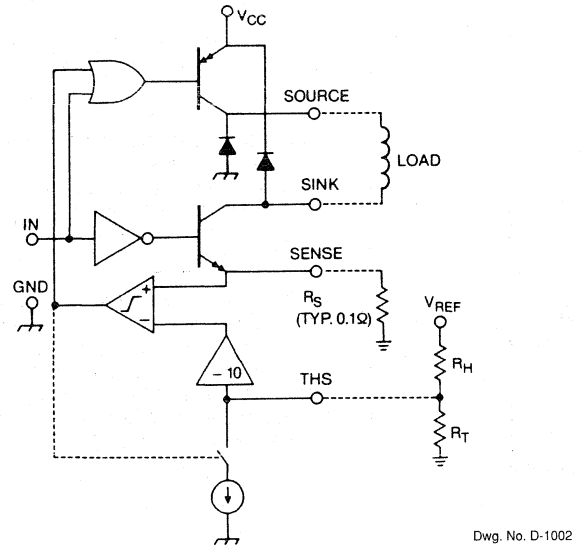
The UDN2962W is in a 12-pin single in-line power tab package. The tab is at ground potential and needs no insulation. For high-currer or high-frequency applications, external heat sinking may be required.

FEATURES

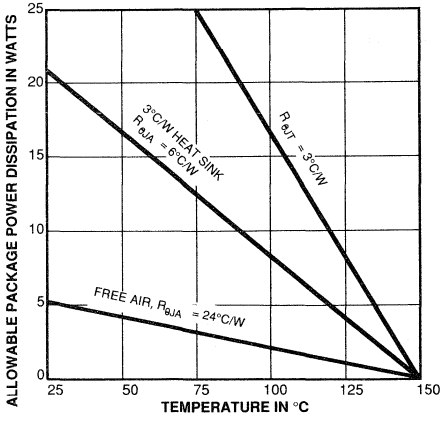
- 4 A Peak Output
- 45 V Min. Sustaining Voltage
- Internal Clamp Diodes
- TTL/PMOS/CMOS Compatible Inputs
- High-Speed Chopper

Always order by complete part number: **UDN2962W** .

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. D-1002



Dwg. GP-012

TRUTH TABLE

V_{IN}	V_{SENSE}	SOURCE DRIVER	SINK DRIVER
High	NA	Off	Off
Low	$<V_{THS}/10$	On	On
Low	$>V_{THS}/10$	Off	On

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{CC} = 45 V, V_{SENSE} = 0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	Operating	20	—	45	V
Output Drivers						
Output Leakage Current	I_{CEX}	V_{IN} = 2.4 V, V_{SOURCE} = 0 V	—	<-1.0	-100	µA
		V_{IN} = 2.4 V, V_{SINK} = 45 V	—	<1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Drivers, I_{LOAD} = 3.0 A	—	2.1	2.3	V
		Source Drivers, I_{LOAD} = 1.0 A	—	1.7	2.0	V
		Sink Drivers, I_{LOAD} = 3.0 A	—	1.7	2.0	V
		Sink Drivers, I_{LOAD} = 1.0 A	—	1.1	1.3	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±3.0 A, L = 3.5 mH	45	—	—	V
Output Current Regulation	ΔI_{OUT}	V_{THS} = 0.6 V to 1.0 V, L = 3.5 mH	—	—	±25	%
		V_{THS} = 1.0 V to 2.0 V, L = 3.5 mH	—	—	±10	%
		V_{THS} = 2.0 V to 5.0 V, L = 3.5 mH	—	—	±5.0	%
Clamp Diode Forward Voltage	V_F	I_F = 3.0 A	—	1.7	2.0	V
Output Rise Time	t_r	I_{LOAD} = 3.0 A, 10% to 90%, Resistive Load	—	0.5	1.0	µs
Output Fall Time	t_f	I_{LOAD} = 3.0 A, 90% to 10%, Resistive Load	—	0.5	1.0	µs
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	1.0	10	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-20	-100	µA
	$I_{THS(ON)}$	$V_{THS} \geq$ 500 mV, $V_{SENSE} \leq V_{THS}/10.5$	—	-2.0	—	µA
	$I_{THS(HYS)}$	$V_{SENSE} \geq V_{THS}/9.5$, V_{THS} = 0.6 V to 5.0 V	140	200	260	µA
V_{THS}/V_{SENSE} Ratio	—	At Trip Point, V_{THS} = 2.0 V to 5.0 V	9.5	10	10.5	—
Supply Current (Total Device)	I_{CC}	V_{IN} = 2.4 V, Outputs OFF	—	8.0	12	mA
		V_{IN} = 0.8 V, Outputs Open	—	25	40	mA
Propagation Delay Time (Resistive Load)	t_{pd}	50% V_{IN} to 50% V_{OUT}, Turn OFF	—	—	2.5	µs
		50% V_{IN} to 50% V_{OUT}, Turn ON	—	—	3.0	µs
		100% V_{SENSE} to 50% V_{OUT}*	—	—	3.0	µs

* Where $V_{SENSE} \geq V_{THS}/9.5$

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

CIRCUIT DESCRIPTION AND APPLICATIONS INFORMATION

The UDN2962W high-current driver is intended for use as a free-running, pulse-width modulated solenoid driver.

Circuit Description. In operation, the source and sink drivers are both turned ON by a low level at the input. The load current rises with time as a function of the load inductance, total circuit resistance, and supply voltage and is sensed by the external sense resistor (R_S). When the load current reaches the trip point (I_{TRIP}), the comparator output goes high and turns OFF the source driver. The actual load current will peak slightly higher than I_{TRIP} because of the internal logic and switching delays.

After the source driver is turned OFF, the load current continues to circulate through the sink driver and an internal ground clamp diode. The rate of current decay is a function of the load inductance and total circuit resistance.

An internal constant current sink reduces the trip point (hysteresis) until the decaying load current reaches the lower threshold, when the comparator output goes low and the source driver is again turned ON. Load current is again allowed to rise to the trip point and the cycle repeats.

Maximum load current and hysteresis is determined by the user.

Determining Maximum Load Current and Hysteresis. Trip current (I_{TRIP}) is determined as a function of resistance R_S and the threshold voltage, V_{THS}:

$$I_{TRIP} = \frac{V_{THS}}{10\ R_S}$$

where $V_{THS} = 10 \bullet V_{SENSE} = 0.6$ V to 5.0 V.

Hysteresis percentage (H) is determined by resistance R_H and is independent of the load current:

$$H = \frac{R_H}{50 \bullet V_{REF}}$$

The chopping frequency is asynchronous and a function of the system and circuit parameters, including load inductance, supply voltage, hysteresis setting, and switching speed of the driver.

Resistance R_T is determined as:

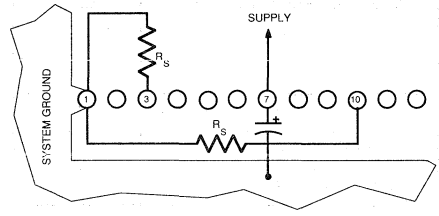
$$R_T = \frac{R_H V_{THS}}{V_{REF} - V_{THS}}$$

Note that if $V_{THS} = V_{REF}$, then $R_T = \infty$.

Circuit Layout. To prevent interaction between channels, each of the two high-level power ground returns (the low side of the sense resistors) must be returned independently to the low-level signal ground (pin 1). The circuit common (pin 1) can then be routed to the system ground.

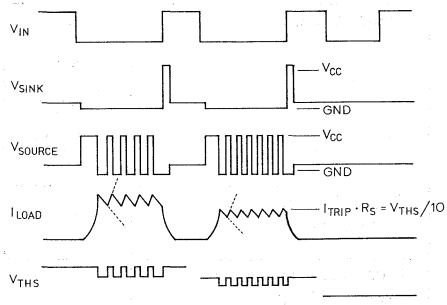
The printed wiring board should utilize a heavy ground plane. For optimum performance, the driver should be soldered directly into the board.

The power supply (V_{CC}) should be decoupled with an electrolytic capacitor (≥10 µF) as close as possible to pin 7.



Dwg. OP-001

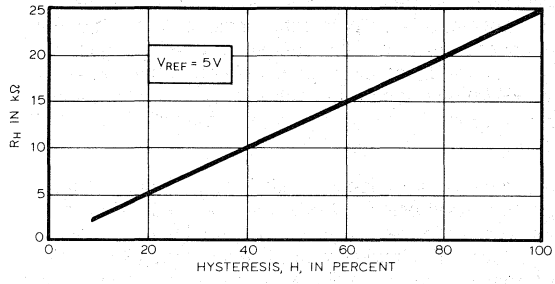
TYPICAL WAVESHAPES



Dwg. WP-006

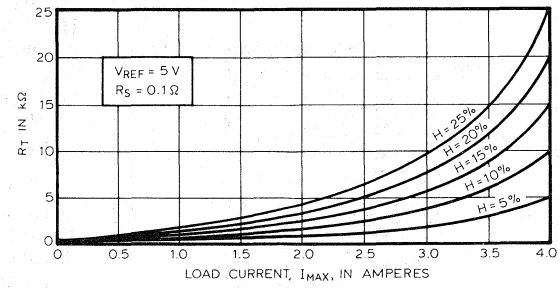
APPLICATIONS INFORMATION

RESISTOR R_H VALUE AS A FUNCTION OF HYSTERESIS



Dwg. No. A-12,417

RESISTOR R_T VALUE AS A FUNCTION OF PEAK LOAD CURRENT



Dwg. No. A-12,416

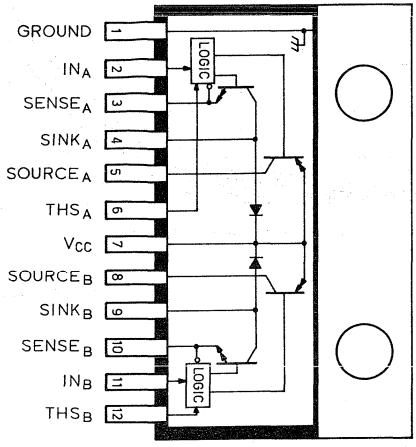
MOUNTING POWER TAB DEVICES

Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. Brute force mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

2966

DUAL SOLENOID DRIVER WITH PWM CURRENT CONTROL



Dwg. PP-024

Rated for continuous operation to 4.8 A and 65 V per channel, the UDN2966W is designed to drive impact printer solenoids. Each of the two independent driver pairs in the UDN2966W include input gain and level shifting, a voltage regulator for single-supply operation, pulse-width modulated (PWM) output-current control, a flyback diode, and on-chip thermal protection. The inputs are compatible with TTL, LSTTL, and low-voltage CMOS or PMOS logic.

The PWM mode helps maximize load efficiency. Output current, threshold voltage, and hysteresis are set by the user's selection of external resistors. At the specified output current trip level, the source driver turns OFF, allowing the load current to decay through the sink driver and an external ground clamp diode. When the lower current trip point is reached, the source driver is turned back ON.

For maximum power-handling capability, the UDN2966W is supplied in a 12-pin single in-line power tab package. An external heat sink is required for most high-current applications. The tab is at ground potential and needs no insulation.

FEATURES

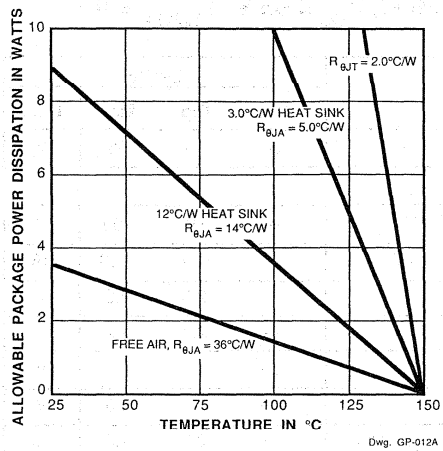
- 5 A Peak Output Current
- 65 V Output Sustaining Voltage
- Internal Flyback Diodes
- Internal Current Control
- Internal Thermal Shutdown Circuitry

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

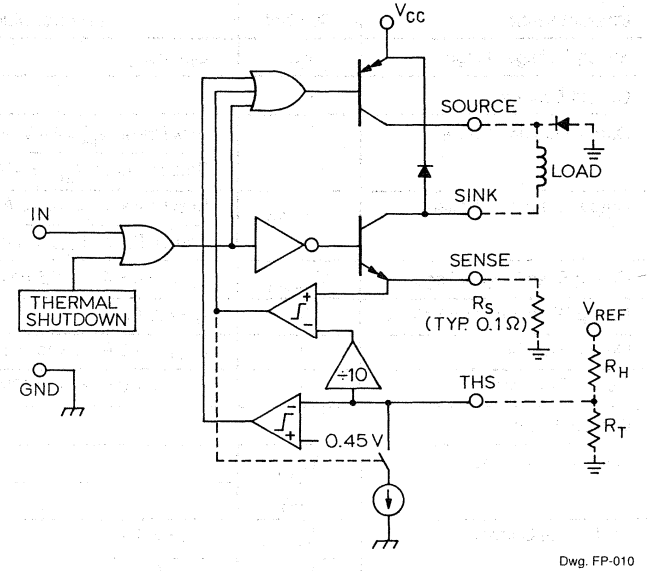
Supply Voltage, V_{CC} . . . . . **65 V**
Peak Output Current, I_{OUT} . . . . . **±5.0 A**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to +7.0 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak output current or a junction temperature of +150°C.

Always order by complete part number: **UDN2966W** .



FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



TRUTH TABLE

V_{IN}	V_{THS}	V_{SENSE}	Source Driver	Sink Driver	Function
High	NA	NA	OFF	OFF	OFF
Low	<0.4 V	NA	OFF	ON	OFF
Low	0.6 V to 5.0 V	$<V_{THS}/10$	ON	ON	ON
Low	0.6 V to 5.0 V	$>V_{THS}/10$	OFF	ON	Chopping

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{CC} = 65 V, V_{SENSE} = 0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max	Units
Supply Voltage Range	V_{CC}	Operating	20	—	65	V
Output Drivers						
Output Leakage Current	I_{CEX}	Sink Driver, V_{IN} = 2.4 V, V_{OUT} = 65 V	—	<10	100	µA
		Source Driver, V_{IN} = 2.4 V, V_{OUT} = 0 V	—	<-10	-100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Sink Driver, I_{OUT} = +4.8 A	—	2.3	2.5	V
		Source Driver, I_{OUT} = -4.8 A	—	2.7	2.9	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±4.8 A, L = 3.5 mH	65	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 4.8 A	—	—	3.0	V
Output Rise Time	t_r	I_{LOAD} = 4.0 A, 10% to 90%, Resistive Load	—	0.5	1.0	µs
Output Fall Time	t_f	I_{LOAD} = 4.0 A, 90% to 10%, Resistive Load	—	0.5	1.0	µs
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	-150	-200	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-150	-200	µA
	$I_{THS(OFF)}$	$V_{THS} \leq$ 400 mV	—	-60	—	µA
	$I_{THS(ON)}$	$V_{THS} \geq$ 500 mV, $V_{SENSE} \leq V_{THS}$/ 10.5	—	-2.0	—	µA
	$I_{THS(HYS)}$	$V_{SENSE} \geq V_{THS}$/9.5, V_{THS} = 0.6 V to 5.0 V	140	200	260	µA
Output Disable Voltage	$V_{THS(OFF)}$		—	—	400	mV
V_{THS}/V_{SENSE} Ratio	—	At Trip Point, V_{THS} = 2.0 V to 5.0 V	9.5	10	10.5	—
Supply Current (Total Device)	I_{CC}	V_{IN} = 2.4 V, Outputs OFF	—	10	15	mA
		V_{IN} = 0.8 V, Outputs Open	—	28	32	mA
Propagation Delay Time (Resistive Load)	t_{pd}	50% V_{IN} to 50% V_{OUT}, Turn OFF	—	—	3.0	µs
		50% V_{IN} to 50% V_{OUT}, Turn ON	—	—	3.0	µs
		100% V_{SENSE} to 50% V_{OUT} *	—	—	3.0	µs
Thermal Shutdown Temp.	T_J		—	175	—	°C

Typical Data is for design information only.
Negative current is defined as coming out of (sourcing) the specified device pin.
*Where $V_{SENSE} \geq V_{THS}$/9.5

2966
DUAL SOLENOID DRIVER WITH PWM CURRENT CONTROL

CIRCUIT DESCRIPTION AND APPLICATIONS INFORMATION

The UDN2966W high-current driver is intended for use as a free-running, pulse-width modulated solenoid driver.

Circuit Description. In operation, the source and sink drivers are both turned ON by a low level at the input. The load current rises with time as a function of the load inductance, total circuit resistance, and supply voltage and is sensed by the external sense resistor (R_S). When the load current reaches the trip point (I_{TRIP}), the comparator output goes high and turns OFF the source driver. The actual load current will peak slightly higher than I_{TRIP} because of the internal logic and switching delays.

After the source driver is turned OFF, the load current continues to circulate through the sink driver and an external ground clamp diode. The rate of current decay is a function of the load inductance and total circuit resistance.

An internal constant current sink reduces the trip point (hysteresis) until the decaying load current reaches the lower threshold, when the comparator output goes low and the source driver is again turned ON. Load current is again allowed to rise to the trip point and the cycle repeats.

Maximum load current and hysteresis is determined by the user.

Determining Maximum Load Current and Hysteresis. Trip current (I_{TRIP}) is determined as a function of resistance R_S and the threshold voltage, V_{THS}:

$$I_{TRIP} = \frac{V_{THS}}{10\ R_S}$$

where $V_{THS} = 10 \bullet V_{SENSE} = 0.6$ V to 5.0 V.

Pulling V_{THS} down to less than 0.4 V disables the source driver, turning the load OFF. This method of turn-OFF produces a relatively long current decay as compared with switching the input. When switching the input, both the source and the sink driver are turned OFF, producing a fast current decay.

Hysteresis percentage (H) is determined by resistance R_H and is independent of the load current:

$$H = \frac{R_H}{50 \bullet V_{REF}}$$

The chopping frequency is asynchronous and a function of the system and circuit parameters, including load inductance, supply voltage, hysteresis setting, and switching speed of the driver.

Resistance R_T is determined as:

$$R_T = \frac{R_H\ V_{THS}}{V_{REF} - V_{THS}}$$

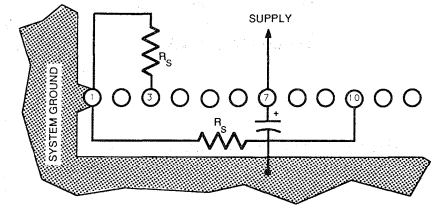
Note that if $V_{THS} = V_{REF}$, then $R_T = \infty$.

External ground clamp power diodes are required at the source outputs (pins 5 and 8) for proper driver operation. To minimize power dissipation due to switching losses, these diodes should have a fast recovery time.

Circuit Layout. To prevent interaction between channels, each of the two high-level power ground returns (the low side of the sense resistors) must be returned independently to the low-level signal ground (pin 1). The circuit common (pin 1) can then be routed to the system ground.

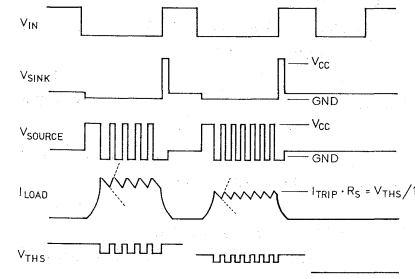
The printed wiring board should utilize a heavy ground plane. For optimum performance, the driver should be soldered directly into the board.

The power supply (V_{CC}) should be decoupled with an electrolytic capacitor (≥10 μF) as close as possible to pin 7.



Dwg. OP-001

TYPICAL WAVESHAPES

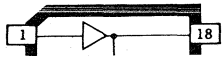


Dwg. WP-006

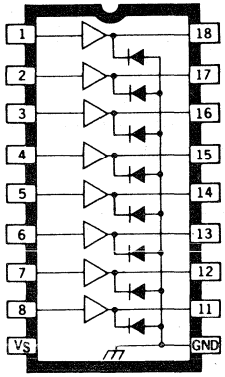
2981 THRU 2984

8-CHANNEL SOURCE DRIVERS

UDN2982/84LW



UDN2981-84A



Dwg. No. A-10, 243

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage Range, V_{CE}
(UDN2981A & UDN2982A/LW) ..... **5 V to 50 V**
(UDN2983A & UDN2984A/LW) ..... **35 V to 80 V**
Input Voltage, V_{IN}
(UDN2981A & UDN2983A) ..... **15 V**
(UDN2982A/LW & UDN2984A/LW) ..... **20 V**
Output Current, I_{OUT} ..... **-500 mA**
Package Power Dissipation, P_D ..... **See Graph**
Operating Temperature Range, T_A ..... **-20°C to +85°C**
Storage Temperature Range, T_S ..... **-55°C to +150°C**

Note that the UDN2982/84A (dual in-line package) and UDN2982/84LW (small-outline IC package), respectively, are electrically identical and share a common pin number assignment.

Recommended for applications requiring separate logic and load grounds, load supply voltages to 80 V, and load currents to 500 mA, the UDN2981A through UDN2984A/LW 8-channel source drivers are used as interfaces between standard low-power digital logic and relays, solenoids, stepping motors, magnetic print hammers, and LEDs.

The UDN2981A and UDN2983A drivers are for use with 5 V logic systems–TTL, Schottky TTL, DTL, and 5 V CMOS. The UDN2982A/LW and UDN2984A/LW drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. The UDN2981A and UDN2982A/LW will withstand a maximum output OFF voltage of 50 V, while the UDN2983A and UDN2984A/LW will withstand an output voltage of 80 V. In all cases, the output is switched ON by an active high input level. All devices incorporate input current limiting resistors and output transient suppression diodes.

The suffix 'A' (all devices) indicates an 18-lead plastic dual in-line package with copper lead frame for optimum power dissipation. Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of 15 V.

The suffix 'LW' (UDN2982LW and UDN2984LW only) indicates a surface-mountable wide-body SOIC package.

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V
- DIP or SOIC Packaging

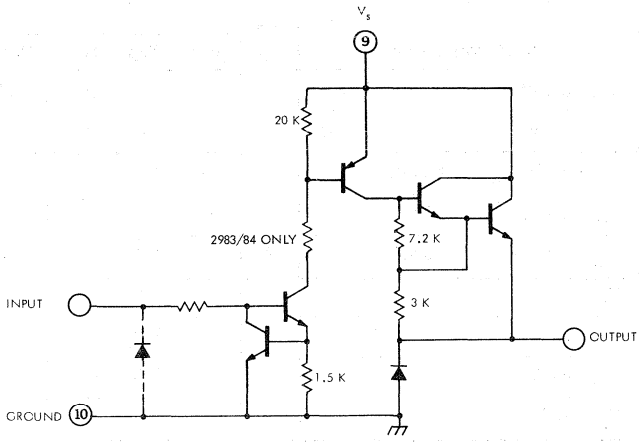
Always order by complete part number, e.g., **UDN2981A**.
Note that all devices are not available in both package types.

ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise specified).

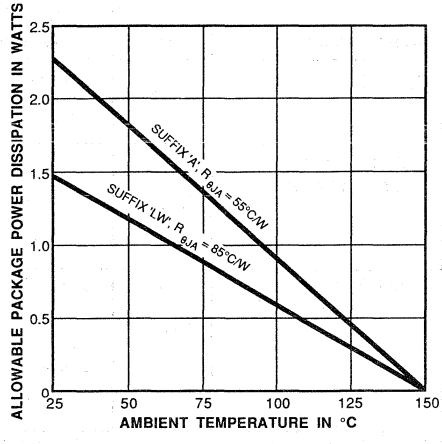
Characteristic	Symbol	Applicable Devices	Test Conditions	Test Fig.	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	UDN2981/82†	V_{IN} = 0.4 V*, V_S = 50 V, T_A = +70°C	1	—	—	200	µA
		UDN2983/84†	V_{IN} = 0.4 V*, V_S = 80 V, T_A = +70°C	1	—	—	200	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	V_{IN} = 2.4 V, I_{OUT} = -100 mA	2	—	1.6	1.8	V
			V_{IN} = 2.4 V, I_{OUT} = -225 mA	2	—	1.7	1.9	V
			V_{IN} = 2.4 V, I_{OUT} = -350 mA	2	—	1.8	2.0	V
Input Current	$I_{IN(ON)}$	UDN2981/83A‡	V_{IN} = 2.4 V	3	—	140	200	µA
			V_{IN} = 3.85 V	3	—	310	450	µA
		UDN2982/84†	V_{IN} = 2.4 V	3	—	140	200	µA
			V_{IN} = 12 V	3	—	1.25	1.93	mA
Output Source Current	I_{OUT}	UDN2981/83A	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	-350	—	—	mA
		UDN2982/84†	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	-350	—	—	mA
Supply Current (Outputs Open)	I_S	UDN2981/82†	V_{IN} = 2.4 V*, V_S = 50 V	4	—	—	10	mA
		UDN2983/84†	V_{IN} = 2.4 V*, V_S = 80 V	4	—	—	10	mA
Clamp Diode Leakage Current	I_R	UDN2981/82†	V_R = 50 V, V_{IN} = 0.4 V*	5	—	—	50	µA
		UDN2983/84†	V_R = 80 V, V_{IN} = 0.4 V*	5	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All	I_F = 350 mA	6	—	1.5	2.0	V
Turn-On Delay	t_{ON}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V	—	—	1.0	2.0	µs
Turn-Off Delay	t_{OFF}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V	—	—	5.0	10	µs

NOTES: Negative current is defined as coming out of (sourcing) the specified device terminal.
* All inputs simultaneously.
† Complete part number includes suffix to identify package style: A = DIP, LW = SOIC.

ONE OF EIGHT DRIVERS



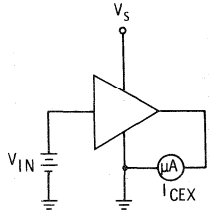
Dwg. No. A-10,242B



Dwg. GP-018A

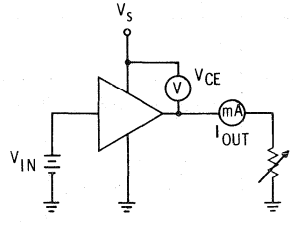
TEST FIGURES

FIGURE 1



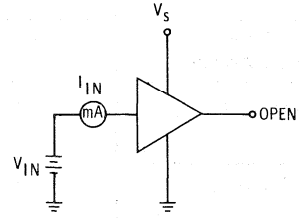
Dwg. No. A-11,083

FIGURE 2



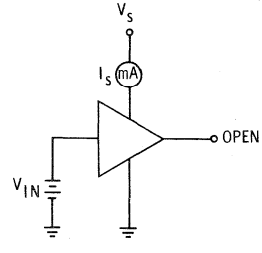
Dwg. No. A-11,084

FIGURE 3



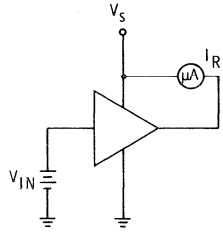
Dwg. No. A-11,085

FIGURE 4



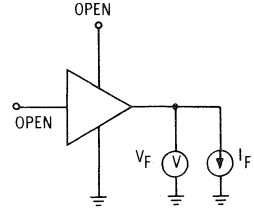
Dwg. No. A-11,086

FIGURE 5



Dwg. No. A-11,087

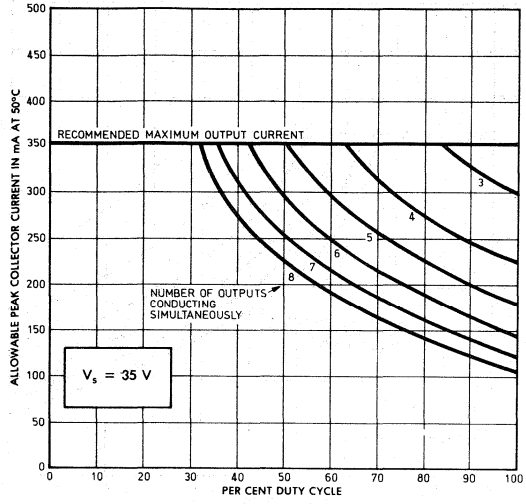
FIGURE 6



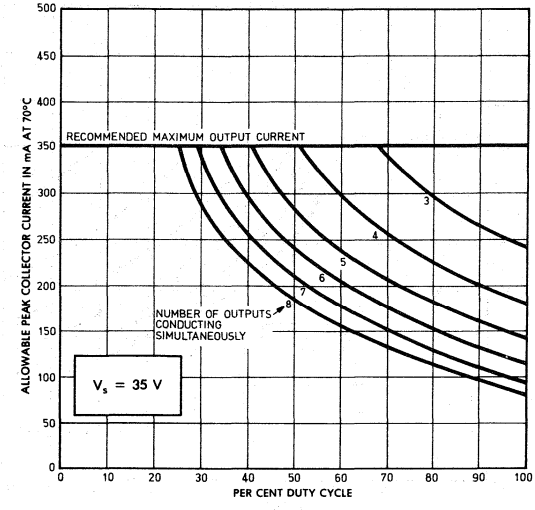
Dwg. No. A-11,088

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

SERIES UDN2980A

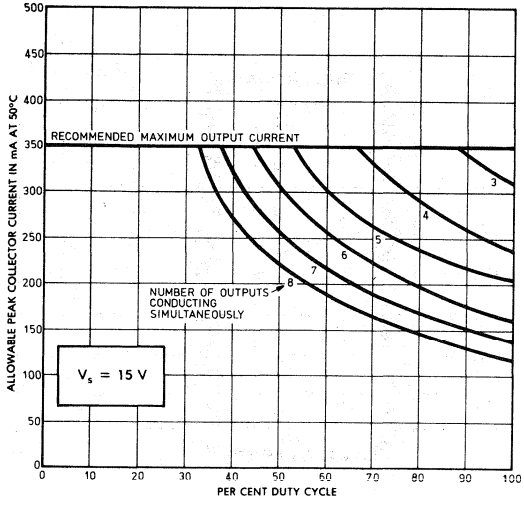


Dwg. No. A-11,106B



Dwg. No. A-11,111B

SERIES UDN2981/82A



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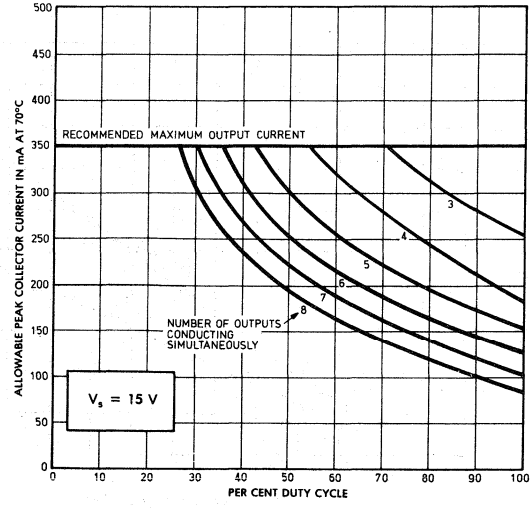
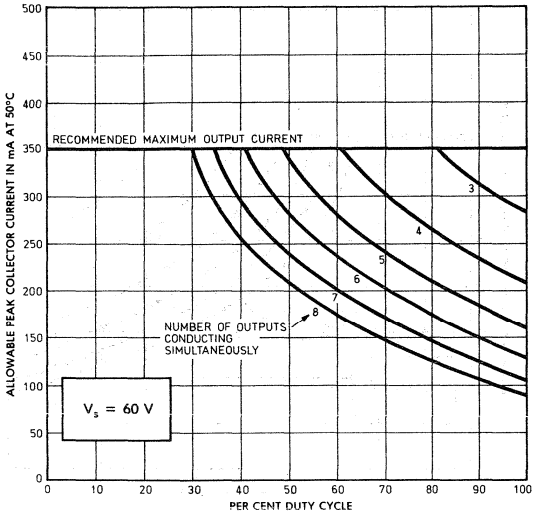


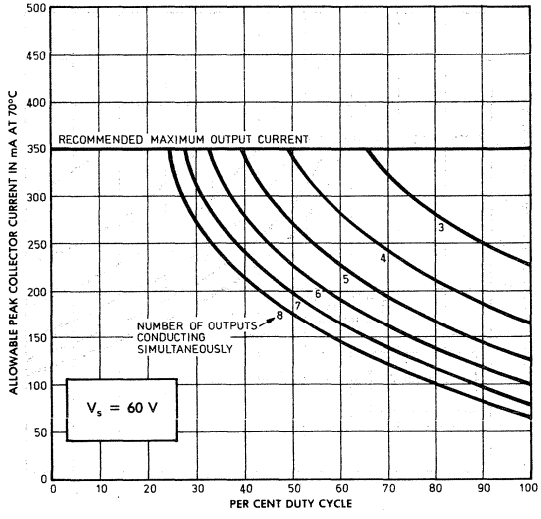
Dwg. No. A-11,108B

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

SERIES UDN2983/84A

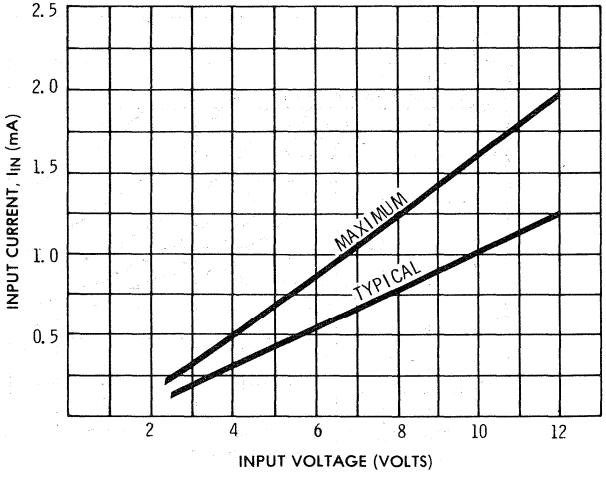


Dwg. No. A-11,109B



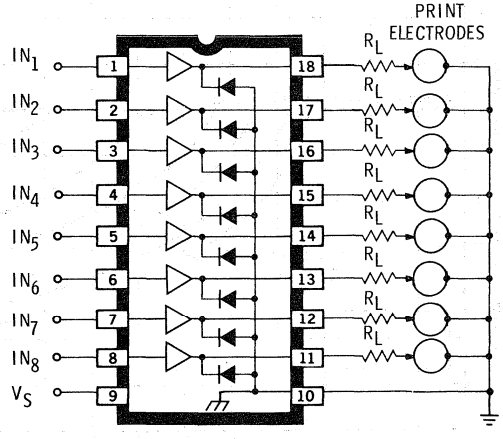
Dwg. No. A-11,110B

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



Dwg. No. A-11,115B

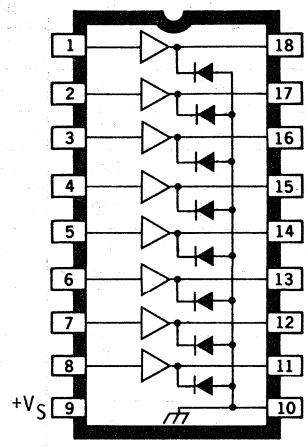
TYPICAL ELECTROSENSITIVE PRINTER APPLICATION



Dwg. No. A-11,113A

2985

8-CHANNEL SOURCE DRIVER



Dwg. No. A-10,243

Recommended for applications requiring separate logic and load grounds, load supply voltages to 30 V, and load currents to 250 mA, the UDN2985A source driver is used as an interface between standard low-power digital logic and LEDs, relays and solenoids. The outputs feature saturated transistors for low collector-emitter saturation voltages.

The UDN2985A driver is for use with 5 V logic systems—TTL, Schottky TTL, DTL, and CMOS. This device has a minimum output breakdown rating of 30 V with a minimum output sustaining voltage of 15 V. The output is switched ON by an active high input level.

Under normal operating conditions, this device can source up to 120 mA for each of the eight outputs at an ambient temperature of 75°C and a supply voltage of 15 V. It incorporates input current-limiting resistors and output transient suppression diodes.

The UDN2985A source driver is supplied in an 18-lead dual in-line package. All inputs are on one side of the package, output pins on the other, to simplify printed wiring board layout.

FEATURES

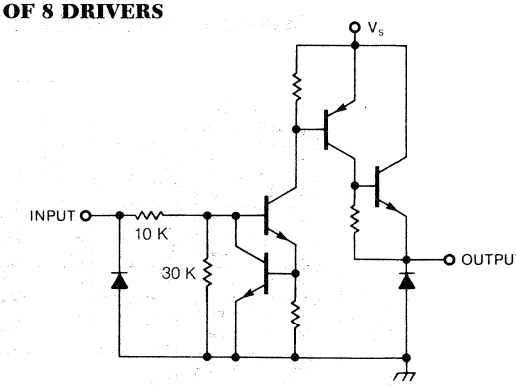
- TTL, DTL, or CMOS Compatible Inputs
- 250 mA Output Source Current Capability
- Output Transient-Suppression Diodes
- 30 V Minimum Output Breakdown Voltage
- Low Output-Saturation Voltage

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Driver Supply Voltage, V_S . . . . . **30 V**
Continuous Output Current,
I_{OUT} . . . . . **-250 mA**
Input Voltage, V_{IN} . . . . . **-20 V**
Package Power Dissipation,
P_D . . . . . **2.2 W***
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*Derate at the rate of 18 mW/°C above T_A = 25°C

PARTIAL SCHEMATIC DIAGRAM
1 OF 8 DRIVERS



Dwg. No. DS-1013

Always order by complete part number: **UDN2985A** .

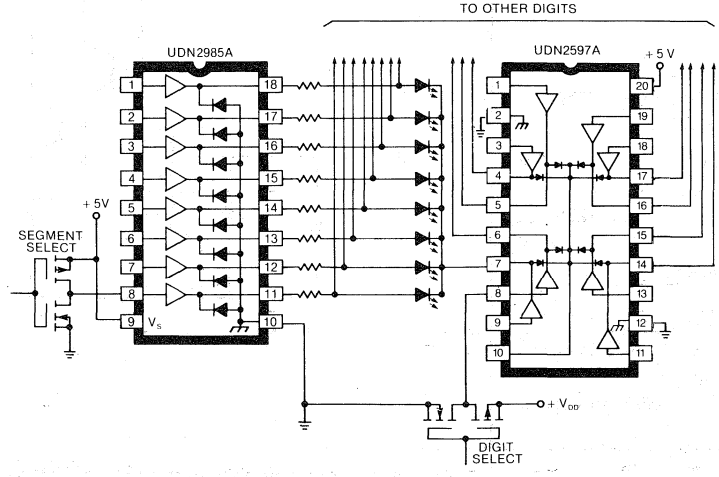
2985
8-CHANNEL SOURCE DRIVER

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_S = 30 V (unless otherwise noted).

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{IN} = 0.4 V, V_{OUT} = 0 V	—	<-1.0	-100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = -120 mA, L = 3 mH	15	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = 2.4, I_{OUT} = -60 mA	—	0.8	1.1	V
		V_{IN} = 2.4, I_{OUT} = -120 mA	—	0.9	1.2	V
Input Current Voltage	$I_{IN(ON)}$	V_{IN} = 2.4 V	—	90	225	µA
		V_{IN} = 5.0 V	—	280	650	µA
	$I_{IN(OFF)}$	V_{IN} = 0.4 V	—	10	15	µA
Supply Current (outputs open)	I_S	V_S = 30 V, V_{IN} = 2.4 V	—	10	15	mA
Clamp Diode Leakage Current	I_R	V_R = 30 V, T_A = 70°C	—	<1.0	50	µA
Clamp Diode Foward Voltage	V_F	I_F = 120 mA	—	1.1	2.0	V
Turn-On Delay	t_{ON}		—	0.5	1.0	µs
Turn-Off Delay	t_{OFF}		—	5.0	10	µs

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

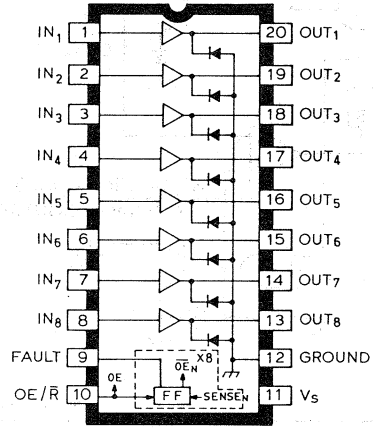
COMMON-CATHODE LED DRIVER



Dwg. No. DS-1014

2987

8-CHANNEL SOURCE DRIVER WITH OVER-CURRENT PROTECTION



Dwg. No. A-13,285

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Driver Supply Voltage, V_S . . . . . **35 V**
Output Sustaining Voltage, $V_{CE(sus)}$ . . . . **35 V**
Continuous Output Current, I_{OUT} . . . . . **-500 mA***
FAULT Output Voltage, V_{CE} . . . . . **35 V**
FAULT Output Current, I_C . . . . . **30 mA**
Input Voltage, V_{IN} . . . . . **15 V**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

* Outputs are disabled at approximately -500 mA per driver.

Providing over-current protection for each of its eight sourcing outputs, the UDN2987A driver is used as an interface between standard low-level logic and relays, motors, solenoids, LEDs, and incandescent lamps. The device includes thermal shutdown and output transient protection/clamp diodes for use with sustaining voltages to 35 V.

In this driver, each channel includes a latch to turn OFF that channel if the maximum channel current is exceeded. All channels are disabled if the thermal shutdown is activated. A common FAULT output is used to indicate either chip thermal shutdown or any over-current condition. All outputs are enabled by pulling the common OE/R input high. When OE/R is low, all outputs are inhibited and the eight latches are reset. The UDN2987A is supplied in a 20-lead dual in-line plastic package.

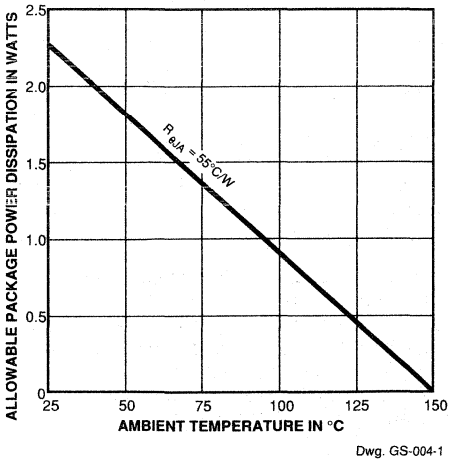
Under normal operating conditions, each of eight outputs will source in excess of 100 mA continuously at an ambient temperature of 25°C and a supply of 35 V. The over-current fault circuit will protect the device from short-circuits to ground with supply voltages of up to 35 V.

The inputs are compatible with 5 V and 12 V logic systems—TTL, Schottky TTL, DTL, PMOS, and CMOS. In all cases, the output is switched ON by an active high input level.

FEATURES

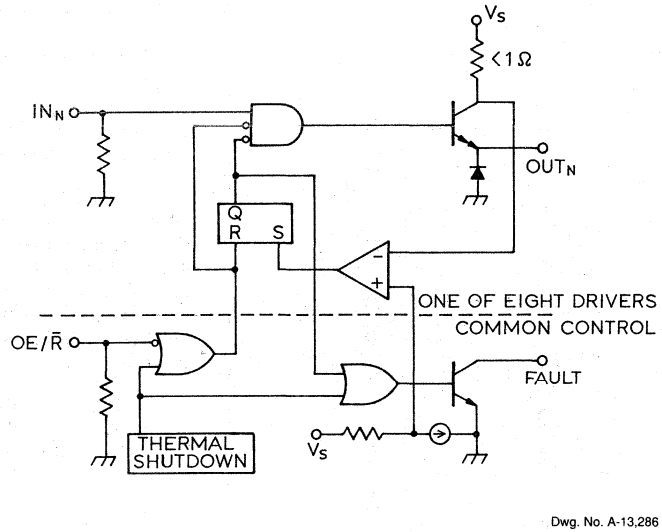
- 350 mA Output Source Current
- Over-Current Protected
- Internal Ground Clamp Diodes
- Output Breakdown Voltage 35 V, Minimum
- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Internal Thermal Shutdown

Always order by complete part number: **UDN2987A** .



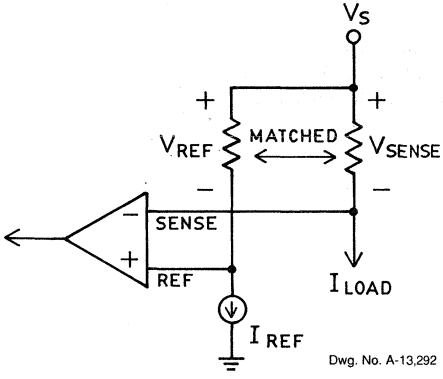
Dwg. GS-004-1

FUNCTIONAL BLOCK DIAGRAM



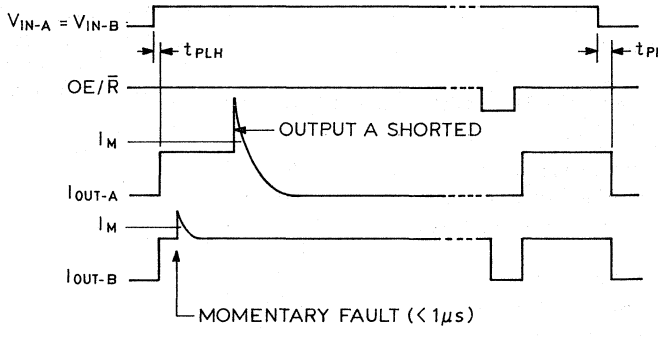
Dwg. No. A-13,286

OVER-CURRENT FAULT SENSE



Dwg. No. A-13,292

OUTPUT CURRENT WAVESHAPES



Dwg. No. A-13,293

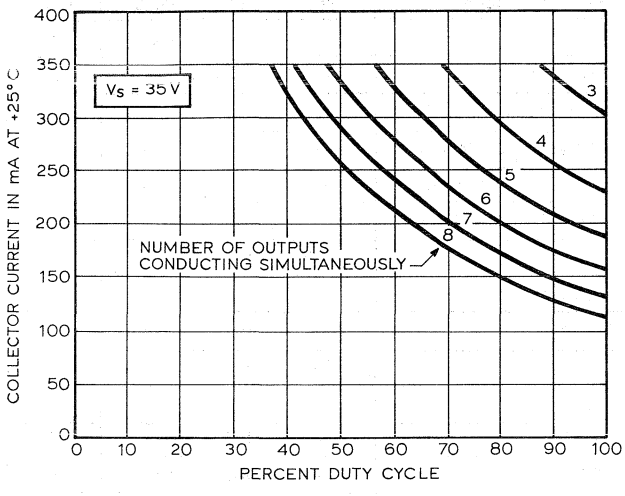
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{OE} = 2.4 V, V_S = 35 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Functional Supply Range	V_S		7.0	—	35	V
Output Leakage Current	I_{CEX}	V_{IN} = 0.4 V*	—	<-5.0	-200	µA
Output Sustaining Voltage	$V_{OUT(sus)}$	I_{OUT} = -350 mA, L = 2.0 mH	35	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{IN} = 2.4 V, I_{OUT} = -100 mA	—	1.6	1.8	V
		V_{IN} = 2.4 V, I_{OUT} = -225 mA	—	1.7	1.9	V
		V_{IN} = 2.4 V, I_{OUT} = -350 mA	—	1.8	2.0	V
Channel Shutdown Threshold	I_M	V_{IN} = 2.4 V	-400	-500	—	mA
FAULT Leakage Current	I_{CEX}	V_{CC} = 35 V	—	<1.0	100	µA
FAULT Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 mA	—	0.3	0.8	V
Input Voltage	$V_{IN(ON)}$		2.4	—	—	V
	$V_{IN(OFF)}$		—	—	0.4	V
Input Current	$I_{IN(ON)}$	V_{IN} = 2.4 V	—	125	170	µA
		V_{IN} = 5.0 V	—	840	1020	µA
		V_{IN} = 12 V	—	1500	1800	µA
	$I_{IN(OFF)}$	V_{IN} = 0.4 V	—	—	15	µA
Clamp Diode Leakage Current	I_R	V_R = 35 V, T_A = 70°C	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.5	1.8	V
Supply Current	$I_{S(ON)}$	V_{IN} = 2.4 V*, Outputs Open	—	13	18	mA
	$I_{S(OFF)}$	V_{IN} = 0.4 V*	—	8.0	12	mA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Hysteresis	ΔT_J		—	15	—	°C
Propagation Delay Time	t_{PLH}	R_L = 100Ω	—	0.3	0.6	µs
	t_{PHL}	R_L = 100Ω	—	2.0	4.0	µs
Dead Time	t_d		—	1.0	—	µs

*All inputs simultaneously.

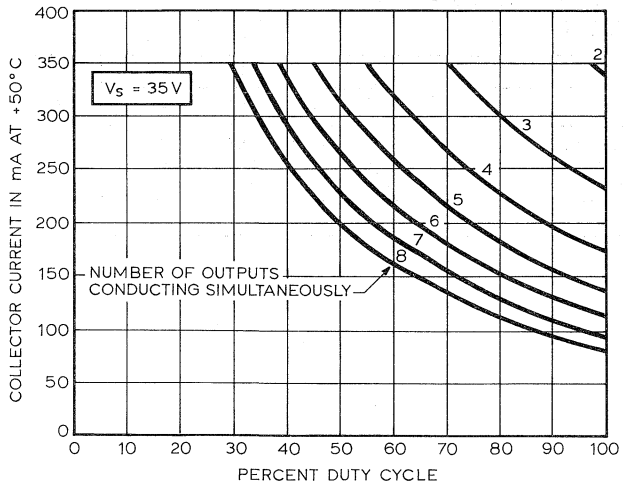
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

AT +25°C



Dwg. No. A-13,288

AT +50°C



Dwg. No. A-13,289

APPLICATIONS INFORMATION AND CIRCUIT DESCRIPTION

As with all power integrated circuits, the UDN2987A has a maximum allowable output current rating. The 500 mA rating does not imply that operation at that value is permitted or even obtainable. The channel output current trip point is specified as -400 mA, minimum; therefore, attempted operation at current levels greater than -400 mA may cause a fault indication and channel shutdown. The device is tested at a maximum of -350 mA and that is the recommended maximum output current per driver. It provides protection for current overloads or shorted loads up to 35 V.

All outputs are enabled by pulling the OE/R input high. When OE/R is low or allowed to float (internal pull-down), all outputs are inhibited and the latches are reset. Note that the RESET pulse duration (OE/R low) should be at least 1 μs. This will ensure safe operation under attempted RESET conditions with a shorted load. The latches are also reset during power-up, regardless of the state of the OE/R input.

The load current causes a small voltage drop across the internal low-value sense resistor. This voltage is compared to the voltage drop across a reference resistor with a constant current. The two resistors are matched to eliminate errors due to manufacturing tolerances or temperature effects. Each channel includes a comparator and its own latch. An over-current fault ($V_{SENSE} > V_{REF}$) will set the affected latch and shut down only that channel. All other channels will continue to operate normally. The latch includes a 1 μs delay (t_d) to prevent unwanted triggering due to crossover currents generated when switching inductive loads. For an abrupt short circuit, the delay and output switching times will allow a brief, permissable current in excess of the trip current before the output driver is turned OFF.

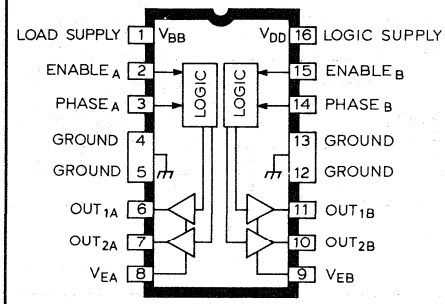
A common thermal shutdown disables all outputs if the chip temperature exceeds +165°C. At thermal shutdown, all latches are reset. The outputs are disabled until the chip cools down to about +150°C (thermal hysteresis).

A common open-collector FAULT output is used to indicate any channel over-current condition or chip thermal shutdown.

2993

DUAL H-BRIDGE MOTOR DRIVERS

UDN2993B



Dwg. No. A-12,455

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Load Supply Voltage, V_{BB} . . . . . **40 V**
Logic Supply Voltage, V_{DD} . . . . . **7.0 V**
Logic Input Voltage Range, V_{PHASE} or V_{ENABLE} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Output Current, I_{OUT} . . . . . **±600 mA**
Sink Driver Emitter Voltage, V_E . . . . . **1.5 V**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

IMPORTANT: Load supply voltage must never be applied without logic supply voltage present.

NOTE: Output current rating may be limited by chopping frequency, ambient temperature, airflow, and heat sinking. Under any set of conditions, do not exceed the specified maximum current and a junction temperature of +150°C.

Brushless dc or bipolar stepper motors to 40 V and 500 mA per phase are economically driven with the UDN2993B and UDN2993LB dual H-bridge drivers. Each pair of full-bridge drivers has separate input level shifting, internal logic, source and sink drivers in an H-bridge configuration, and internal clamp diodes. Monolithic, space-saving construction offers reliability unobtainable with discrete components.

Except for supply voltages, the two H-bridges are independent. The ENABLE function is provided for each bridge to allow pulse-width (chopper) modulation with the use of external choppers. The chopper-drive mode is characterized by low power-dissipation levels and maximum efficiency. A PHASE input to each bridge determines load-current direction. In addition, the emitters from each bridge are externally available to allow the addition of current-sensing circuitry. Both devices provide an internally generated dead-time to prevent crossover currents during changes in load-current phase.

These devices are packaged in plastic DIPs (suffix B) or surface-mountable wide-body SOICs (suffix LB) with copper lead frames for optimum power dissipation without heat sinks. The lead configurations allow automatic insertion, fit standard IC sockets or printed wiring board layouts, and enable easy attachment of a heat sink for maximum power-handling capability. The heat-sink tabs are at ground potential and require no insulation.

Dual full-bridge drivers with peak current ratings of ±3 A are supplied as the UDN2998W.

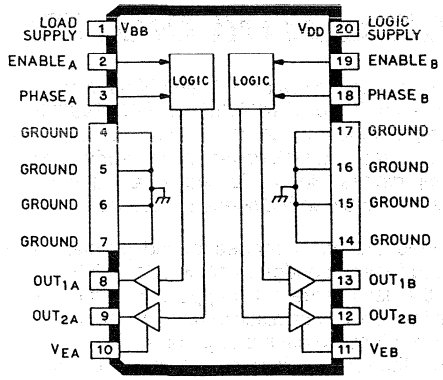
FEATURES

- ±600 mA Output Current
- Output Voltage to 40 V
- Crossover Current Protection
- TTL/NMOS/CMOS Compatible Inputs
- Low Input Current
- Internal Clamp Diodes
- DIP or SOIC Packaging

Always order by complete part number:

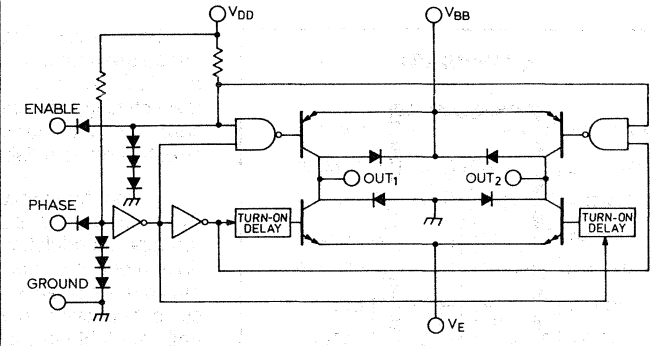
Part Number	Package
UDN2993B	16-Pin DIP
UDN2993LB	20-Lead Wide-Body SOIC

UDN2993LB



Dwg. No. A-14,340

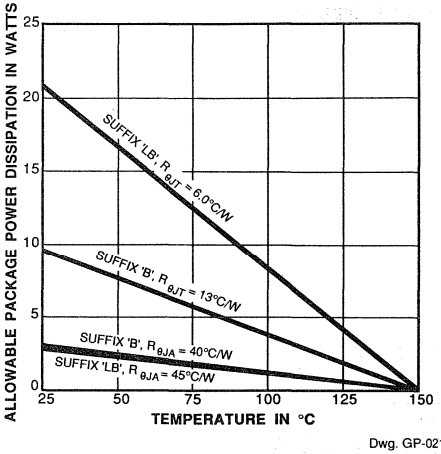
FUNCTIONAL BLOCK DIAGRAM
(One of Two Drivers)



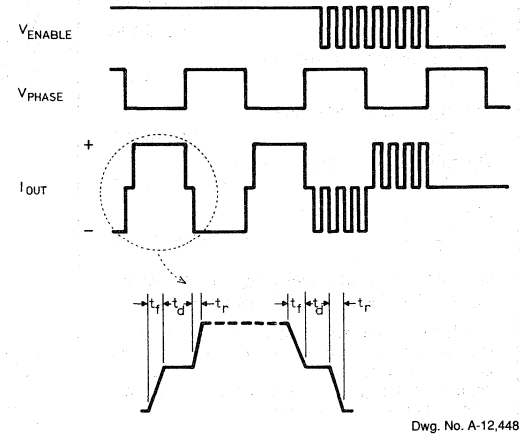
Dwg. No. A-12,447

TRUTH TABLE

Enable Input	Phase Input	Output 1	Output 2
High	High	Low	High
High	Low	High	Low
Low	High	Low	Open
Low	Low	Open	Low



Dwg. GP-021



Dwg. No. A-12,448

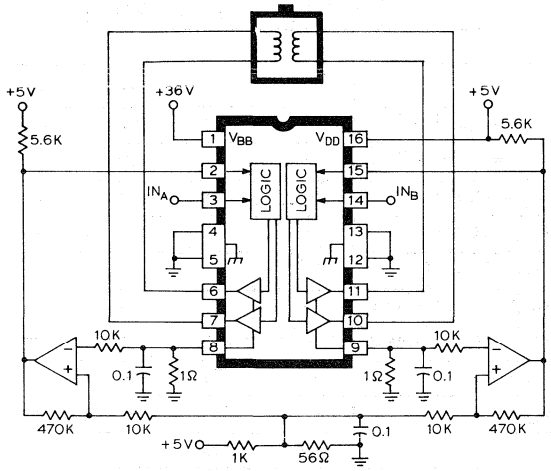
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 40 V, V_{DD} = 5 V, V_E = 0 V, $T_J \leq$ +150°C Figure 1 (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Operating Voltage Range	V_{BB}		10	—	40	V
Output Leakage Current	I_{CEX}	V_{ENABLE} = 0.8 V, V_{OUT} = V_{BB}, Note 2	—	< 1.0	10	µA
		V_{ENABLE} = 0.8 V, V_{OUT} = 0 V, Note 2	—	< -1.0	-10	µA
Output Saturation Voltage	$V_{CE(SAT)}$	V_{ENABLE} = 2.4 V, I_{OUT} = 500 mA	—	1.6	1.8	V
		V_{ENABLE} = 2.4 V, I_{OUT} = -500 mA	—	1.6	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±500 mA, Figure 2, Note 2	40	50	—	V
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 2.4 V, Outputs Open, Note 2	—	1.0	3.0	mA
	$I_{BB(OFF)}$	V_{ENABLE} = 0.8 V, Outputs Open, Note 2	—	250	300	µA
Source Driver Rise Time	t_r	I_{OUT} = -500 mA, V_{BB} = 30 V	—	-75	—	ns
Source Driver Fall Time	t_f	I_{OUT} = -500 mA, V_{BB} = 30 V	—	280	—	ns
Clamp Diode Forward Voltage	V_F	I_F = 500 mA	—	1.6	1.8	V
Control Logic (PHASE or ENABLE)						
Logic Input Current	$I_{IN(1)}$	V_{PHASE} or V_{ENABLE} = 2.4 V	—	< 1.0	10	µA
	$I_{IN(0)}$	V_{PHASE} or V_{ENABLE} = 0.8 V	—	-200	-300	µA
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Supply Current	I_{DD}		—	14	20	mA
Turn-On Delay Time	t_{pd0}	ENABLE Input to Source Drivers	—	250	—	ns
Turn-Off Delay Time	t_{pd1}	ENABLE Input to Source Drivers	—	500	—	ns

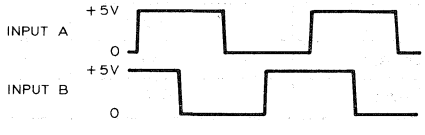
NOTES: 1. Each driver is tested separately.
2. Test is performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.4 V.
3. Negative current is defined as coming out of (sourcing) the specified device pin.

TYPICAL APPLICATION

2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)



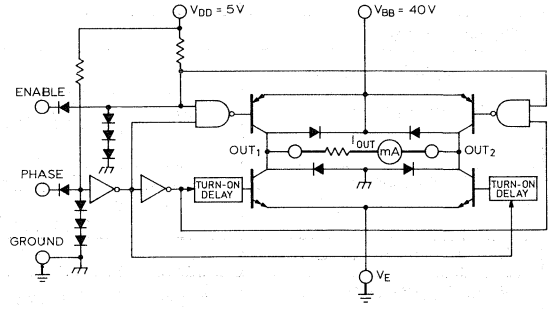
Dwg. No. A-12,453



Dwg. No. A-12,454

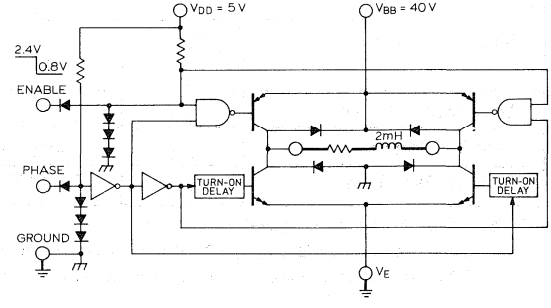
TEST FIGURES

FIGURE 1



Dwg. No. A-12,449

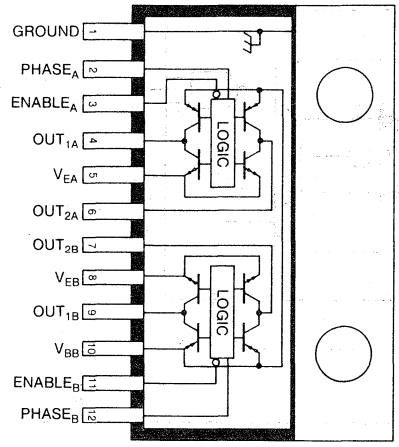
FIGURE 2



Dwg. No. A-12,450

2998

DUAL FULL-BRIDGE MOTOR DRIVER



Dwg. No. W-106

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Supply Voltage, V_{BB} . . . . . **50 V**
Output Current, I_{OUT} (DC) . . . . . **±2 A**
(Peak) . . . . . **±3 A**
Sink Driver Emitter Voltage, V_E . . . . . **1.5 V**
Logic Input Voltage Range,
V_{PHASE} or V_{ENABLE} . . . . . **-0.3 V to 15 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

NOTE: Output current rating may be limited by chopping frequency, ambient temperature, air flow, or heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of +150°C.

As an interface between low-level logic and solenoids, brushless dc motors, or stepper motors, the UDN2998W dual full-bridge driver will operate inductive loads up to 50 V with continuous output currents of up to 2 A per bridge or peak (start-up) currents to 3 A. The control inputs are compatible with TTL, DTL, and 5 V CMOS logic. Except for a common supply voltage and thermal shutdown, the two drivers in each package are completely independent.

For external PWM control, an Output Enable for each bridge circuit is provided and the sink driver emitters are pinned out for connection to external current-sensing resistors. The chopper drive mode is characterized by low power dissipation levels and maximum efficiency. A PHASE input to each bridge determines load-current direction.

Extensive circuit protection is provided on-chip. Both ground-clamp and flyback diodes for each bridge are provided. A thermal shutdown circuit disables the load drive if chip temperature rating (package power dissipation) is exceeded. Internally-generated delays provide crossover-current protection.

The UDN2998W is packaged in a 12-pin single in-line power tab package for high power capabilities. Driving either of the bridges at the full 2 A dc rating requires the use of an external heat-sink. The tab is at ground potential and needs no insulation.

A similar dual full-bridge driver for use with continuous load currents to ±500 mA is the UDN2993B.

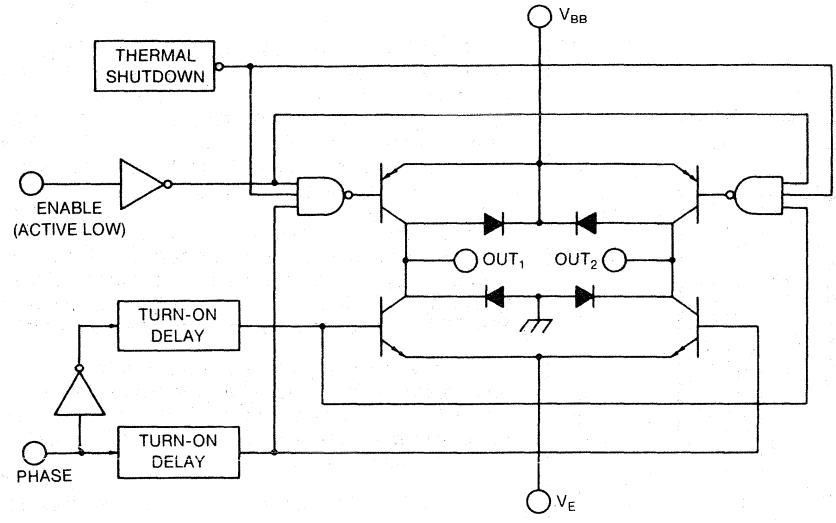
FEATURES

- ±3 A Peak Output Current
- Output Voltage to 50 V
- Integral Output Suppression Diodes
- Output Current Sensing
- TTL/CMOS Compatible Inputs
- Internal Thermal Shutdown Circuitry
- Crossover-Current Protected

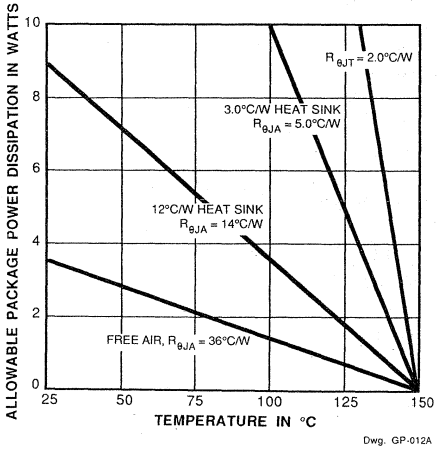
Always order by complete part number: **UDN2998W** .

2998
DUAL FULL-BRIDGE MOTOR DRIVER

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. W-107A



Dwg. GP-012A

To maintain isolation between integrated circuit components and to provide for normal transistor operation, the ground tab must be connected to the most negative point in the external circuit.

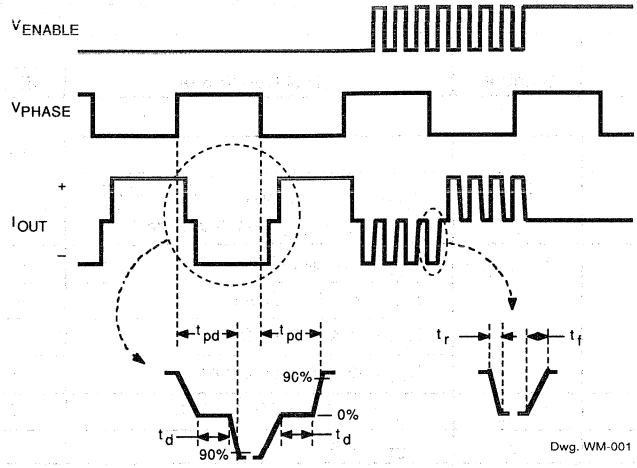
TRUTH TABLE

ENABLE INPUT	PHASE INPUT	OUTPUT 1	OUTPUT 2
Low	High	High	Low
Low	Low	Low	High
High	High	Open	Low
High	Low	Low	Open

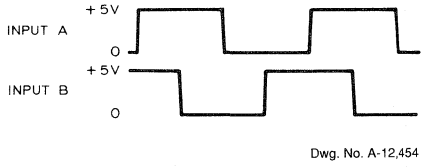
ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{BB} = 50 V

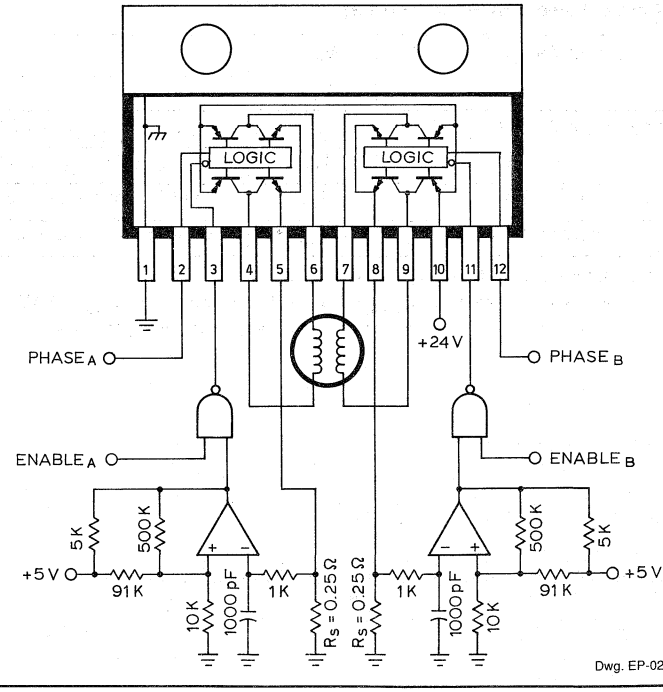
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Drivers						
Operating Voltage Range	V_{BB}		10	—	50	V
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V, V_{ENABLE} = 2.0 V, Note 2	—	<5.0	50	µA
		V_{OUT} = 0, V_{ENABLE} = 2.0 V, Note 2	—	<-5.0	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 1 A, Sink Driver	—	1.2	1.4	V
		I_{OUT} = 2 A, Sink Driver	—	1.7	1.9	V
		I_{OUT} = -1 A, Source Driver	—	1.7	1.9	V
		I_{OUT} = -2 A, Source Driver	—	2.0	2.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±2 A, L = 3.5 mH, Note 2	50	—	—	V
Source Driver Rise Time	t_r	I_{OUT} = -2 A	—	500	—	ns
Source Driver Fall Time	t_f	I_{OUT} = -2 A	—	750	—	ns
Deadtime	t_d	I_{OUT} = ±2 A	—	2.5	—	µs
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	<5.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	1.5	2.0	V
Supply Current	I_{BB}	$V_{ENABLE(1)}$ = $V_{ENABLE(2)}$ = 0.8 V	—	30	35	mA
Control Logic (PHASE or ENABLE)						
Logic Input Voltage	$V_{IN(0)}$		—	—	0.8	V
	$V_{IN(1)}$		2.0	—	—	V
Logic Input Current	$I_{IN(0)}$	V_{PHASE} or V_{ENABLE} = 0.8 V	—	-5.0	-25	µA
	$I_{IN(1)}$	V_{PHASE} or V_{ENABLE} = 2.0 V	—	<1.0	10	µA
Turn-On Delay Time	t_{pd0}	ENABLE Input to Source Drivers	—	0.4	1.0	µs
Turn-Off Delay Time	t_{pd1}	ENABLE Input to Source Drivers	—	2.0	4.0	µs

NOTES: 1. Each driver is tested separately.
2. Test is performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.0 V.
3. Negative current is defined as coming out of (sourcing) the specified device pin.



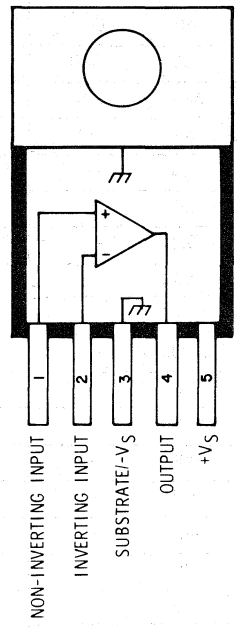
TYPICAL APPLICATION
2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)





3751

POWER OPERATIONAL AMPLIFIER



Dwg. No. PS-002

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Supply Voltage Differential
($+V_S$ to $-V_S$) . . . . . **28 V**
Peak Output Current, I_{OUT} . . . . . **±3.5 A**
Input Voltage Range,
V_{IN} . . . . . **$+V_S$ to $-V_S$ – 0.3 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **0°C to +70°C**
Storage Temperature Range,
T_S . . . . . **-40°C to +150°C**

As a combination general-purpose operational amplifier and power booster, Type ULN3751Z integrated circuit simplifies circuit design, reduces component count, and enhances system reliability.

This power op amp features high-impedance differential inputs, a unity-gain stable amplifier that needs no external compensation, and a high-current power output. Typical applications include use as voice-coil motor drivers, linear servo amplifiers, power oscillators, bipolar voltage regulators, and audio power drivers.

The ULN3751Z is for applications demanding up to ±3.5 A of output current. It is furnished in a modified 5-lead JEDEC-style TO-220 plastic package. Lead forming for vertical or horizontal mounting is available (ULN3751ZV or ULN3751ZH). The heat sink tab is at substrate potential and must be insulated from ground when the device is used with a split supply.

This power op amp operates over a recommended supply voltage range of ±3 V to ±13 V. Dual power op amps are available as the ULN3755B (16-pin DIP) and the high-power ULN3755W (12-pin SIP). Both of those devices include output current sensing and a voltage boost connection to maximum output voltage swing to ±20 V supplies at up to ±3.5 A peak output current.

FEATURES

- ±3 V to ±13 V Operation
- High Output Swing
- Peak Output Current to ±3.5 A
- Low Input Offset
- 90 dB Typical Open-Loop Gain
- Internal Thermal Shutdown
- High Common-Mode Input Range
- Unity Gain Stable
- Pin Compatible with L165, L465, SG1173

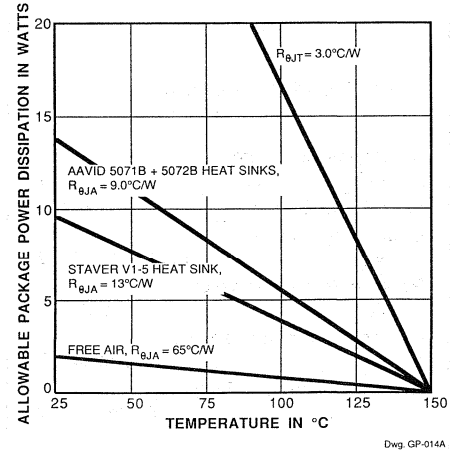
Always order by complete part number: **ULN3751Z** .

3751
POWER OPERATIONAL AMPLIFIER

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $T_j \leq$ +150°C, V_S = ±6.0 V (unless otherwise noted).

Characteristic	Test Conditions	Limits			Units
		Min.	Typ.	Max.	
Functional Supply Voltage Range	$+V_S$ to $-V_S$	6.0	—	26	V
Quiescent Supply Current		—	40	60	mA
Input Bias Current	V_{IN} = 0, I_{OUT} = 0	—	-60	-1000	nA
Input Offset Voltage	V_{IN} = 0, I_{OUT} = 0	—	±2.0	±10	mV
Input Offset Current	V_{IN} = 0, I_{OUT} = 0	—	10	100	nA
Input Noise Voltage†	BW = 40 Hz to 15 kHz	—	4.0	—	µV
Input Noise Current†	BW = 40 Hz to 15 kHz	—	60	—	pA
Crossover Distortion†	P_{OUT} = 50 mW, R_L = 4Ω	—	<0.05	—	%
Common Mode Rejection	Δ V_{CM} = 2 V	60	85	—	dB
Input Common Mode Range†	Positive	—	$+V_S$ – 2 V	—	V
	Negative	—	$-V_S$ – 0.3 V	—	V
Open-Loop Voltage Gain	f = 0	80	90	—	dB
Slew Rate	V_{IN} = V_{OUT} = 6 Vpp, R_L = ∞	1.0	2.3	—	V/µs
Gain-Bandwidth Product†	A_V = 40 dB	—	900	—	kHz
Output Voltage Swing	I_{OUT} = 1.0 A	4.5	4.7	—	V
	I_{OUT} = -1.0 A	-4.5	-4.7	—	V
Supply Voltage Rejection	$+V_S$, Δ V = 1 V	60	85	—	dB
	$-V_S$, Δ V = 1 V	60	80	—	dB
Thermal Shutdown Temp.†		—	160	—	°C

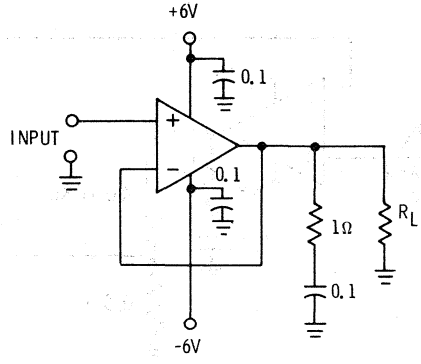
† Typical values given for circuit design information only.



Dwg. GP-014A

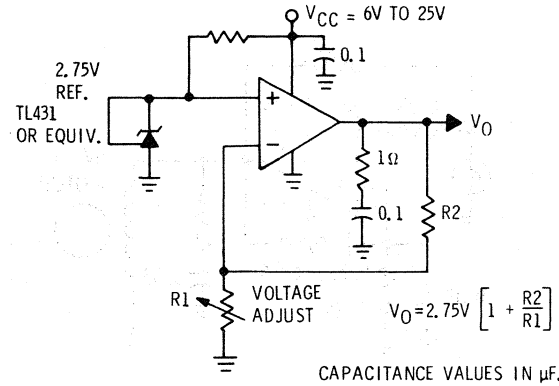
TYPICAL APPLICATIONS

UNITY GAIN VOLTAGE FOLLOWER



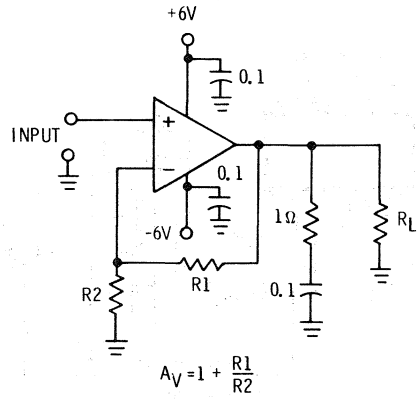
Dwg. No. A-12,551

LINEAR VOLTAGE REGULATOR



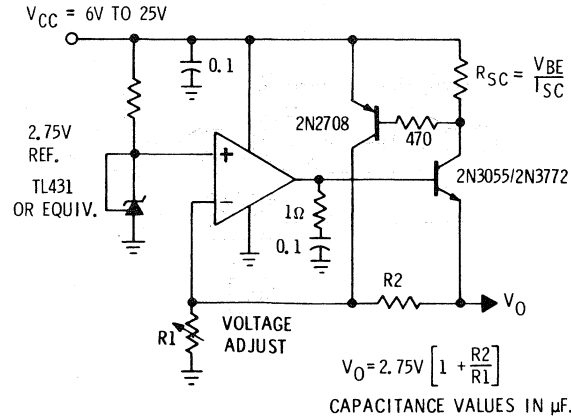
Dwg. No. A-12,553A

NON-INVERTING POWER AMPLIFIER



Dwg. No. A-12,552

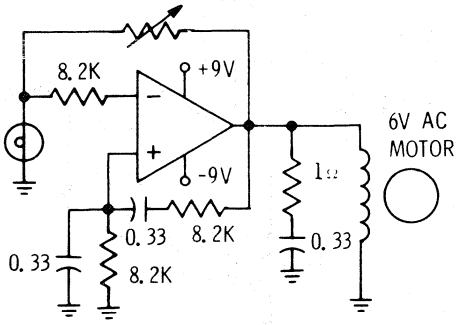
HIGH-POWER LINEAR REGULATOR
(Short-Circuit Protected)



Dwg. No. A-12,554B

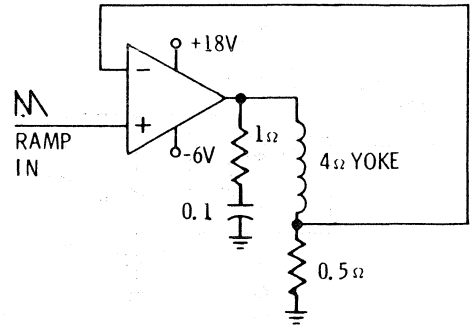
TYPICAL APPLICATIONS

WIEN BRIDGE OSCILLATOR/MOTOR DRIVER



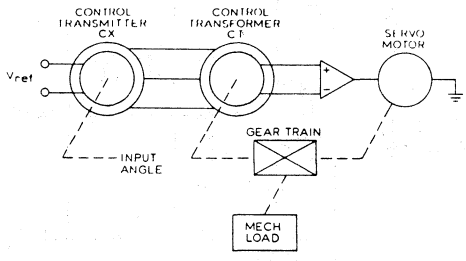
Dwg. No. A-12,376B

VIDEO MONITOR VERTICAL DEFLECTION AMP.



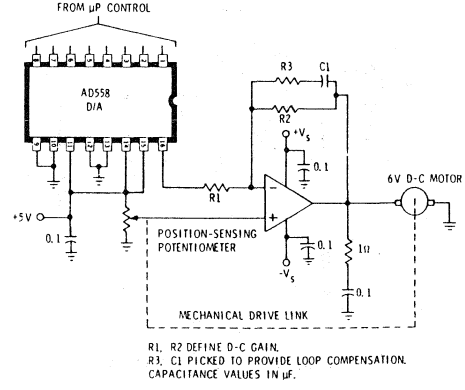
Dwg. No. A-12,375A

SIMPLIFIED SERVO APPLICATION WITH CONTROL TRANSFORMERS



Dwg. No. A-14,250

SINGLE-ENDED POSITION SERVO WITH SENSE POTENTIOMETER

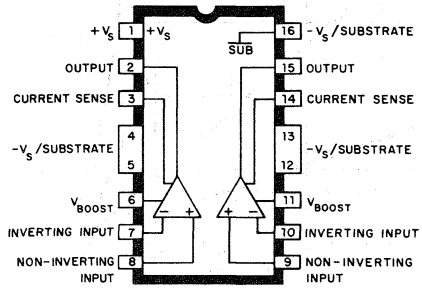


Dwg. No. A-12,556

3755

DUAL POWER OPERATIONAL AMPLIFIERS

ULN3755B



Dwg. No. A-13,063

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Differential
($+V_S$ to $-V_S$) . . . . . **40 V**
Peak Supply Voltage (50 ms) . . . . . **45 V**
Continuous Output Current, I_{OUT}
(V_S = ±15 V) . . . . . **±2.0 A**
(V_S = ±6 V) . . . . . **±2.5 A**
Peak Output Current, I_{OUT}
(50 ms) . . . . . **±3.5 A**
Package Power Dissipation,
P_D . . . . . **See Graphs**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +125°C**

Always order by complete part number:

Part Number	Package
ULN3755B	16-Pin DIP
ULN3755W	12-Pin Power-Tab SIP

Consisting of two high-power operational amplifier circuits in a single in-line power-tab package or a batwing dual in-line package, the ULN3755B and ULN3755W are specifically designed to drive high-current linear servo loads such as voice coil motors used in disc-drive applications. Their building block design concept also makes them ideal for a wide variety of other motor drive applications, for use as audio power amplifiers, power oscillators, and linear voltage regulators. Low crossover distortion eliminates servo hunting under null conditions and is required for most audio applications.

The inputs are designed to allow a wide common mode range from the negative supply (or ground in single supply applications) to within approximately two volts of the positive supply. Common-mode and power supply rejection are in excess of 60 dB. The amplifiers' wide output swing is complemented by current sensing, which is referenced to the negative supply and allows for feedback as required to produce a transconductance characteristic.

Separate supply pins are provided for the low-level input and high-level output circuits to allow voltage boost or bootstrapping to maximize output swing.

The ULN3755B is furnished in a 16-pin dual in-line package with copper heat-sink contact tabs. It can typically dissipate 6 W at a tab temperature of +70°C. The lead configuration enables easy attachment of a heat sink while fitting a standard socket or printed wiring board layout. For higher power requirements, the ULN3755W is supplied in a 12-pin single in-line power-tab package. It can safely dissipate significantly higher power levels with appropriate heat sinking. With either package configuration, the heat sink is at the negative supply, or ground in a single-ended application.

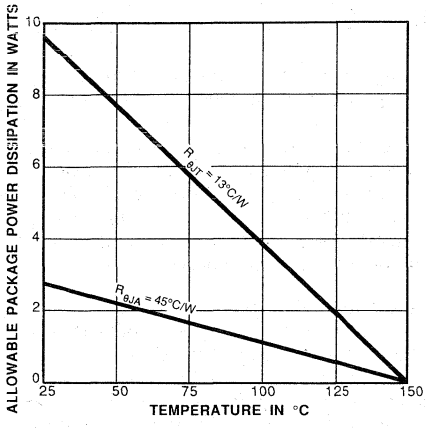
FEATURES

- Operating Supply Range ±3 to ±20 Volts
- Output Current to ±3.5 A Peak
- Output Current Limiting
- Output Current Sensing
- High Output-Voltage Swing
- Low Crossover Distortion
- Low Input Offset Voltage
- Unity-Gain Stable
- High Open-Loop Gain
- Output Protection Diodes
- Thermal Shutdown Protection
- Excellent Supply and Common-Mode Rejection
- Single or Dual In-Line Power Packages

APPLICATIONS

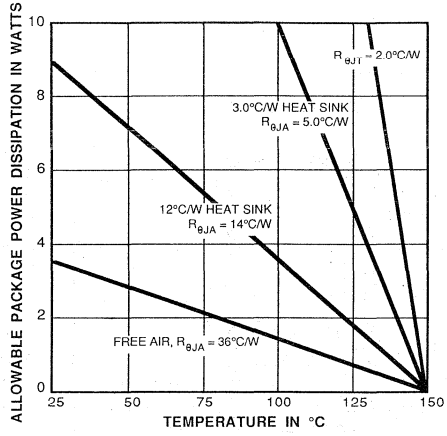
- Dual Half-Bridge and Full-Bridge Motor Drivers
  - Linear Servo Motors
  - Voice Coil Motors
  - AC and DC Motors
  - Microstepping Applications
- Power Transconductance Amplifier
- Audio Power Amplifier Stereo or BTL
- Power Oscillator/Amplifier
- Dual Bipolar Voltage Regulator

ULN3755B



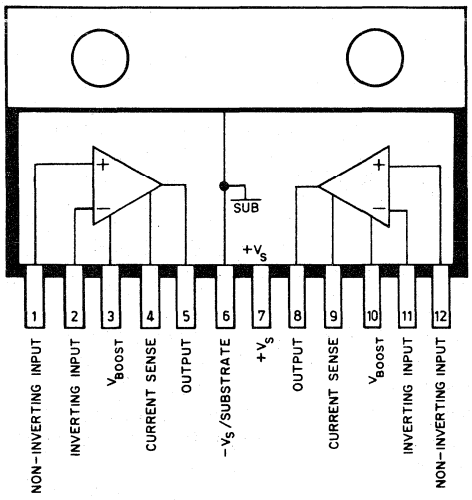
Dwg. GP-004

ULN3755W



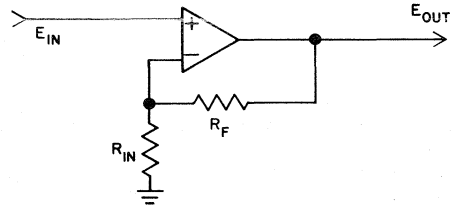
Dwg. GP-012A

ULN3755W



Dwg. No. A-13,064

NON-INVERTING AMPLIFIER

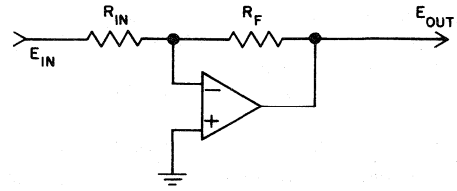


$$\frac{E_{OUT}}{E_{IN}} = 1 + \frac{R_F}{R_{IN}}$$

IF $R_F = 0$ or $R_{IN} = \infty$ THEN $E_{OUT} = E_{IN}$

Dwg. No. A-13,061

INVERTING AMPLIFIER



$$\frac{E_{OUT}}{E_{IN}} = -\frac{R_F}{R_{IN}}$$

Dwg. No. A-13,062

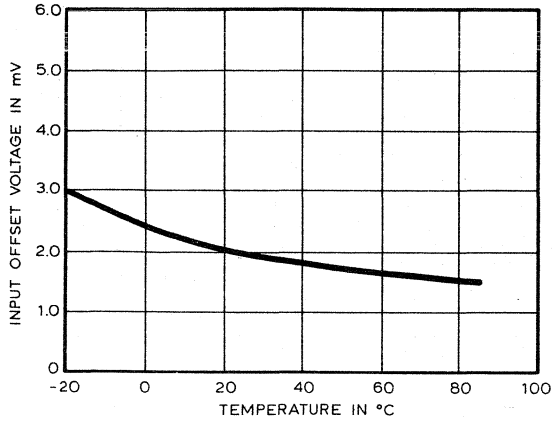
ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_S = ±6.0 V, V_{BOOST} = +9.0 V, each amplifier tested separately (unless otherwise specified).

Characteristic	Test Conditions	Limits			
		Min.	Typ.	Max.	Units
Functional Supply Voltage Range	ULN3755B, $+V_S$ to $-V_S$	6.0	—	30	V
	ULN3755W, $+V_S$ to $-V_S$	6.0	—	40	V
Quiescent Supply Current	I_{BOOST} (Each Amp.)	—	7.0	10	mA
	$+I_S$ (Total)	—	75	130	mA
Input Bias Current	V_{OUT} = 0	—	-80	-1000	nA
Input Offset Voltage	V_{OUT} = 0, I_{OUT} = 0	—	±1.0	±10	mV
Input Offset Voltage TC†	Over Operating Temperature Range	—	-15	—	µV/°C
Input Offset Current	V_{OUT} = 0, I_{OUT} = 0	—	10	100	nA
Input Noise Voltage†	BW = 40 Hz to 15 kHz	—	4.0	—	µV
Input Noise Current†	BW = 40 Hz to 15 kHz	—	60	—	pA
Crossover Distortion†	P_{OUT} = 50 mW, R_L = 4Ω	—	0.2	—	%
Common Mode Rejection	Δ V_{CM} = 3 V	60	85	—	dB
Input Common Mode Range*	V_S = ±6 V	-6.3	—	+4.0	V
	V_S = ±15 V	-15.3	—	+13	V
Open-Loop Voltage Gain	f = 0	80	100	—	dB
Slew Rate	V_{IN} = V_{OUT} = 6 Vpp	0.5	1.0	—	V/µs
Gain-Bandwidth Product†	A_V = 40 dB	—	800	—	kHz
Channel Separation†	I_{out} = 100 mA, f = 1 kHz	—	60	—	dB
Output Voltage Swing	I_{OUT} = 1 A, V_{BOOST} = +6 V	9.0	9.5	—	Vpp
	I_{OUT} = 1 A, V_{BOOST} = +9 V	9.5	10.1	—	Vpp
Supply Voltage Rejection	$+V_S$, Δ V = 1 V	60	85	—	dB
	$-V_S$, Δ V = 1 V	60	80	—	dB
Thermal Resistance, $R_{\theta JT}$*	ULN3755B	—	—	15	°C/W
	ULN3755W	—	—	3.0	°C/W
Thermal Shutdown Temp.†		—	165	—	°C

* This parameter is tested to a lot sample plan only.
† Typical values given for circuit design information only.

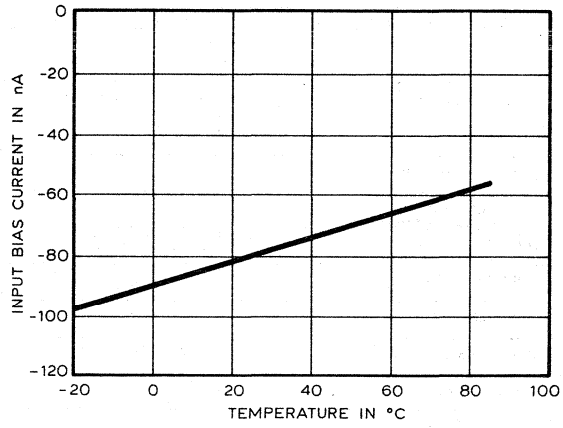
TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



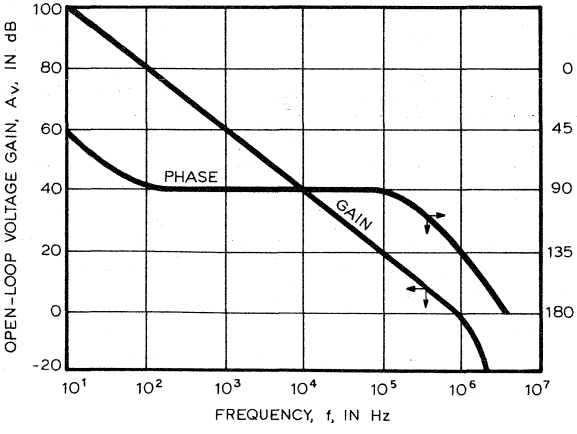
Dwg. No. A-13,294

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



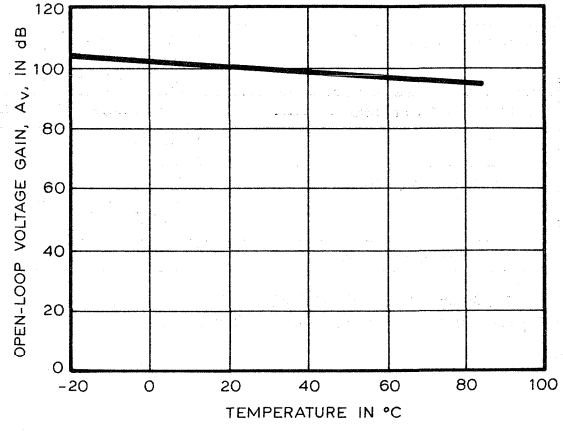
Dwg. No. A-13,295

OPEN-LOOP VOLTAGE GAIN AND PHASE AS A FUNCTION OF FREQUENCY



Dwg. No. A-13,296

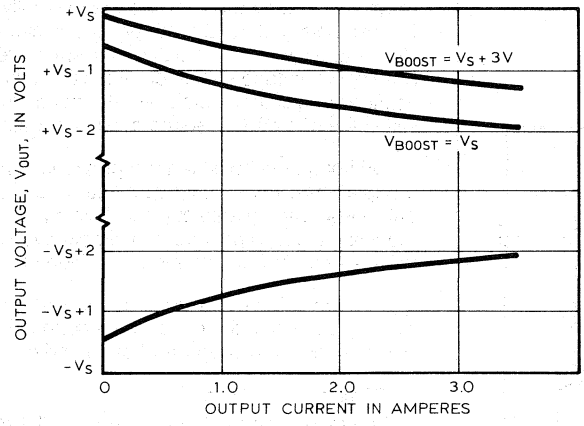
OPEN-LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



Dwg. No. A-13,297

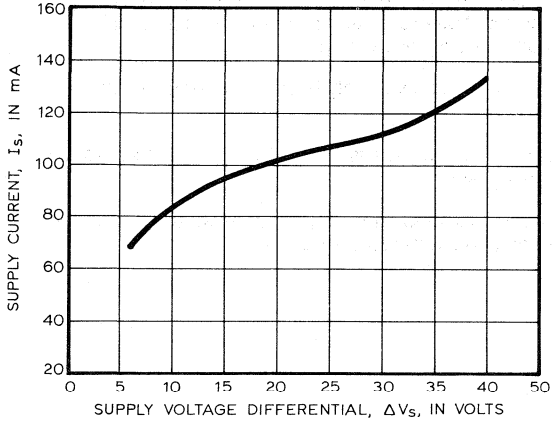
TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE SWING AS A FUNCTION OF OUTPUT CURRENT



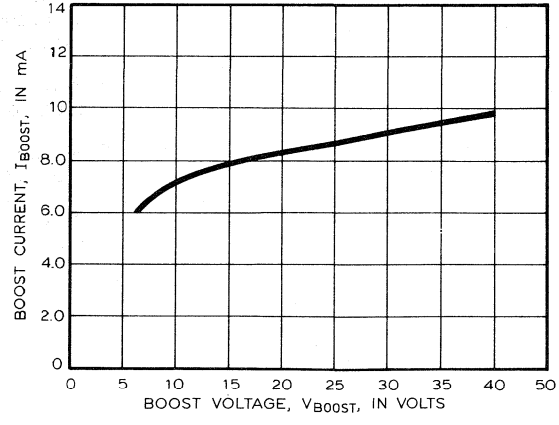
Dwg. No. A-13,298

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



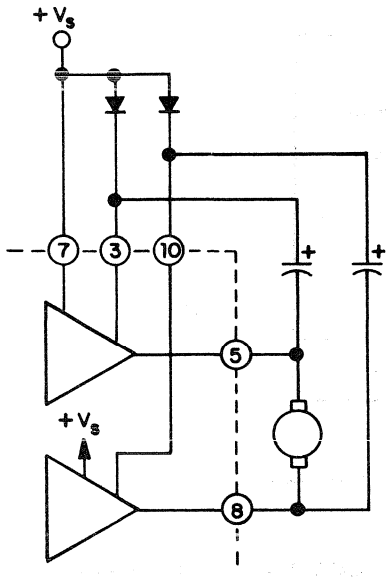
Dwg. No. A-13,299

BOOST CURRENT AS A FUNCTION OF BOOST VOLTAGE



Dwg. No. A-13,300

VOLTAGE DOUBLER BOOST SUPPLY
(ULN3755W pin numbers shown)



Dwg. No. 13,088

APPLICATIONS

INCREASED OUTPUT-VOLTAGE SWING

If a voltage higher than the supply is applied to the ULN3755B/W's boost pins, the positive output swing is limited only by the saturation resistance of the output transistors (typically less than 0.5 ohms). For example, with a 12 V supply, the circuit typically supplies a 10.5 Vpp output swing at 1 A output current. Note that the externally-supplied boost voltage should be at least 3 V higher than the load supply voltage. This criterion satisfied, the boost voltage can be any value within the IC's 40 V absolute maximum rating.

Although the boost feature provides important additional output swing at the amplifier's full rated current, the IC's boost input requires only a low, unregulated current. This can be obtained from inexpensive, modular dc to dc converters, a simple overwinding in the motor, or a voltage doubler from the motor's driven phases.

An example of a simple voltage doubler boost supply is shown. This circuit affects the doubling by connecting a series diode-capacitor between the main supply and each end of the load.

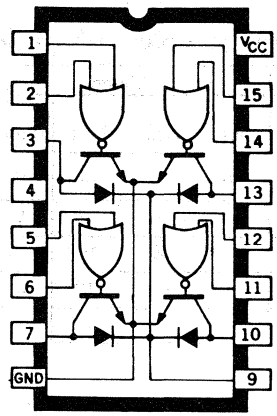
APPLICATION TIPS

1. Due to the nature of the composite PNP/NPN output structure, all applications of these devices require use of an output R-C compensation network, as shown in Figures 2, 4, and 5. Values shown are typical and will vary somewhat depending on load impedance.
2. As is the usual practice in high-gain power circuits, input and output grounds should be kept separate.
3. The current sense pins are the emitters of the power driver output totem poles and must be grounded or returned to the negative supply if not used for current sensing.
4. Provide good high-frequency supply bypass (ceramic or film capacitor).
5. All input, output, and supply leads should be properly dressed and kept as short as possible.
6. If the boost or bootstrapping capability is not used, the boost pins must be connected to the positive supply.

5703 AND 5706

QUAD 2-INPUT PERIPHERAL/POWER DRIVERS —TRANSIENT-PROTECTED OUTPUTS

UDN5703A



Dwg. No. A-9869

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} . . . . . **30 V**
Output Off-State Voltage,
V_{OFF} . . . . . **80 V**
Output On-State Sink Current,
I_{ON} . . . . . **600 mA**
Suppression Diode Off-StateVoltage,
V_{OFF} . . . . . **80 V**
Suppression Diode On-State Current,
I_{ON} . . . . . **600 mA**
Power Dissipation, P_D . . . . . **2.0 W***
Each Driver . . . . . **0.8 W**
Operating Free-Air Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*Derate at the rate of 16.7 mW/°C above T_A = +25°C

These 16-lead quad 2-input peripheral and power drivers are bipolar monolithic integrated circuits containing AND or OR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Series UDN5700A quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient-suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need of discrete diodes.

FEATURES

- Two Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V

Always order by complete part number:

Part Number	Description
UDN5703A	Quad OR Driver
UDN5706A	Quad AND Driver

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4. 75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{IN(1)}$	—	MIN	—	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	—	MIN	—	—	—	—	—	0.8	V	—
"0" Input Current	$I_{IN(0)}$	—	MAX	0.4 V	30 V	—	—	-50	-100	µA	2
"1" Input Current	$I_{IN(1)}$	—	MAX	30 V	0 V	—	—	—	10	µA	2
Input Clamp Voltage	V_{LK}	—	MIN	-12 mA	—	—	—	—	-1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts), C_L = 15 pF	—	200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts), C_L = 15 pF	—	300	750	ns	3

NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

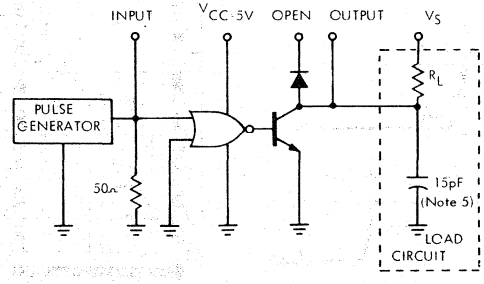
INPUT PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	t_f = 7 ns	t_p = 1µs
$V_{IN(1)}$ = 3.5 V	t_r = 14 ns	PRR = 500 kHz

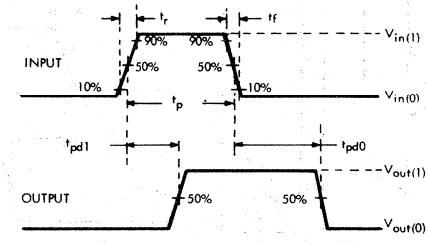
UDN5703A QUAD OR DRIVER
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	MIN	2.0 V	0 V	80 V	—	—	100	µA	—
		—	OPEN	2.0 V	0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	0.8 V	0.8V	150 mA	—	0.35	0.5	V	—
		—	MIN	0.8 V	0.8V	300 mA	—	0.5	0.7	V	—
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V	—	—	16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V	—	—	72	100	mA	1, 2

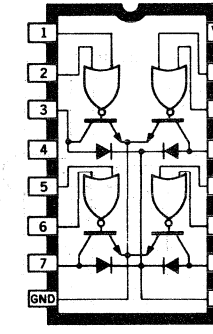
NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package
3. Diode leakage current measured at $V_R = V_{off\ (min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.



Dwg. No. A-9123A



Dwg. No. A-7628C

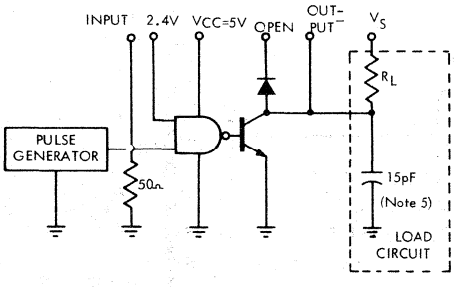


Dwg. No. A-9869

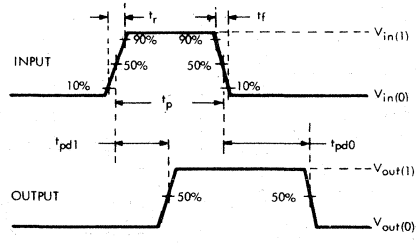
UDN5706A QUAD AND DRIVER
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	MIN	2.0 V	2.0 V	80 V	—	—	100	µA	—
		—	OPEN	2.0 V	2.0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	0.8 V	V_{CC}	150 mA	—	0.35	0.5	V	—
		—	MIN	0.8 V	V_{CC}	300 mA	—	0.5	0.7	V	—
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V	—	—	16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V	—	—	70	98	mA	1, 2

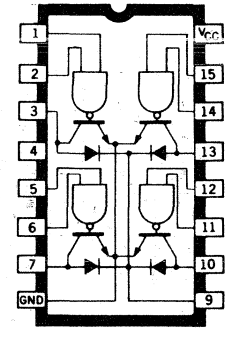
NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.



Dwg. No. A-7878A



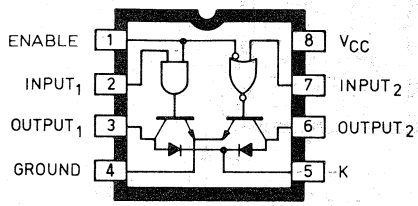
Dwg. No. A-7628C



Dwg. No. A-9866

5725

DUAL PERIPHERAL/POWER DRIVER —ENHANCED OUTPUT CAPABILITY



Dwg. No. 13,242

The UDN5725M power driver combines NAND and NOR logic gates in a configuration particularly useful with small brushless dc motor drivers. The integrated circuit includes high-current saturated output transistors and transient-suppression diodes. It can be used in many applications beyond the capabilities of standard logic buffers: With inputs tied together, one of two loads is energized by a single input signal.

Additional applications include driving peripheral loads such as solenoids, light-emitting diodes, memories, heaters, and incandescent lamps with peak load currents of up to 1.2 A.

Each of the output transistors is capable of sinking 800 mA continuously at 55°C, or 650 mA at 85°C. In the OFF state, the drivers will withstand at least 70 V.

The UDN5725M is supplied in a miniature 8-pin dual-in-line plastic package with a copper lead frame for superior package power dissipation ratings.

For applications requiring output currents of up to 700 mA, Series UDN5740M is recommended.

FEATURES

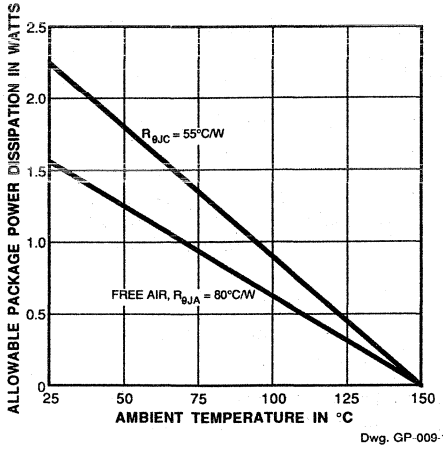
- DTL/TTL/PMOS/CMOS Compatible
- Low Input Current
- Continuous Output Current to 1 A
- 70 V Output Standoff Voltage

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Off-State Voltage, V_{OFF} . . . . . **70 V**
Output On-State Sink Current, I_{ON}
(continuous) . . . . . **1.0 A†**
(peak) . . . . . **1.2 A**
Logic Supply Voltage, V_{CC} . . . . . **16 V**
Input Voltage, V_{IN} . . . . . **30 V**
Suppression Diode Off-State Voltage, V_{OFF} . . . . . **70 V**
Suppression Diode On-State Current, I_{ON} . . . . . **1.0 A**
Allowable Package Power Dissipation, P_D . . . . . **See Graph**
Operating Free-Air Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

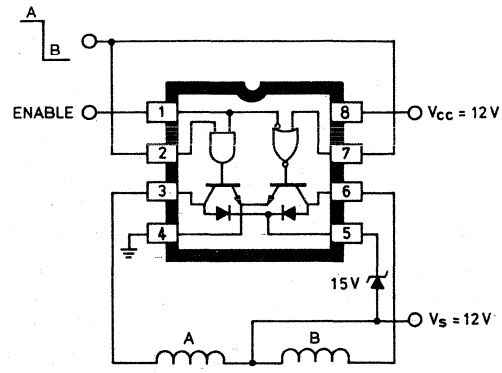
† Limited by P_D.

Always order by complete part number: **UDN5725M** .



Dwg. GP-009-1

TYPICAL APPLICATION



Dwg. No. 13,244

RECOMMENDED OPERATING CONDITIONS

Operating Conditions	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.75	12	14	V
Output Current, I_{ON}	—	—	650	mA
Operating Temperature Range	0	+25	+85	°C

SWITCHING CHARACTERISTICS at T_A = +25°C , V_{CC} = 5.0 V

Characteristic	Symbol	Test Conditions	Limits			Notes
			Min.	Max.	Units	
Turn-On Delay Time	t_{pd0}	V_S = 30 V, R_L = 100 Ω (10 W), C_L = 15 pF	—	750	ns	1, 2
Turn-Off Delay Time	t_{pd1}	V_S = 30 V, R_L = 100 Ω (10 W), C_L = 15 pF	—	1000	ns	1, 2

NOTES: 1. Capacitance value specified includes probe and test fixture capacitance.
2. Voltage values shown in test circuit waveforms are with respect to network ground.

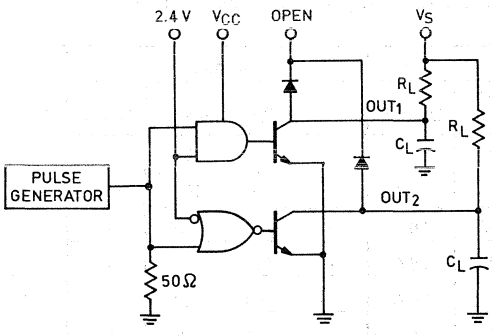
TRUTH TABLE

Strobe Input	Phase Inputs		Outputs	
	1	2	1	2
H	H	H	L	H
H	H	L	L	L
H	L	L	H	L
H	L	H	H	H
L	X	X	H	H

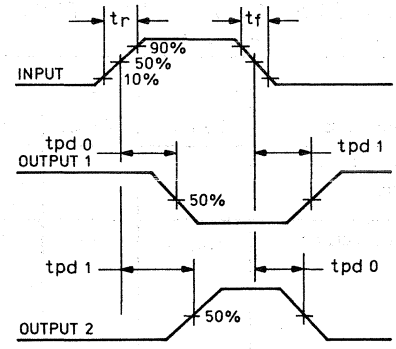
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Enable Input	Other Inputs	Output	Min.	Typ.	Max.	Units	
Output Reverse Current	I_{CEX}	—	4.75	0.8 V	2.0 V	70 V	—	—	100	µA	—
			4.75	0.8 V	0.8 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(sat)}$	—	14	2.0 V	2.0 V	0.6 A	—	0.4	0.6	V	—
			14	2.0 V	2.0 V	0.8 A	—	0.7	1.0	V	—
			14	2.0 V	2.0 V	1.0 A	—	0.9	1.2	V	3
			14	2.0 V	0.8 V	0.6 A	—	0.4	0.6	V	—
			14	2.0 V	0.8 V	0.8 A	—	0.7	1.0	V	—
			14	2.0 V	0.8 V	1.0 A	—	0.9	1.2	V	3
	$V_{CE(sus)}$	+25°C	14	⊓	0 V	0.8 A	50	—	—	V	3, 4
			14	⊓	2.0 V	0.8 A	50	—	—	V	3, 4
Input Voltage	$V_{IN(1)}$	—	—	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	—	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	12.6	0.4 V	30 V	—	—	5.0	25	µA	1
	$I_{IN(1)}$	—	12.6	30 V	0 V	—	—	5.0	25	µA	1
Enable Input Current	$I_{IN(0)}$	—	12.6	0.4 V	30 V	—	—	10	50	µA	—
	$I_{IN(1)}$	—	12.6	30 V	0 V	—	—	10	50	µA	—
Input Clamp Volt.	V_{CLAMP}	—	4.75	-12 mA	—	—	—	—	-1.5	V	—
Diode Leakage	I_R	+25°C	5.0	0 V	0 V	Open	—	—	100	µA	2
Diode Forward Voltage	V_F	+25°C	5.0	0 V	0 V	0.6 A	—	1.5	2.0	V	—
			5.0	0 V	0 V	1.0 A	—	1.9	2.5	V	3
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	12.6	0 V	0 V	—	—	3.9	5.0	mA	—
			12.6	0 V	2.0 V	—	—	3.9	5.0	mA	—
	$I_{CC(0)}$	+25°C	12.6	2.0 V	0 V	—	—	22	30	mA	—
			12.6	2.0 V	2.0 V	—	—	22	30	mA	—

NOTES: 1. Except ENABLE input, each input tested separately.
2. Diode leakage current measured at V_R = 70 V.
3. Pulse Test.
4. L_L = 3 mH.



Dwg. No. 13,245



Dwg. No. 13,246

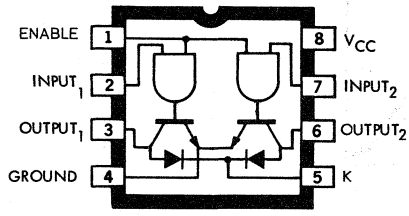
INPUT-PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	t_f = 7 ns	t_p = 1 µs
$V_{IN(1)}$ = 3.5 V	t_r = 14 ns	PRR = 500 kHz

SERIES 5740

DUAL PERIPHERAL/POWER DRIVERS —TRANSIENT-PROTECTED OUTPUTS

UDN5742M



Dwg. No. A-9790B

ABSOLUTE MAXIMUM RATINGS

Output Off-State Voltage, V_{OFF} . . . . . **70 V**
Output On-State Sink Current,
I_{ON} . . . . . **700 mA**
Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} . . . . . **30 V**
Suppression Diode Off-State Voltage,
V_{OFF} . . . . . **70 V**
Suppression Diode On-State Current,
V_{ON} . . . . . **700 mA**
Allowable Package Power Dissipation,
P_D . . . . . **1.5 W***
Operating Free-Air Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*Derate at the rate of 12.5 mW/°C above T_A = +25°C.

Peripheral and power drivers combining dual logic gates, high-current saturated output transistors, and transient-suppression diodes is the Series UDN5740M. These monolithic dual drivers surpass the interface requirements normally associated with standard logic buffers and are ideally suited for interface between low-level logic and high-current inductive loads. Internal transient-suppression diodes allow thei use with loads such as stepping motors, relays, or solenoids. Additiona (non-inductive) applications include driving peripheral loads such as light-emitting diodes, memories, heaters, and incandescent lamps with peak load currents of up to 700 mA.

The Series UDN5740M is capable of sinking 600 mA continuously for a single output (57% duty cycle for both outputs). The outputs may be paralleled for higher load-current capability. In the OFF state, the drivers will withstand at least 70 V.

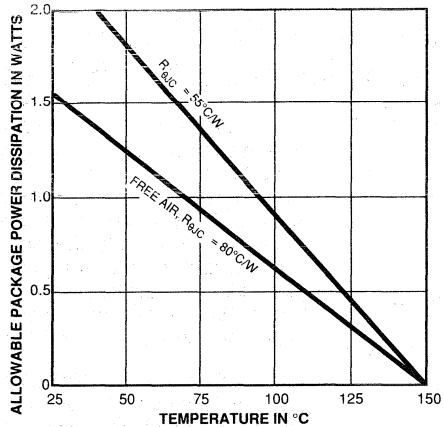
All devices in this series are supplied in a miniature 8-pin dual-in-line plastic package with a copper lead frame for superior package power dissipation ratings.

FEATURES

- DTL/TTL/PMOS/CMOS Compatible
- Low Input Current
- Output Current to 700 mA
- 70 V Output Standoff Voltage

Always order by complete part number:

Part Number	Description
UDN5741M	Dual AND Driver
UDN5742M	Dual NAND Driver
UDN5743M	Dual OR Driver
UDN5744M	Dual NOR Driver



Dwg. GP-009-1

RECOMMENDED OPERATING CONDITIONS

Operating Condition	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.75	5.00	5.25	V
Output Current, I_{ON}	—	—	600	mA
Operating Temperature Range	0	+25	+85	°C

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

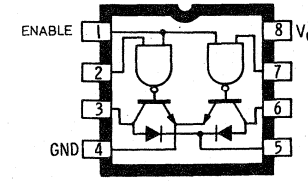
Characteristic	Symbol	Test Conditions	Limits			Notes
			Min.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 30 V, R_L = 100 Ω (10 W), C_L = 15 pF	—	750	ns	1,2
Turn-off Delay Time	t_{pd1}	V_S = 30 V, R_L = 100 Ω (10 W), C_L = 15 pF	—	1000	ns	1,2

NOTES: 1. Capacitance value specified includes probe and test fixture capacitance.
2. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.

INPUT-PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	$t_f \leq 7$ ns	t_p = 1 µs
$V_{IN(1)}$ = 3.5 V	$t_r \leq 14$ ns	PRR = 500 kHz

SERIES 5740
DUAL PERIPHERAL/POWER DRIVERS



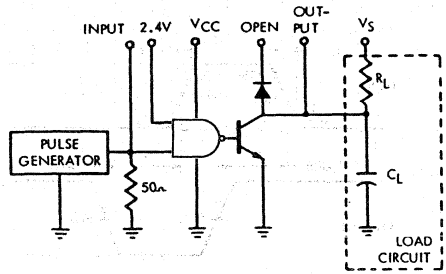
Dwg. No. A-9791A

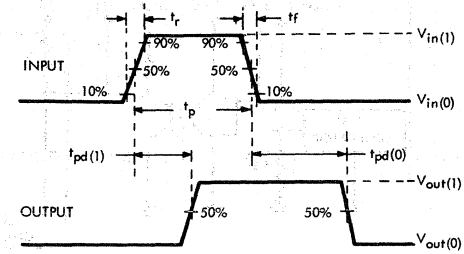
UDN5741M

ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
Output Reverse Current	I_{CEX}	—	4.75	2.0 V	2.0 V	70 V	—	—	100	µA	—
			Open	2.0 V	2.0 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	4.75	0.8 V	4.75 V	300 mA	—	0.3	0.6	V	—
			4.75	2.0 V	4.75 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	5.25	0.4 V	30 V	—	—	-5.0	-10	µA	1
	$I_{IN(1)}$	—	5.25	30 V	0 V	—	—	5.0	10	µA	1
Enable Input Current	$I_{IN(0)}$	—	5.25	0.4 V	30 V	—	—	-10	-20	µA	—
	$I_{IN(1)}$	—	5.25	30 V	0 V	—	—	10	20	µA	—
Input Clamp Voltage	V_{CLAMP}	—	4.75	-12 mA	—	—	—	—	-1.5	V	—
Diode Leakage Current	I_R	+25°C	5.0	0 V	0 V	Open	—	—	100	µA	2
Diode Forward Voltage	V_F	+25°C	5.0	5.0 V	5.0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5.25	5.0 V	5.0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5.25	0 V	0 V	—	—	20	25	mA	—

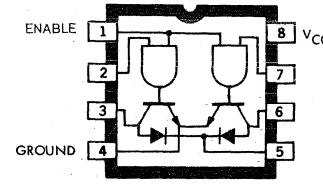
NOTES: 1. Except ENABLE input, each input tested separately.
2. Diode leakage current measured at V_R = 70 V.





Dwg. No. A-7628D

SERIES 5740
DUAL PERIPHERAL/POWER DRIVERS

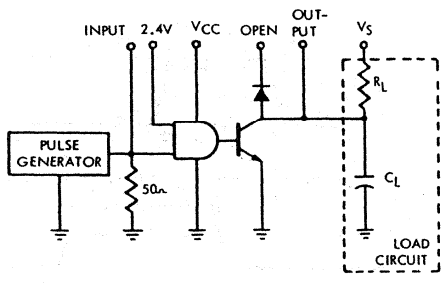


Dwg. No. A-9790B

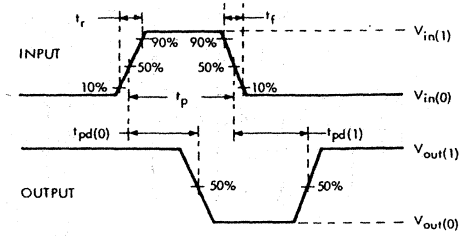
UDN5742M
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
Output Reverse Current	I_{CEX}	—	4.75	0.8 V	4.75 V	70 V	—	—	100	µA	—
			Open	0.8 V	4.75 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	4.75	2.0 V	2.0 V	300 mA	—	0.3	0.6	V	—
			4.75	2.0 V	2.0 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	5.25	0.4 V	30 V	—	—	-5.0	-10	µA	1
	$I_{IN(1)}$	—	5.25	30 V	0 V	—	—	5.0	10	µA	1
Enable Input Current	$I_{IN(0)}$	—	5.25	0.4 V	30 V	—	—	-10	-20	µA	—
	$I_{IN(1)}$	—	5.25	30 V	0 V	—	—	10	20	µA	—
Input Clamp Voltage	V_{CLAMP}	—	4.75	-12 mA	—	—	—	—	-1.5	V	—
Diode Leakage Current	I_R	+25°C	5.0	5.0 V	5.0 V	Open	—	—	100	µA	2
Diode Forward Voltage	V_F	+25°C	5.0	0 V	0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5.25	0 V	0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5.25	5.0 V	5.0 V	—	—	20	25	mA	—

NOTES: 1. Except ENABLE input, each input tested separately.
2. Diode leakage current measured at V_R = 70 V.

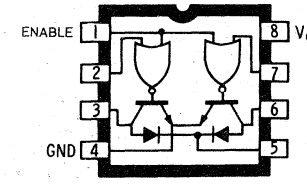


Dwg. No. A-11,746A



Dwg. No. A-7900B

SERIES 5740
DUAL PERIPHERAL/POWER DRIVERS



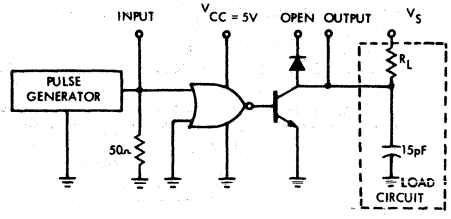
Dwg. No. A-9789A

UDN5743M

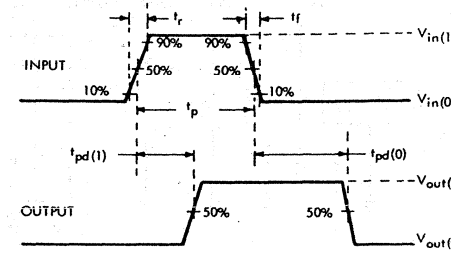
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
Output Reverse Current	I_{CEX}	—	4.75	2.0 V	0 V	70 V	—	—	100	µA	—
			Open	2.0 V	0 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	4.75	0.8 V	0.8 V	300 mA	—	0.3	0.6	V	—
			4.75	0.8 V	0.8 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	5.25	0.4 V	30 V	—	—	-5.0	-10	µA	1
	$I_{IN(1)}$	—	5.25	30 V	0 V	—	—	5.0	10	µA	1
Enable Input Current	$I_{IN(0)}$	—	5.25	0.4 V	30 V	—	—	-10	-20	µA	—
	$I_{IN(1)}$	—	5.25	30 V	0 V	—	—	10	20	µA	—
Input Clamp Voltage	V_{CLAMP}	—	4.75	-12 mA	—	—	—	—	1.5	V	—
Diode Leakage Current	I_R	+25°C	0	0 V	0 V	Open	—	—	100	µA	2
Diode Forward Voltage	V_F	+25°C	5.0	5.0 V	5.0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5.25	5.0 V	5.0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5.25	0 V	0 V	—	—	20	25	mA	—

NOTES: 1. Except ENABLE input, each input tested separately.
2. Diode leakage current measured at V_R = 70 V.

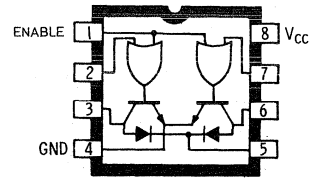


Dwg. No. A-13,219A



Dwg. No. A-7628D

SERIES 5740
DUAL PERIPHERAL/POWER DRIVERS

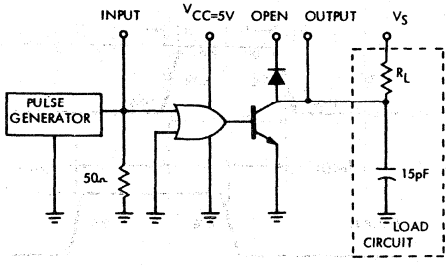


Dwg. No. A-9788A

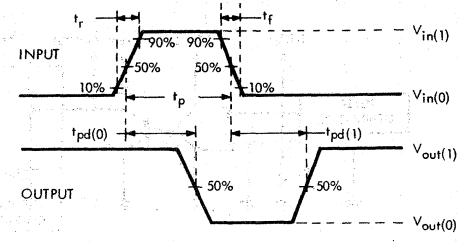
UDN5744M
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
Output Reverse Current	I_{CEX}	—	4.75	0.8 V	0.8 V	70 V	—	—	100	µA	—
			Open	0.8 V	0.8 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	4.75	2.0 V	0 V	300 mA	—	0.3	0.6	V	—
			4.75	2.0 V	0 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	5.25	0.4 V	0 V	—	—	-5.0	-10	µA	1
	$I_{IN(1)}$	—	5.25	30 V	30 V	—	—	5.0	10	µA	1
Enable Input Current	$I_{IN(0)}$	—	5.25	0.4 V	0 V	—	—	-10	-20	µA	—
	$I_{IN(1)}$	—	5.25	30 V	30 V	—	—	10	20	µA	—
Input Clamp Voltage	V_{CLAMP}	—	4.75	-12 mA	—	—	—	—	-1.5	V	—
Diode Leakage Current	I_R	+25°C	5.0	5.0 V	5.0 V	Open	—	—	100	µA	2
Diode Forward Voltage	V_F	+25°C	5.0	0 V	0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5.25	0 V	0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5.25	5.0 V	5.0 V	—	—	20	25	mA	—

NOTES: 1. Except ENABLE input, each input tested separately.
2. Diode leakage current measured at V_R = 70 V.



Dwg. No. A-13,218A

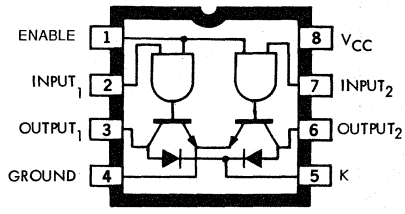


Dwg. No. A-7900B

5752

DUAL PERIPHERAL AND POWER DRIVER —TRANSIENT-PROTECTED OUTPUTS

UDN5752M



Dwg. No. A-9790B

Combining dual AND logic gates, high-current switching transistors, and transient suppression diodes in a bipolar monolithic integrated circuit, this peripheral and power driver meets interface requirements beyond the capabilities of standard logic buffers. The UDN5752M will sink 500 mA continuously for a single output (86% duty cycle for both outputs). In the OFF state, the drivers will withstand at least 70 V. In addition to driving common peripheral loads such as LEDs, heaters, or incandescent lamps with peak (in-rush) currents to 600 mA, the internal diodes allow its use directly with inductive loads such as stepping motors, relays, or solenoids. This device was previously sold as the UDN5732M.

The UDN5752M is supplied in a miniature 8-pin dual in-line plastic package with a copper lead frame for enhanced package power dissipation capabilities.

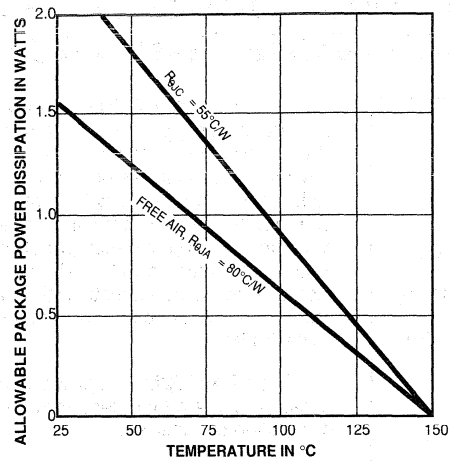
FEATURES

- DTL/TTL/PMOS/CMOS Compatible
- Low Input Current
- Output Current to 600 mA
- 70 V Output Standoff Voltage

ABSOLUTE MAXIMUM RATINGS

Output Off-State Voltage, V_{OFF} . . . . . **70 V**
Output On-State Sink Current,
I_{ON} . . . . . **600 mA**
Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} . . . . . **30 V**
Suppression Diode Off-State Voltage,
V_{OFF} . . . . . **70 V**
Suppression Diode On-State Current,
I_{ON} . . . . . **600 mA**
Allowable Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Free-Air Temperature Range,
T_A . . . . . **-20°C to + 85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Always order by complete part number: **UDN5752M**.



Dwg. GP-009-1

RECOMMENDED OPERATING CONDITIONS

Operating Condition	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.75	5.00	5.25	V
Output Current, I_{ON}	—	—	500	mA
Operating Temperature Range	0	+25	+85	°C

SWITCHING CHARACTERISTICS at T_A = +25°C , V_{CC} = 5.0 V

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Max.	Units	Notes
Turn-On Delay Time	t_{pd0}	V_S = 30 V, R_L = 100 (10 W), C_L = 15 pF	—	750	ns	1, 2
Turn-Off Delay Time	t_{pd1}	V_S = 30 V, R_L = 100 (10 W), C_L = 15 pF	—	1000	ns	1, 2

NOTES: 1. Capacitance value specified includes probe and test fixture capacitance.
2. Voltage values shown in test circuit waveforms are with respect to network ground.

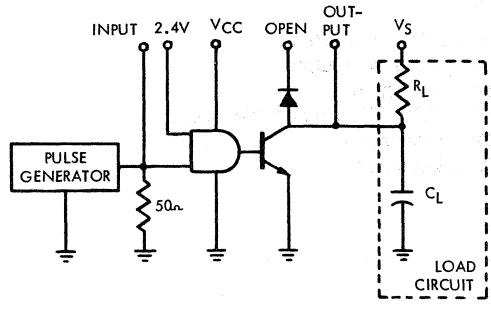
INPUT-PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	$t_f \leq 7$ ns	t_p = 1 µs
$V_{IN(1)}$ = 3.5 V	$t_r \leq 14$ ns	PRR = 500kHz

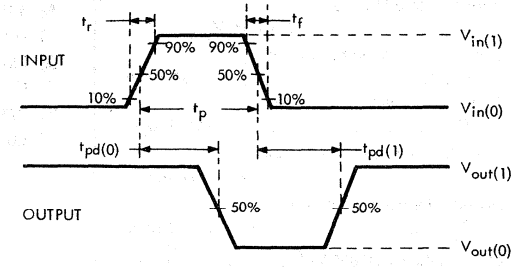
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
Output Reverse Current	I_{CEX}	—	4.75	0.8 V	4.75 V	70 V	—	—	100	µA	—
			Open	0.8 V	4.75 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	4.75	2.0 V	2.0 V	300 mA	—	0.3	0.6	V	—
			4.75	2.0 V	2.0 V	500 mA	—	0.5	0.8	V	—
Input Voltage	$V_{IN(1)}$	—	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	5.25	0.4 V	30 V	—	—	- 5.0	-10	µA	1
	$I_{IN(1)}$	—	5.25	30 V	0 V	—	—	5.0	10	µA	1
Enable Input Current	$I_{IN(0)}$	—	5.25	0.4 V	30 V	—	—	-10	- 20	µA	—
	$I_{IN(1)}$	—	5.25	30 V	0 V	—	—	10	20	µA	—
Input Clamp Voltage	V_{CLAMP}	—	4.75	-12 mA	—	—	—	—	-1.5	V	—
Diode Leakage Current	I_R	+25°C	5.0	5.0 V	5.0 V	Open	—	—	100	µA	2
Diode Forward Voltage	V_F	+25°C	5 0	0 V	0 V	500 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5.25	0 V	0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5.25	5.0 V	5.0 V	—	—	20	25	mA	—

NOTES: 1. Except ENABLE input, each input tested separately.
2. Diode leakage current measured at V_R = 70 V.



Dwg. No. A-11,746A

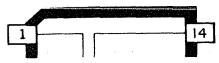


Dwg. No. A-7900B

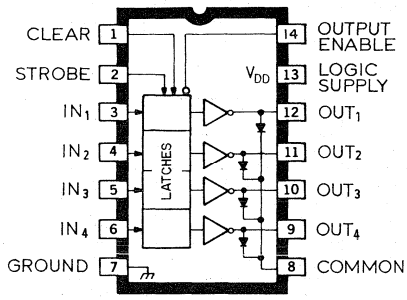
5800 AND 5801

BiMOS II LATCHED DRIVERS

UCN5800L



UCN5800A



Dwg. No. A-10,499D

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . **50 V**
Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Collector Current,
I_C . . . . . **500 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Note that the UCN5800A (dual in-line package) and UCN5800L (small-outline IC package) are electrically identical and share a common pin number assignment.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5800A/L and UCN5801A/EP latched drivers are high-voltage, high-current integrated circuits comprised of CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The UCN5800A and UCN5800L each contain four latched drivers; the UCN5801A and UCN5801EP contain eight latched drivers.

BiMOS II devices have much faster data input rates than the original BiMOS circuits (UCN4401A and UCN4801A). With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

All devices have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

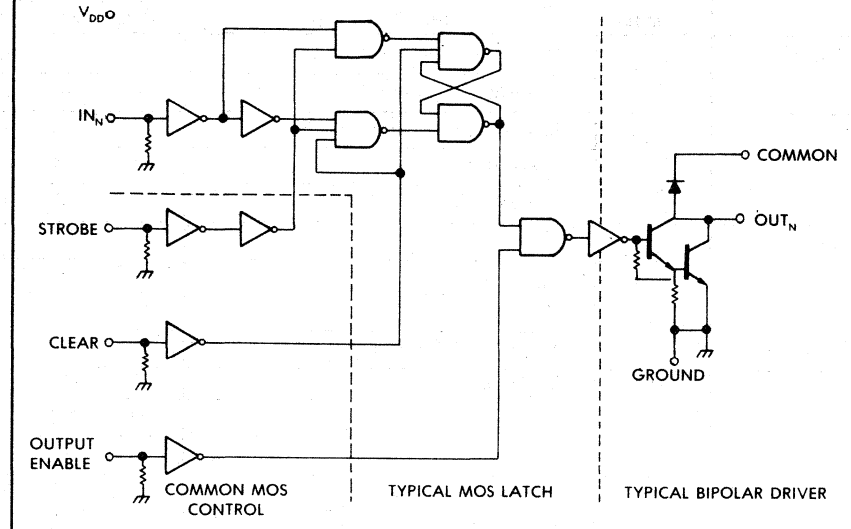
The UCN5800A is furnished in a standard 14-pin DIP; the UCN5800L in a surface-mountable SOIC; the UCN5801A in a 22-pin DIP with 0.400" (10.16 mm) row centers; the UCN5801EP in a 28-lead PLCC.

FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

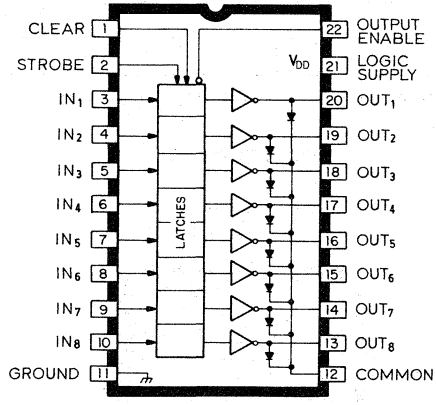
Always order by complete part number, e.g., **UCN5801EP**.

FUNCTIONAL BLOCK DIAGRAM

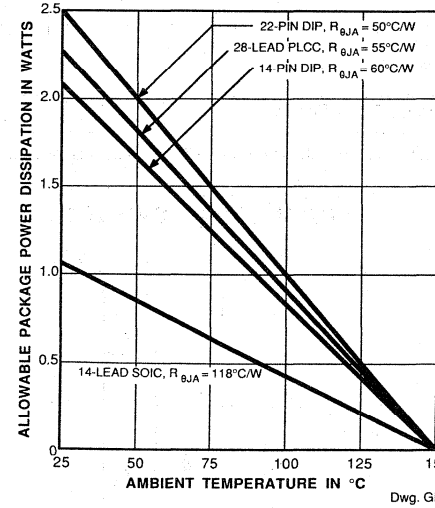


Dwg. No. A-10,495A

UCN5801A



Dwg. No. A-10,498D



Dwg. GP-023

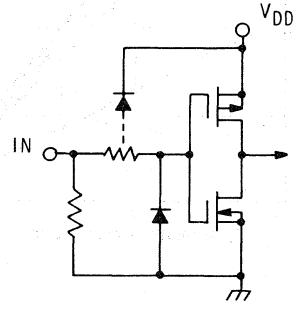
5800 AND 5801
BiMOS II LATCHED DRIVERS

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C	—	—	50	µA
		V_{CE} = 50 V, T_A = +70°C	—	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	0.9	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	50	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = +25°C	—	—	50	µA
		V_R = 50 V, T_A = +70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

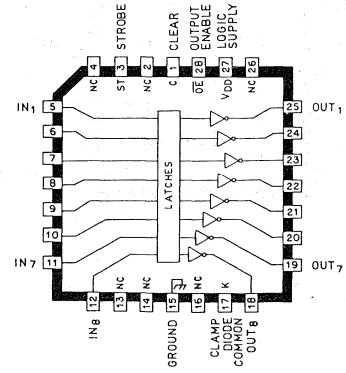
NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

TYPICAL INPUT CIRCUIT

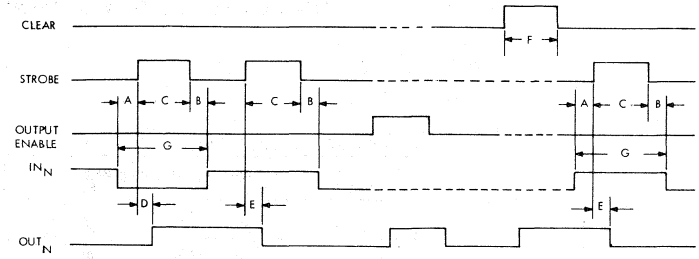


Dwg. No. A-12,520

UCN5801EP



Dwg. No. 14,353



Dwg. No. A-10,895A

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . . **50 ns**
C. Minimum Strobe Pulse Width . . . . . **125 ns**
D. Typical Time Between Strobe Activation and Output On to Off Transition . . . . . **500 ns**
E. Minimum Time Between Strobe Activation and Output Off to On Transition . . . . . **500 ns**
F. Minimum Clear Pulse Width . . . . . **300 ns**
G. Minimum Data Pulse Width. . . . . **225 ns**

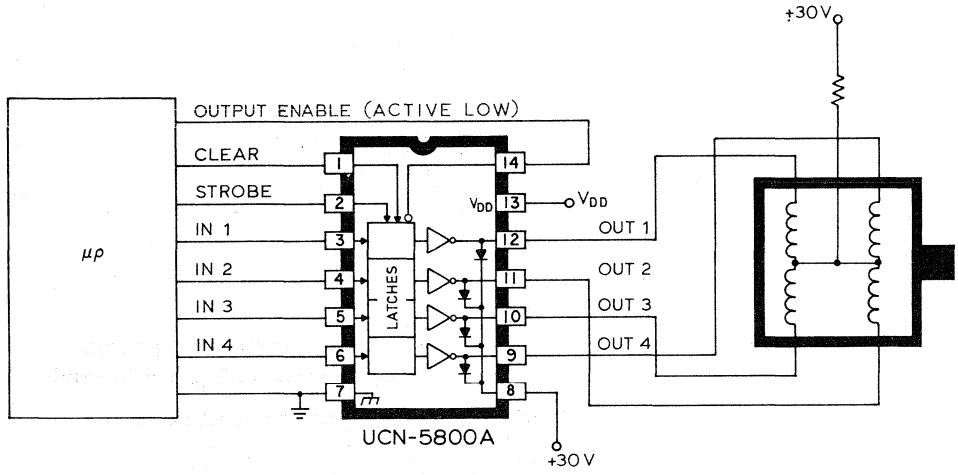
Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_{IN} t-1	OUT_{IN} t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

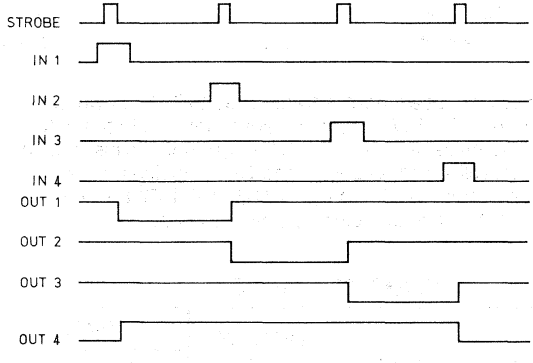
X = irrelevant
t-1 = previous output state
t = present output state

TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



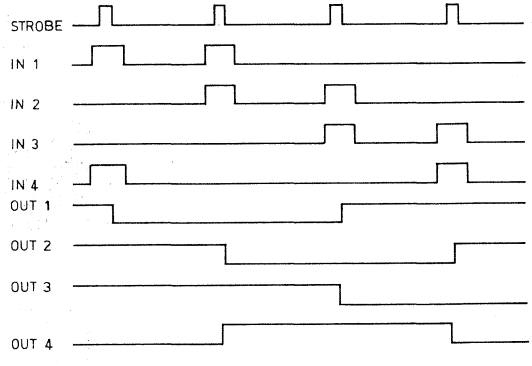
Dwg. No. B-1537

UNIPOLAR WAVE DRIVE



Dwg. No. A-11,446

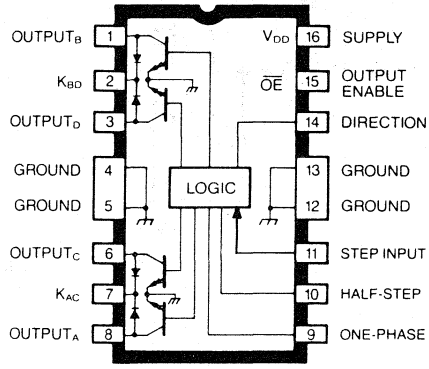
UNIPOLAR 2-PHASE DRIVE



Dwg. No. A-11,447

5804

BiMOS II UNIPOLAR STEPPER-MOTOR TRANSLATOR/DRIVER



Dwg. No. W-194

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} . . . . . **50 V**
Output Sustaining Voltage, $V_{CE\ (sus)}$ . . . . . **35 V**
Output Sink Current, I_{OUT} . . . . . **1.5 A**
Logic Supply Voltage, V_{DD} . . . . . **7.0 V**
Input Voltage, V_{IN} . . . . . **7.0 V**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

Combining low-power CMOS logic with high-current and high-voltage bipolar outputs, the UCN5804B BiMOS II translator/driver provides complete control and drive for a four-phase unipolar stepper-motor with continuous output current ratings to 1.25 A per phase (1.5 A startup) and 35 V.

The CMOS logic section provides the sequencing logic, DIRECTION and OUTPUT ENABLE control, and a power-ON reset function. Three stepper-motor drive formats, wave-drive (one-phase), two-phase, and half-step are externally selectable. The inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or LSTTL may require the use of appropriate pull-up resistors to ensure a proper input-logic high.

The wave-drive format consists of energizing one motor phase at a time in an A-B-C-D (or D-C-B-A) sequence. This excitation mode consumes the least power and assures positional accuracy regardless of any winding inbalance in the motor. Two-phase drive energizes two adjacent phases in each detent position (AB-BC-CD-DA). This sequence mode offers an improved torque-speed product, greater detent torque, and is less susceptible to motor resonance. Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-BC-C-CD-D-DA), providing an eight-step sequence.

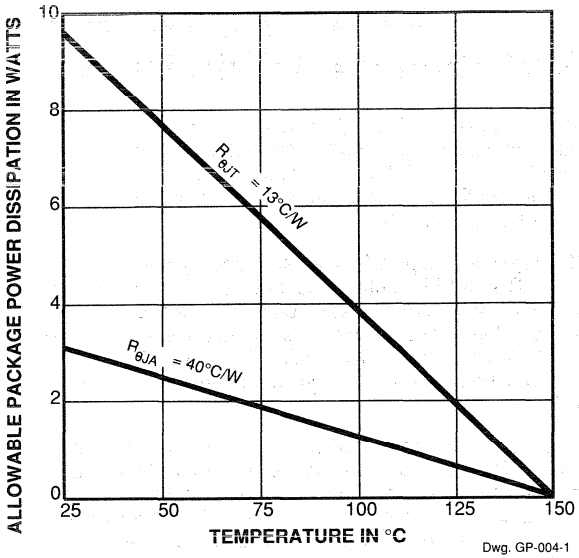
The bipolar outputs are capable of sinking up to 1.5 A and withstanding 50 V in the OFF state (sustaining voltages up to 35 V). Ground clamp and flyback diodes provide protection against inductive transients. Thermal protection circuitry disables the outputs when the chip temperature is excessive.

The UCN5804B is rated for operation over the temperature range of -20°C to +85°C. It is supplied in a 16-pin dual in-line plastic batwing package with a copper lead frame and heat-sinkable tabs for improved power dissipation capabilities.

FEATURES

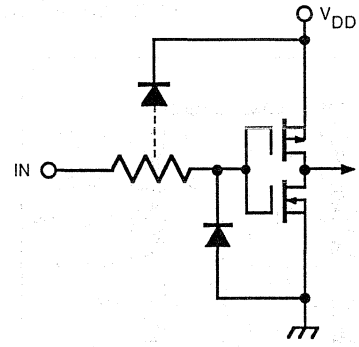
- 1.5 A Maximum Output Current
- 35 V Output Sustaining Voltage
- Wave-Drive, Two-Phase, and Half-Step Drive Formats
- Internal Clamp Diodes
- Output Enable and Direction Control
- Power-ON Reset
- Internal Thermal Shutdown Circuitry

Always order by complete part number: **UCN5804B** .



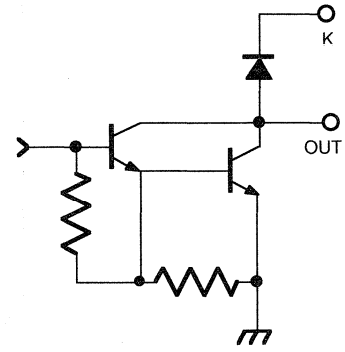
Dwg. GP-004-1

TYPICAL INPUT CIRCUIT



Dwg. EP-010-5

TYPICAL OUTPUT DRIVER



Dwg. EP-021-4

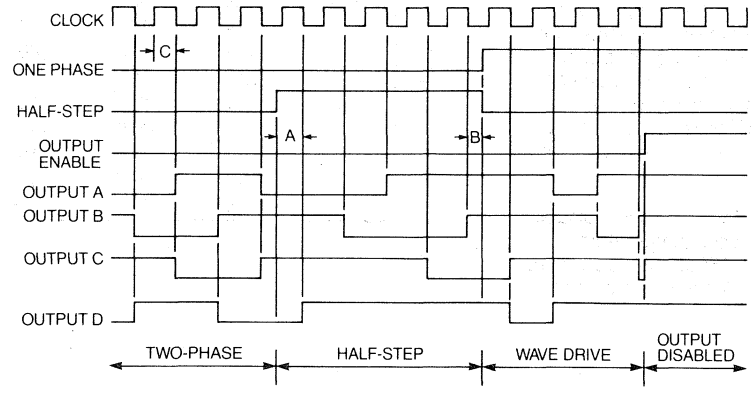
TRUTH TABLE

Drive Format	Pin 9	Pin 10
Two-Phase	L	L
One-Phase	H	L
Half-Step	L	H
Step-Inhibit	H	H

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $T_J \leq$ 150°C, V_{DD} = 4.5 V to 5.5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	10	50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = 1.25 A, L = 3 mH	35	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 700 mA	—	1.0	1.2	V
		I_{OUT} = 1 A	—	1.1	1.4	V
		I_{OUT} = 1.25 A	—	1.2	1.5	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	10	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 1.25 A	—	1.5	3.0	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	0.5	5.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.5	-5.0	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5 V	3.5	—	5.3	V
	$V_{IN(0)}$		-0.3	—	0.8	V
Supply Current	I_{DD}	2 Outputs ON	—	20	30	mA
Turn-Off Delay	t_{ON}	50% Step Inputs to 50% Output	—	—	10	µs
Turn-On Delay	t_{OFF}	50% Step Inputs to 50% Output	—	—	10	µs
Thermal Shutdown Temperature	T_J		—	165	—	°C

TIMING CONDITIONS



Dwg. No. W-110A

A. Minimum Data Set Up Time . . . . . **100 ns**
B. Minimum Data Hold Time . . . . . **100 ns**
C. Minimum Step Input Pulse Width . . . . . **500 ns**

APPLICATIONS INFORMATION

Internal power-ON reset (POR) circuitry resets $OUTPUT_A$ (and $OUTPUT_D$ in the two-phase drive format) to the ON state with initial application of the logic supply voltage. After reset, the circuit then steps according to the tables.

The outputs will advance one sequence position on the high-to-low transition of the STEP INPUT pulse. Logic levels on the HALF-STEP and ONE-PHASE inputs will determine the drive format (one-phase, two-phase, or half-step). The DIRECTION pin determines the rotation sequence of the outputs. Note that the STEP INPUT must be in the low state when changing the state of ONE-PHASE, HALFSTEP, or DIRECTION to prevent erroneous stepping.

All outputs are disabled (OFF) when OUTPUT ENABLE is at a logic high. If the function is not required, OUTPUT ENABLE should be tied low. In that condition, all outputs depend only on the state of the step logic.

During normal commutation of a unipolar stepper motor, mutual coupling between the motor windings can force the outputs of the UCN5804B below ground. This condition will cause forward biasing of the collector-to-substrate junction and source current from the output. For many L/R applications, this substrate current is high enough to adversely affect the logic circuitry and cause misstepping. External series diodes (Schottky are recommended for increased efficiency at low voltage operation) will prevent substrate current from being sourced through the outputs. Alternatively, external ground clamp diodes will provide a preferred current path from ground when the outputs are pulled below ground.

Internal thermal protection circuitry disables all outputs when the junction temperature reaches approximately 165°C. The outputs are enabled again when the junction cools down to approximately 145°C.

WAVE-DRIVE SEQUENCE

← DIRECTION = L

Half Step = L, One Phase = H				
Step	**A**	**B**	**C**	**D**
POR	ON	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF
3	OFF	OFF	ON	OFF
4	OFF	OFF	OFF	ON

→ DIRECTION = H

TWO-PHASE DRIVE SEQUENCE

← DIRECTION = L

Half Step = L, One Phase = L				
Step	**A**	**B**	**C**	**D**
POR	ON	OFF	OFF	ON
1	ON	OFF	OFF	ON
2	ON	ON	OFF	OFF
3	OFF	ON	ON	OFF
4	OFF	OFF	ON	ON

→ DIRECTION = H

HALF-STEP DRIVE SEQUENCE

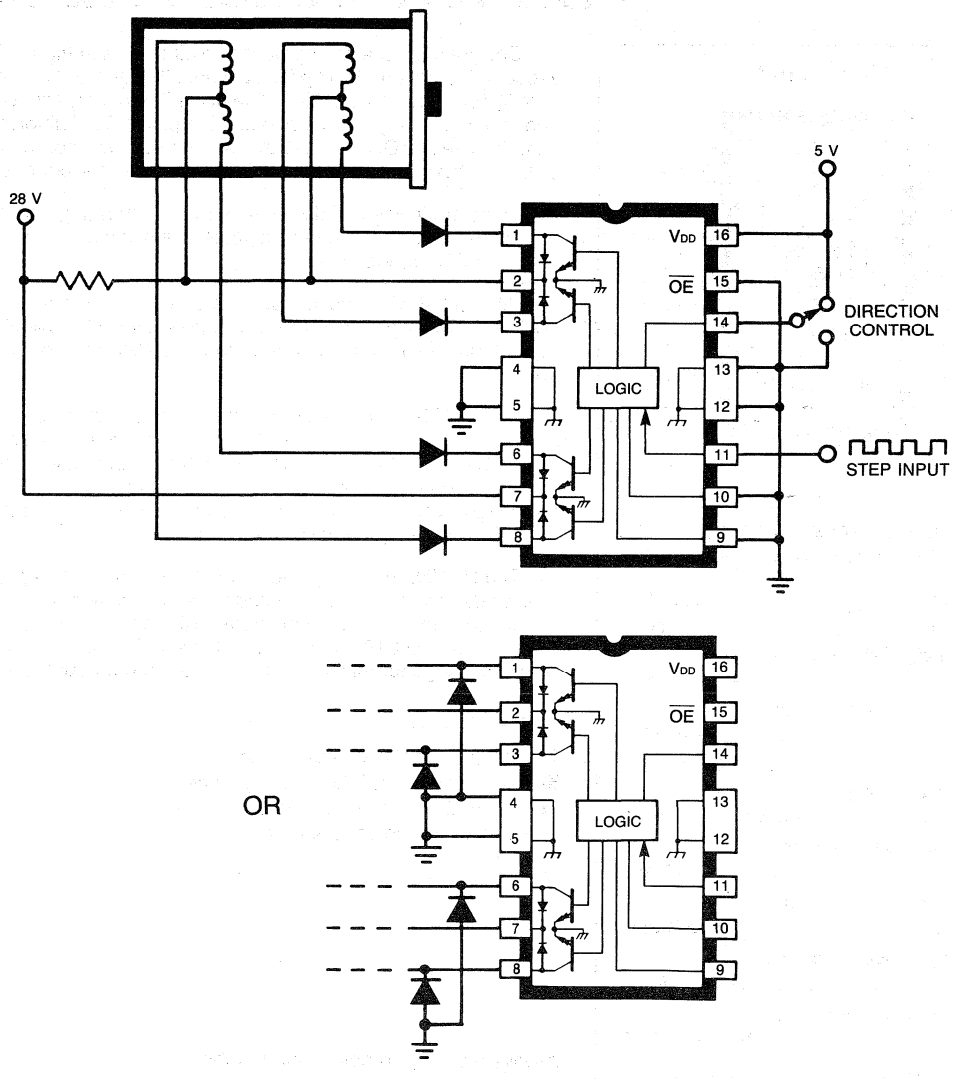
← DIRECTION = L

Half Step = H, One Phase = L				
Step	**A**	**B**	**C**	**D**
POR	ON	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	ON	ON	OFF	OFF
3	OFF	ON	OFF	OFF
4	OFF	ON	ON	OFF
5	OFF	OFF	ON	OFF
6	OFF	OFF	ON	ON
7	OFF	OFF	OFF	ON
8	ON	OFF	OFF	ON

→ DIRECTION = H

TYPICAL APPLICATION

L/R STEPPER-MOTOR DRIVE

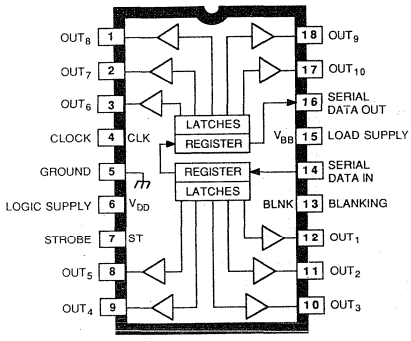


Dwg. EP-029

5810

BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

UCN5810A



Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **60 V**
(Suffix -1) . . . . . **80 V**
Logic Supply Voltage Range,
V_{DD} . . . . . **4.5 V to 15 V**
Driver Supply Voltage Range,
V_{BB} . . . . . **5.0 V to 60 V**
(Suffix-1) . . . . . **5.0 V to 80 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **-40 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5810A (dual in-line package) and UCN5810LW (small outline IC package) are electrically identical and share a common pin number assignment.

Designed for use as segment or digit drivers in high-voltage, vacuum-fluorescent display applications, the UCN5810A and UCN5810LW combine a 10-bit CMOS shift register, associated latches, and control circuitry (strobe and blanking) with 60 V bipolar source outputs. The BiMOS drivers can also be used with non-multiplexed LED displays within their output limitation of 40 mA per driver.

Selected devices (suffix-1) have maximum ratings of 80 V and 40 mA per driver. In all other respects, the basic part and the part with the "-1" suffix are identical.

BiMOS II devices have much faster data input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS circuits. Use of these drivers with TTL or DTL circuits may require appropriate input pull-up resistors to ensure an input logic high. A CMOS serial data output allows cascading for multiple drive-line applications required by many dot matrix, alpha-numeric, and bar graph displays.

The UCN5810A is supplied in an 18-pin dual in-line plastic package. Under normal operating conditions, this device will allow all outputs to source 25 mA continuously at ambient temperatures up to 60°C. The UCN5810LW is furnished in a wide-body, small-outline plastic package for minimum-area surface-mount applications.

FEATURES

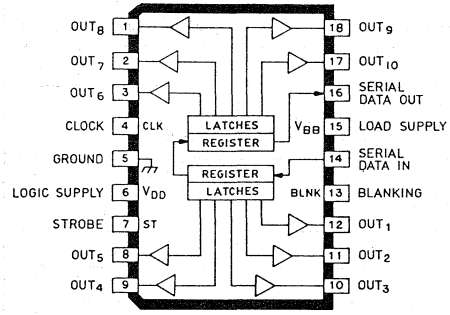
- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 60 V or 80 V Source Outputs
- Internal Pull-Down Resistors

Always order by complete part number:

Part Numbers	Package	Max. V_{BB}
UCN5810A UCN5810A-1	18-Pin DIP	60 V 80 V
UCN5810LW UCN5810LW-1	18-Lead SOIC	60 V 80 V

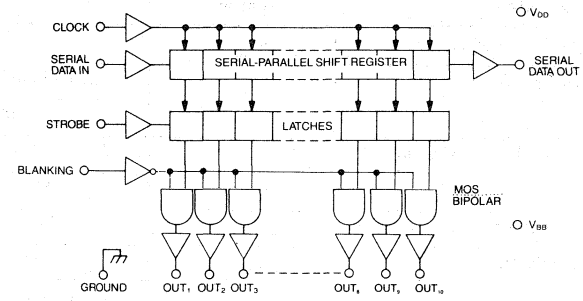
5810
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

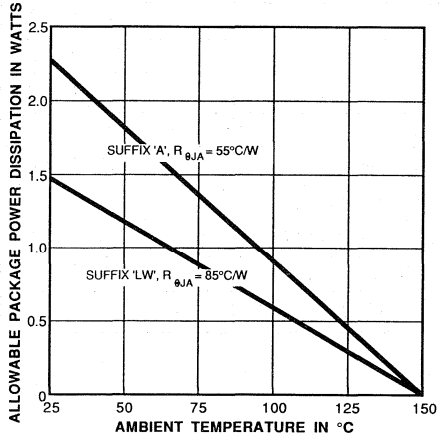
UCN5810LW



Dwg. No. A-14,355

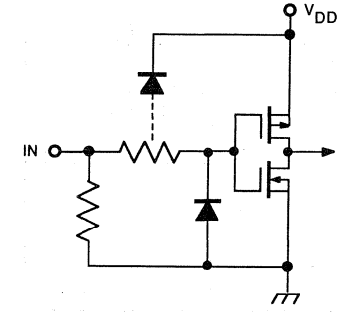
FUNCTIONAL BLOCK DIAGRAM





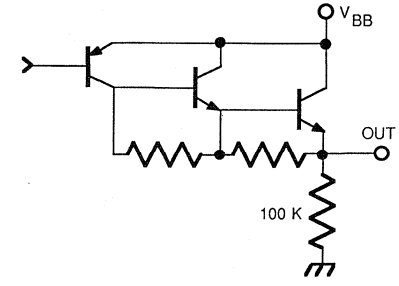
Dwg. GP-018A

TYPICAL INPUT CIRCUIT



Dwg. EP-010-

TYPICAL OUTPUT DRIVER



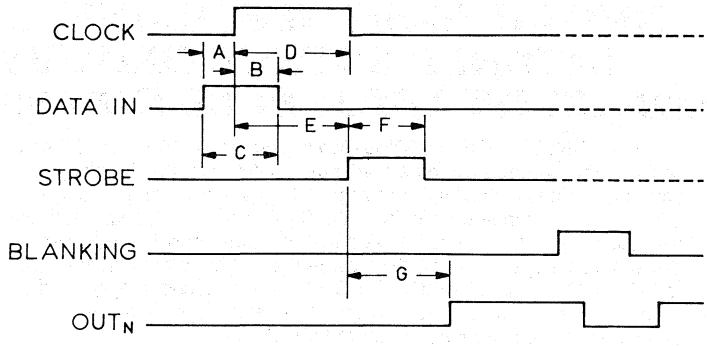
Dwg. EP-021-3

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	I_{OUT} = -25 mA, V_{BB} = 60 V	57.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V ("-1" only)	77.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = 60 V	400	850	µA
		V_{OUT} = 80 V = V_{BB} ("-1" only)	550	1150	µA
Output Leakage Current	I_{OUT}	T_A = +70°C	—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	V_{DD} = 5 V to 12 V	-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, All outputs open	—	13	mA
		All outputs OFF, All outputs open	—	200	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, Inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

5810
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg. No. 12,649A

TIMING CONDITIONS
(V_{DD} = 5 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transition . . . . . **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

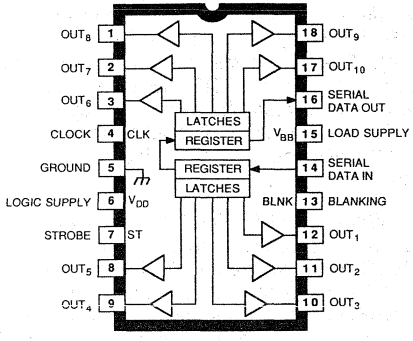
Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⌐¯	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⌐¯	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	¯⌐	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5810-F

BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

UCN5810AF



Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} . . . . . **15 V**
Driver Supply Voltage, V_{BB} . . . . . **60 V**
(suffix '-1') . . . . . **80 V**
Continuous Output CurrentRange,
I_{OUT} . . . . . **-40 to +15 mA**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation, P_D
(UCN5810AF) . . . . . **2.27 W***
(UCN5810LWF) . . . . . **1.29 W†**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

* Derate at rate of 18 mW/°C above T_A = +25°C
† Derate at rate of 10 mW/°C above T_A = +25°C

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5810AF (dual in-line package) and UCN5810LWF (small-outline IC package) are electrically identical and share a common pin number assignment

The UCN5810AF and UCN5810LWF combine a 10-bit CMOS shift register and accompanying data latches, control circuitry, bipolar sourcing outputs with DMOS active pull-downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. Selected devices (suffix '-1') have maximum output ratings of 80 V. The UCN5810AF/LWF feature reduced supply requirements (active DMOS pull-downs) and lower saturation voltages when compared with the industry-standard UCN5810A.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V logic supply, serial-data input rates are typically over 5 MHz, with significantly higher speeds obtainable at 12 V. Use with TTL may require appropriate pull-up resistors to insure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCN5811A (12 bits), UCN5812AF/EPF (20 bits) and UCN5818AF/EPF (32 bits).

The UCN5810AF/LWF output source drivers are PNP-NPN Darlingtons capable of sourcing up to 40 mA. The DMOS active pull-downs are capable of sinking up to 15 mA. For inter-digit blanking, all of the output drivers can be disabled and the DMOS sink drivers turned on by the BLANKING input high.

The UCN5810AF is furnished in an 18-pin dual in-line plastic package. The UCN5810LWF is furnished in a wide-body, small-outline plastic package (SOIC) with gull-wing leads and 0.300" lead row spacing. Copper lead frames, reduced supply current requirements, and lower output saturation voltages allow both the UCN5810AF and the UCN5810LWF to source 25 mA from all outputs continuously, over the entire operating temperature range.

FEATURES

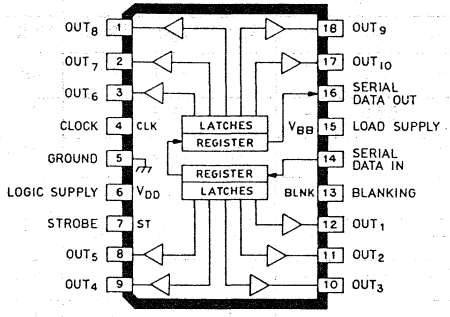
- High-Speed Source Drivers
- 60 V or 80 V Minimum Output Breakdown
- Active DMOS Pull-Downs
- Low Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- 3.3 MHz Minimum Data Input Rate
- Improved Replacements for TL4810B

Always order by complete part number:

Part Numbers	Package	Max. V_{BB}
UCN5810AF UCN5810AF-1	18-Pin DIP	60 V 80 V
UCN5810LWF UCN5810LWF-1	18-Lead SOIC	60 V 80 V

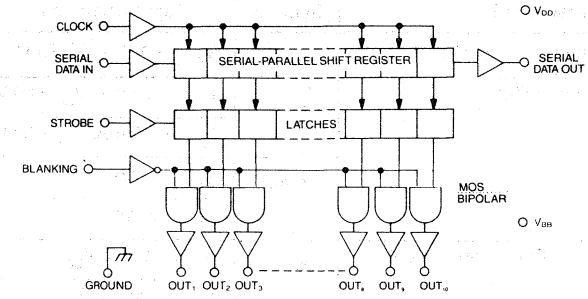
5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

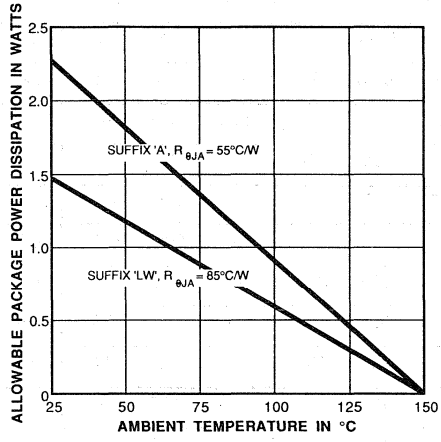
UCN5810LWF



Dwg. No. A-14,355

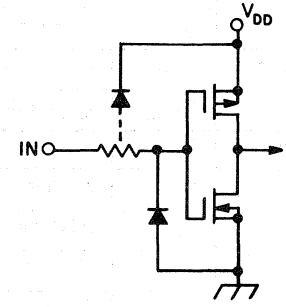
FUNCTIONAL BLOCK DIAGRAM





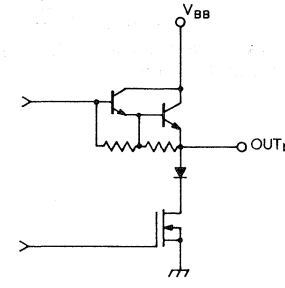
Dwg. GP-018A

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,03

TYPICAL OUTPUT DRIVER



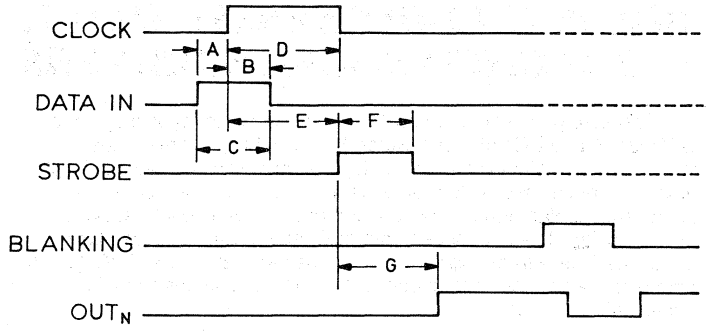
Dwg. No. A-14,21

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V (UCN5810AF/LWF) or 80 V (suffix '-1') unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	0.7	2.0	—	0.7	2.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out of (sourcing) the specified device pin.
* UCN5810AF-1 and UCN5810LWF-1 only.

5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS



Dwg. No. 12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transistion . . . . . **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

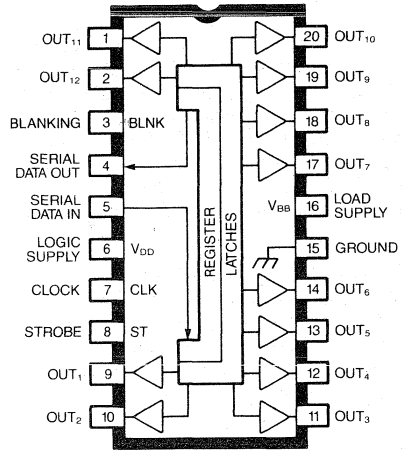
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Blanking	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	⌐	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⌐	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	¬	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5811

BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg. No. W-180

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} ..... **15 V**
Driver Supply Voltage,
V_{BB} (UCN5811A) ..... **60 V**
(UCN5811A-1) ..... **80 V**
Continuous Output Current,
I_{OUT} ..... **-40 to +25 mA**
Input Voltage Range,
V_{IN} ..... **0.3 V to V_{DD} +0.3 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Designed primarily for use with vacuum-fluorescent displays, the UCN5811A and UCN5811A-1 Smart Power BiMOS II drivers feature low-output saturation voltages and high output switching speed. These devices contain CMOS shift registers, data latches, and control circuitry, and bipolar high-speed sourcing outputs with DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interface with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines.

The UCN5811A features 60 V and -40 mA output ratings, allowing it to be used in many other peripheral power driver applications. Selected devices (UCN5811A-1) have maximum output ratings of 80 V. In all other respects, the UCNL5811A and UCNL5811A-1 are identical.

The UCN5811A can be used as an improved replacement tor the SN75512B. The Sprague devices do not require special power-up sequencing.

The UCN5811A and UCN5811A-1 have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high.

Both devices are supplied in 20-pin plastic dual in-line packages. They can be operated over the ambient temperature range of -20°C to +85°C. Copper lead frames and low output saturation voltages allow all outputs to be operated at 25 mA continuously at ambient temperatures of up to 76°C .

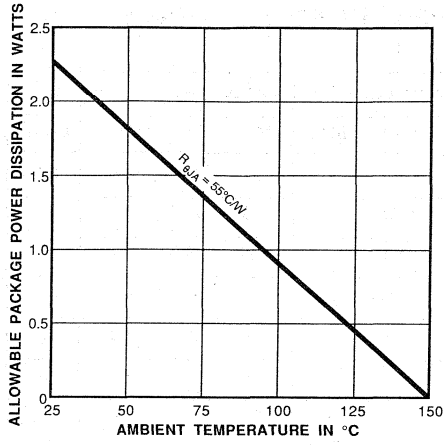
FEATURES

- 3.3 MHz Guaranteed Data Input Rate
- Low-Power CMOS Logic and Latches
- High-Speed Source Drivers
- Active Pull-Downs
- Low-Output Saturation Voltages
- Improved Replacement for SN75512B

Always order by complete part number:

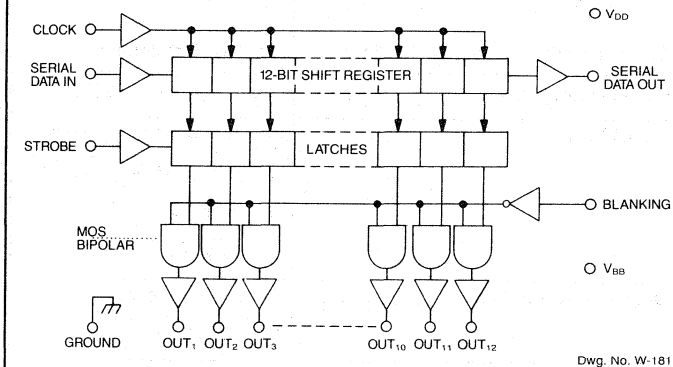
Part Number	Max. V_{BB}
UCN5811A	60 V
UCN5811A-1	80 V

5811
BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER



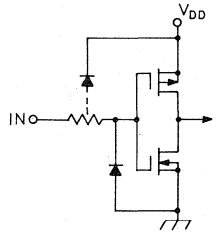
Dwg. GS-004-1

FUNCTIONAL BLOCK DIAGRAM



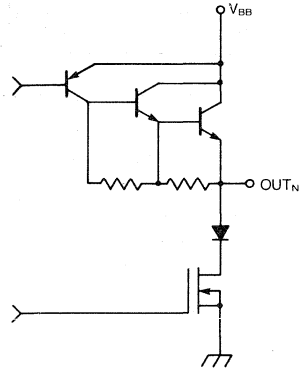
Dwg. No. W-181

TYPICAL INPUT CIRCUIT



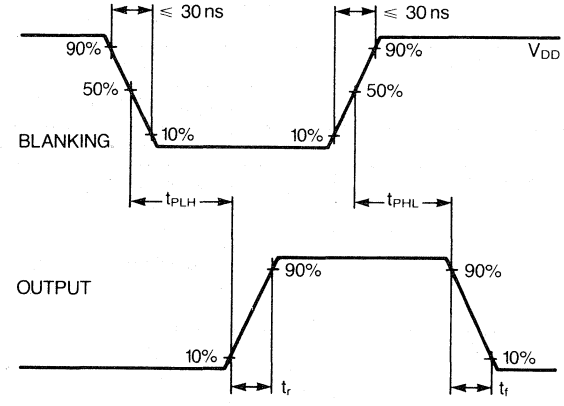
Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



Dwg. No. W-182

TIMING WAVESHAPES



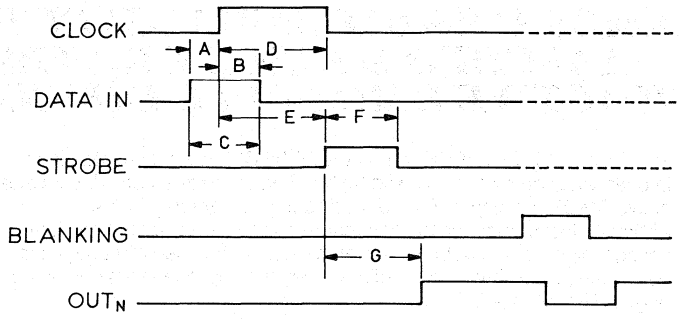
Dwg. No. W-184

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V (UCN5811A) or 80 V (UCN5811A-1), unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(H)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(L)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.0	V
Output Pull-Down Current	$I_{OUT(L)}$	V_{OUT} = 10 V to V_{BB}	2.5	4.0	—	—	—	—	mA
		V_{OUT} = 40 V to V_{BB}	—	—	—	15	18	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(H)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(L)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(H)}$	All Outputs High	—	3.0	5.0	—	15	20	mA
	$I_{DD(L)}$	All Outputs Low	—	2.5	4.0	—	7.0	10	mA
	$I_{BB(H)}$	Outputs High, No Load	—	7.5	12	—	7.5	12	mA
	$I_{BB(L)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF	—	300	550	—	125	150	ns
	t_{PLH}	C_L = 30 pF	—	250	450	—	170	200	ns
Output Fall Time	t_f	C_L = 30 pF	—	1000	1250	—	250	300	ns
Output Rise Time	t_r	C_L = 30 pF	—	150	170	—	150	170	ns

Negative current is defined as coming out of (sourcing) the specified device pin.
* UCN5811A-1 only.

5811
BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER



Dwg. No. A-12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
C. Minimum Data Pulse Width ..... **150 ns**
D. Minimum Clock Pulse Width ..... **150 ns**
E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
F. Minimum Strobe Pulse Width ..... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition ..... **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information toward the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

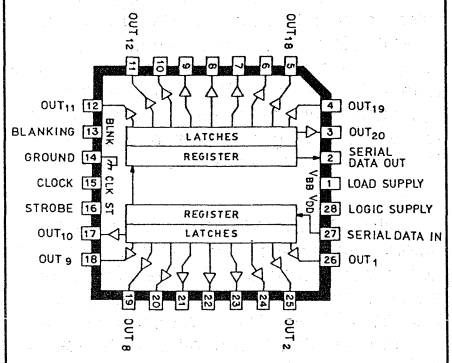
Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⊓	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⊓	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⊔	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5812-F

BiMOS II 20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

UCN5812EPF



Dwg. No. A-14,356

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} . . . . . **15 V**
Driver Supply Voltage, V_{BB} . . . . . **60 V**
(suffix '-1') . . . . . **80 V**
Continuous Output Current Range,
I_{OUT} . . . . . **-40 to +15 mA**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} +0.3 V**
Package Power Dissipation, P_D
(UCN5812AF) . . . . . **3.12 W***
(UCN5812EPF) . . . . . **1.92 W†**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

* Derate at rate of 25 mW/°C above T_A = + 25°C
† Derate at rate of 15 mW/°C above T_A = + 25°C

Caution: Allegro CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5812AF (dual in-line package) and UCN5812EPF (PLCC package) are electrically identical and share a common pin number assignment

The UCN5812AF/EPF combine a 20-bit CMOS shift register, data latches, and control circuitry with high-voltage bipolar source drivers and active DMOS pull-downs for reduced supply current requirements. Although designed primarily for vacuum-fluorescent displays, the high-voltage, high-current outputs also allow them to be used in many other peripheral power driver applications. They are improved versions of the original UCN5812A/EP.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Data input rates are typically over 5 MHz with a 5 V logic supply, and over 7.5 MHz at 12 V. Especially useful for inter-digit blanking, the BLANKING input disables the output source drives and turns on the DMOS sink drivers. Use with TTL may require the use of appropriate pull-up resistors to insure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCN5810AF/LWF (10 bits), UCN5811A (12 bits), and UCN5818AF/EPF (32 bits).

The output source drivers are high-voltage PNP-NPN Darlingtons with a minimum breakdown of 60 V and are capable of sourcing up to 40 mA. Selected devices (suffix '-1') feature 80 V minimum breakdowns. The DMOS active pull-downs are capable of sinking up to 15 mA.

The UCN5812AF is supplied in a 28-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. For surface-mounting, the UCN5812EPF is furnished in 28-lead plastic chip carrier (quad pack) with 0.050"(1.22 mm) centers. Copper lead-frames, reduced supply current requirements and lower output saturation voltages, allow continuous operation, with all outputs sourcing 25 mA, of the UCN5812AF over the operating temperature range, and the UCN5812EPF up to +75°C.

FEATURES

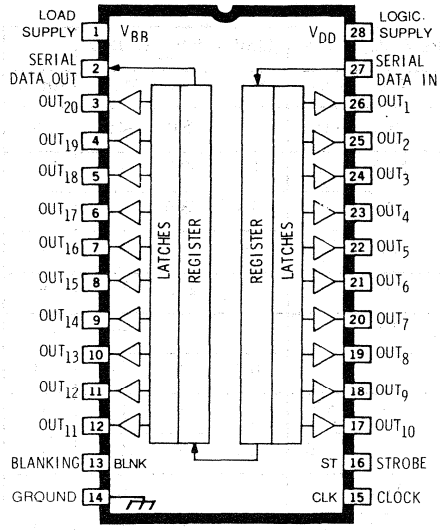
- High-Speed Source Drivers
- 60 V or 80 V Source Outputs
- Active DMOS Pull-Downs
- Low-Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- 3.3 MHz Minimum Data Input Rate
- Reduced Supply Current Requirements
- Improved Replacement for TL5812

Always order by complete part number:

Part Number	Package	Max V_{BB}
UCN5812AF UCN5812AF-1	28 Pin DIP	60 V 80 V
UCN5812EPF UCN5812EPF-1	28-Lead PLCC	60 V 80 V

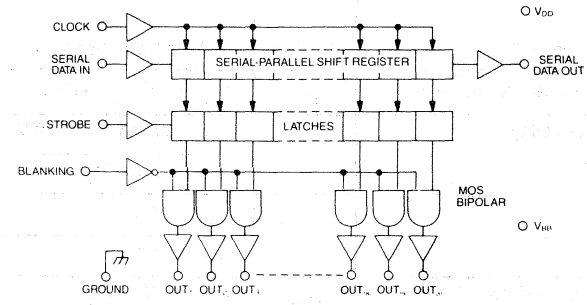
5812-F
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

UCN5812AF

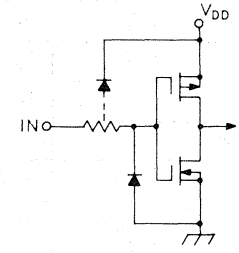


Dwg. No. A-12,270

FUNCTIONAL BLOCK DIAGRAM

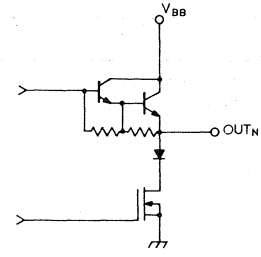


TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



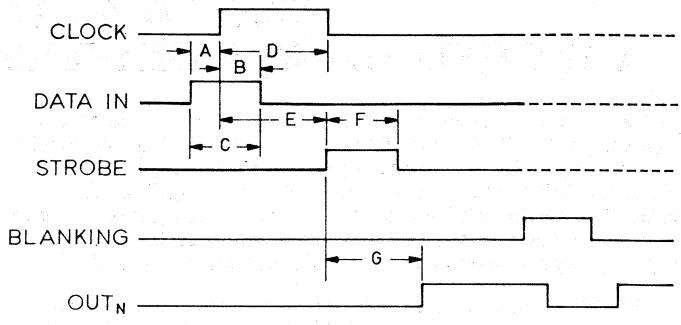
Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{BB} = 60 V (UCN5812AF/EPF) or 80 V (suffix '-1') unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	1.5	2.5	—	1.5	2.5	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out ot (sourcing) the specified device pin.
* UCN5812AF-1 and UCN5812EPF-1 only.

5812-F
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS



Dwg. No. 12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transistion . . . . . **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

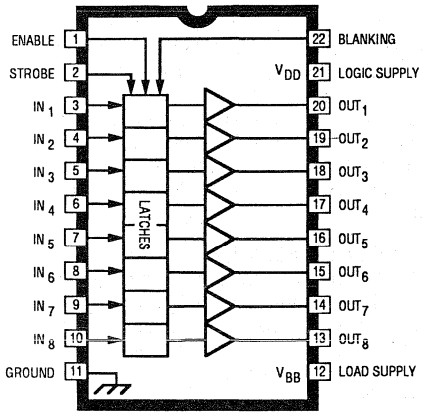
Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⊓	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⊓	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⊔	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5815

BiMOS II 8-BIT LATCHED SOURCE DRIVERS

UCN5815A



Dwg. No. A-10,987

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **60 V**
(Suffix '-1') . . . . . **80 V**
Logic Supply Voltage Range, V_{DD} . . . . . **4.5 V to 15 V**
Load Supply Voltage Range, V_{BB} . . . . . **5.0 V to 60 V**
(Suffix '-1') . . . . . **5.0 V to 80 V**
Input Voltage Range, V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current, I_{OUT} . . . . . **-40 mA**
Package Power Dissipation, P_D
(DIP) . . . . . **2.5 W***
(PLCC) . . . . . **2.27 W***
Operating Temperature Range, T_A . . . . . **-20°C to +85°C**
Storage Temperature Range, T_S . . . . . **-55°C to +150°C**

* Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily for use with high-voltage vacuum-fluorescent displays, the UCN5815A and UCN5815EP BiMOS II integrated circuits consist of eight NPN Darlington source drivers with output pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions. Selected devices (suffix "-1") have maximum output ratings of 80 V and 40 mA per driver. In all other respects, they are identical to the 60 V devices without the suffix.

BiMOS II devices have considerably better data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. TTL or DTL circuits may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. All eight outputs can be activated simultaneously at ambient temperatures in excess of 75°C. To simplify printed wiring board layout, output connections are opposite the inputs. A minimum component display subsystem, requiring few or no discrete components, can be assembled using the UCN5815A/EP with the UCN5810A/LW, UCN5812A/EP, or UCN5818A/EP serial-to-parallel latched driver.

Suffix 'A' devices are furnished in a standard 22-pin plastic DIP; suffix 'EP' indicates a 28-lead PLCC.

FEATURES

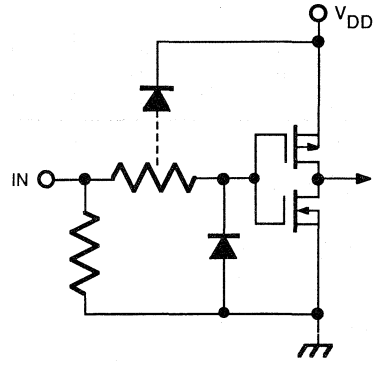
- 4.4 MHz Minimum Date-Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 4.5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	I_{OUT} = -25 mA, V_{BB} = 60 V	57.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V, Suffix "-1" only	77.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	µA
		V_{BB} = V_{OUT} = 80 V, Suffix "-1" only	550	1150	µA
Output Leakage Current	I_{OUT}	T_A = 70°C	—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10.5	mA
		All outputs OFF, All outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

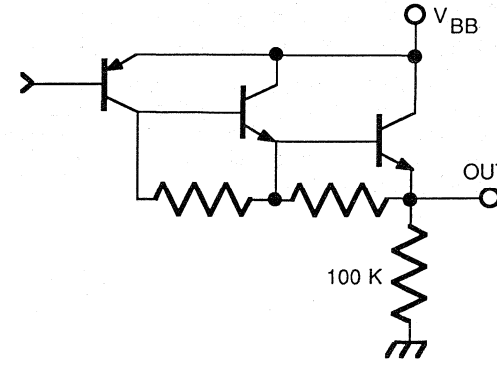
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL INPUT CIRCUIT



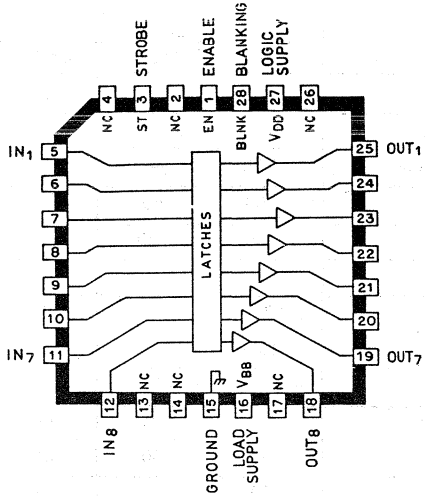
Dwg. No. EP-010-4

TYPICAL OUTPUT DRIVER

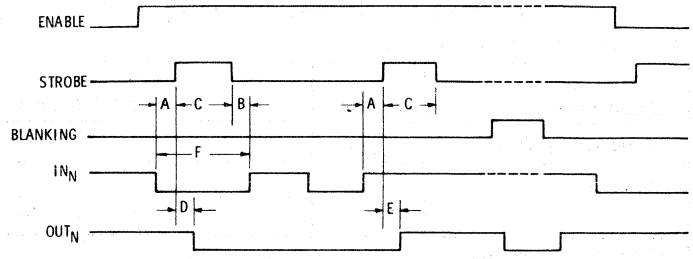


Dwg. No. EP-021-3

UCN5815EP



Dwg. No. A-14,357



Dwg. No. A-10,991

TIMING CONDITIONS

(V_{DD} = 5 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**

B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . . **50 ns**

C. Minimum Strobe Pulse Width . . . . . **125 ns**

D. Typical Time Between Strobe Activation and Output ON to OFF Transition . . . . . **5.0 µs**

E. Typical Time Between Strobe Activation and Output OFF to ON Transition . . . . . **500 ns**

F. Minimum Data Pulse Width . . . . . **225 ns**

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

The timing conditions shown above guarantee a 4.4 MHz minimum data input rate with a 5 V supply. Typically, input rates above 5 MHz are permitted. With a 12 V supply, rates in excess of 10 MHz are possible.

TRUTH TABLE

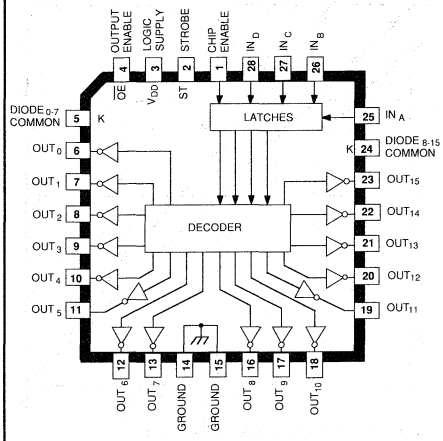
INPUTS				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = Irrelevant
t-1 = Previous Output State
t = Present Output State

5816

4-TO-16 LINE LATCHED DECODER/DRIVERS

UCN5816EP



Dwg. PP-030

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{CE} . . . . . **60 V**
Logic Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Output Current, I_C . . . . . **500 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5816A and UCN5816EP 4-to-16 line latched decoder/drivers combine low-power CMOS inputs and logic with 16 high-current, high-voltage bipolar outputs. The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure an input logic high. The logic operates over a supply range of 5 V to 12 V. A CHIP ENABLE function can be used with two devices for 5-to-32 line decoding applications.

The 16 bipolar power outputs are open-collector 60 V Darlington drivers capable of sinking 350 mA continuously. Internal transient-suppression diodes provide protection for use with inductive loads. Other (3-to-8 line) addressable latched drivers are the UCN4807A and UCN4808A.

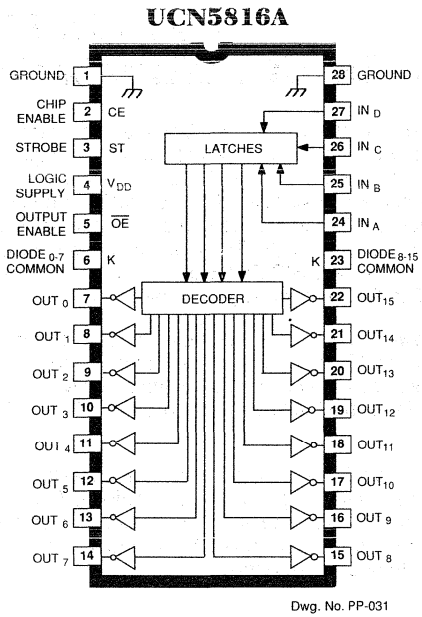
The UCN5816A is supplied in a 28-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. The UCN5816EP is furnished in a 28-lead plastic chip carrier (quad pack) for minimum-area surface-mount applications. Both devices will drive 350 mA loads continuously over the full operating temperature range.

FEATURES

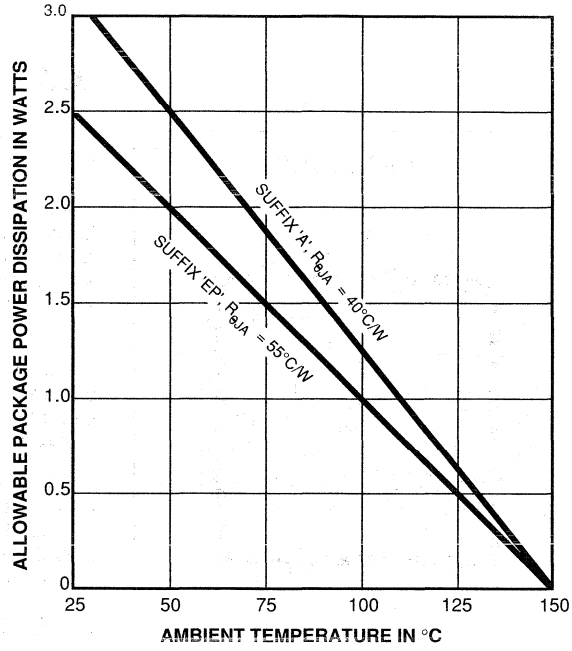
- Addressable Data Entry
- 60 V Minimum Output Breakdown
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Output Transient Protection
- Output Enable and Strobe Functions

Always order by complete part number:

Part Number	Package
UCN5816A	28-Pin DIP
UCN5816EP	28-Lead PLCC

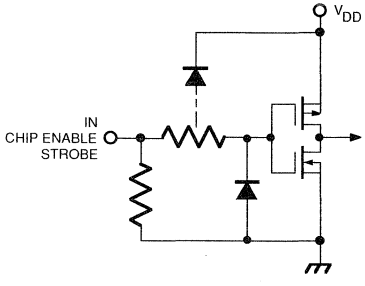


Dwg. No. PP-031

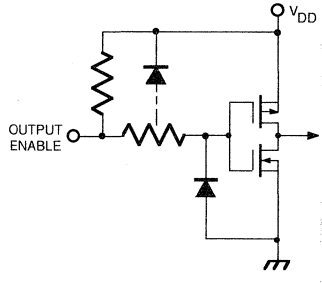


Dwg. GP-028-1

TYPICAL INPUT CIRCUITS

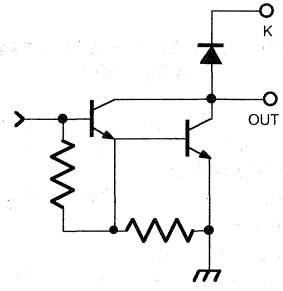


Dwg. EP-010-4



Dwg. EP-010-3

TYPICAL OUTPUT DRIVER

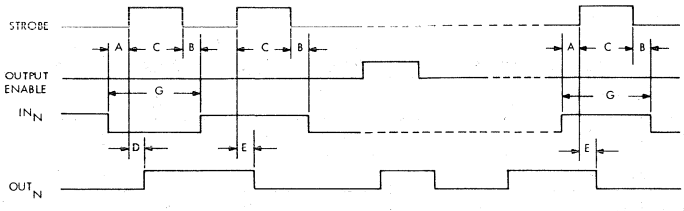


Dwg. EP-021-4

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{CE} = 60 V, T_A = +25°C	—	—	50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		-0.3	—	0.8	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 5.0 V	3.5	—	5.3	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200	—	kΩ
		V_{DD} = 5.0 V	100	600	—	kΩ
Supply Current	$I_{DD(ON)}$	V_{DD} = 12 V, Outputs Open	—	2.0	3.0	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	1.5	mA
	$I_{DD(OFF)}$	All Drivers OFF, All Inputs = 0 V, OE = V_{DD} = 5.0 V	—	—	100	µA
		All Drivers OFF, All Inputs = 0 V, OE = V_{DD} = 12 V	—	—	200	µA
Clamp Diode Leakage Current	I_R	V_R = 60 V, T_A = +25°C	—	—	50	µA
		V_R = 60 V, T_A = +70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.5	2.0	V

5816
4-TO-16 LINE LATCHED DECODER/DRIVERS



p/o Dwg. No. A-10,895A

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... **50 ns**

B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... **50 ns**

C. Minimum Strobe Pulse Duration ..... **125 ns**

D. Typical Time Between Strobe Activation and Output On to Off Transition ..... **500 ns**

E. Typical Time Between Strobe Activation and Output Off to On Transition ..... **500 ns**

G. Minimum Data Pulse Duration ..... **225 ns**

Information present at the inputs is transferred to the latches when the STROBE is high. The latches will continue to accept new data as long as the STROBE is held high. With the STROBE in the low state, no information can be loaded into the latches. Depending on the four address inputs, the 4-to-16 line decoder enables one of the 16 output sink drivers. When the OUTPUT ENABLE is high, all of the outputs are disabled (OFF) without affecting the information stored in the latches. When the OUTPUT ENABLE is low, the outputs are controlled by the information in the latches. When the CHIP ENABLE is low, all of the outputs are disabled (OFF). With two decoder/drivers and an inverter, the CHIP ENABLE function can be used for 5-to-32 line decoding applications.

TRUTH TABLE

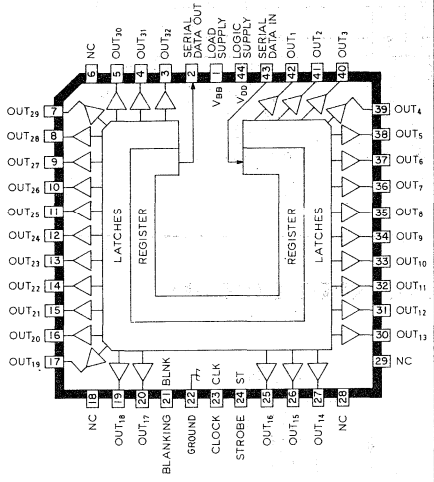
STROBE	CHIP ENABLE	IN_D (MSB)	IN_C	IN_B	IN_A (LSB)	OUTPUT ENABLE	OUTPUTS (OFF unless otherwise specified)
1	1	0	0	0	0	0	OUT_0 ON
1	1	0	0	0	1	0	OUT_1 ON
1	1	0	0	1	0	0	OUT_2 ON
1	1	0	0	1	1	0	OUT_3 ON
1	1	0	1	0	0	0	OUT_4 ON
1	1	0	1	0	1	0	OUT_5 ON
1	1	0	1	1	0	0	OUT_6 ON
1	1	0	1	1	1	0	OUT_7 ON
1	1	1	0	0	0	0	OUT_8 ON
1	1	1	0	0	1	0	OUT_9 ON
1	1	1	0	1	0	0	OUT_{10} ON
1	1	1	0	1	1	0	OUT_{11} ON
1	1	1	1	0	0	0	OUT_{12} ON
1	1	1	1	0	1	0	OUT_{13} ON
1	1	1	1	1	0	0	OUT_{14} ON
1	1	1	1	1	1	0	OUT_{15} ON
0	1	X	X	X	X	0	Q_O
X	0	X	X	X	X	X	All OFF
X	X	X	X	X	X	1	All OFF

Q_O = The output condition prior to the high-to-low transition of the STROBE input.
X = Irrelevant

5818-F

BiMOS II 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

UCN5818EPF



Dwg. No. A-14,218

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} . . . . . **15 V**
Driver Supply Voltage, V_{BB} . . . . . **60 V**
(suffix '-1') . . . . . **80 V**
Continuous Output Current,
I_{OUT} . . . . . **-40 to +15 mA**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} +0.3 V**
Package Power Dissipation, P_D
(UCN5818AF) . . . . . **3.5 W***
(UCN5818EPF) . . . . . **2.5W†**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

* Derate at rate of 28 mW/°C above T_A = + 25°C
† Derate at rate of 20 mW/°C above T_A = + 25°C

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily for use with vacuum fluorescent displays, the UCN5818AF and UCN5818EPF smart power BiMOS II drivers combine CMOS shift registers, data latches, and control circuitry, with bipolar high-speed sourcing outputs and DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interfacing with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Both devices feature 60 V and -40 mA output ratings, allowing them to be used in many other peripheral power driver applications. Selected devices (suffix '-1') have maximum output ratings of 80 V. In all other respects, devices with and without the '-1' suffix are identical.

These smart power drivers have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high. All devices can be operated over the ambient temperature range of -20°C to +85°C.

The UCN5818AF is supplied in a 40-pin plastic dual in-line package with 0.600" (15.24 mm) row spacing. A copper lead frame, reduced supply current requirement, and low output saturation voltage permits operation with minimum junction temperature rise. The 'A' package allows all 32 outputs to be operated at -25 mA continuously over the operating temperature range.

For high-density packaging applications, the UCN5818EPF is furnished in a 44-lead plastic chip carrier (quad pack) for surface mounting on solder lands with 0.050" (1.27 mm) centers. The PLCC allows -25 mA continuous operation of all outputs simultaneously at ambient temperatures to 60°C.

Similar devices are available as the UCN5810AF/LWF (10 bits), UCN5811A (12 bits), and UCN5812AF/EPF (20 bits).

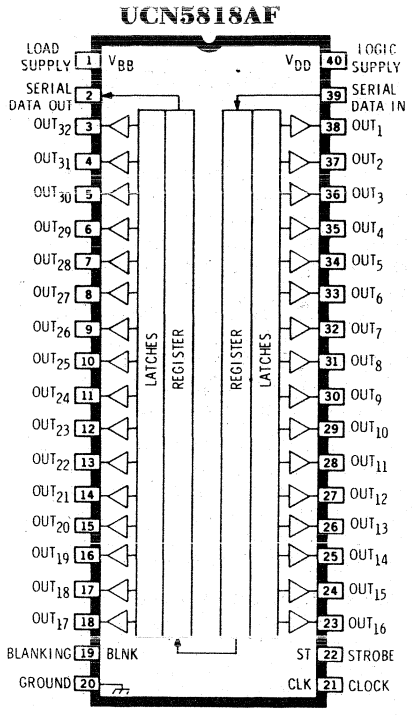
FEATURES

- 60 V or 80 V Source Outputs
- High-Speed Source Drivers
- Active DMOS Pull-Downs
- Low-Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- 3.3 MHz Minimum Data Input Rate
- Reduced Supply Current Requirements
- Improved Replacements for SN75518N/FN

Always order by complete part number:

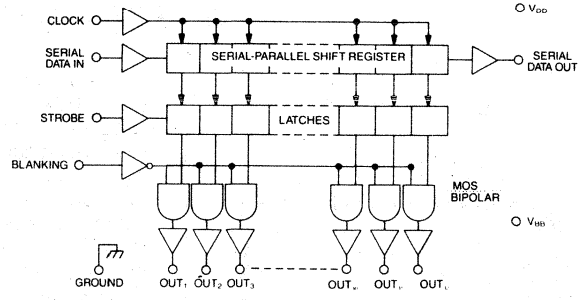
Part Numbers	Package	Max. V_{BB}
UCN5818AF	40-Pin DIP	60 V
UCN5818AF-1		80 V
UCN5818EPF	44-Lead PLCC	60 V
UCN5818EPF-1		80 V

5818-F
32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

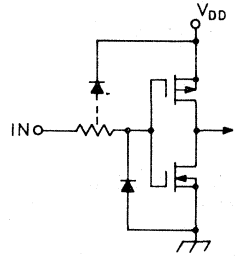


Dwg. No. A-12,269A

FUNCTIONAL BLOCK DIAGRAM

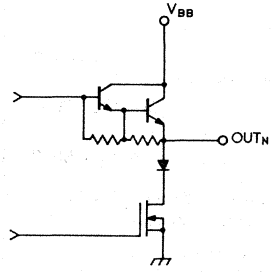


TYPICAL INPUT CIRCUIT

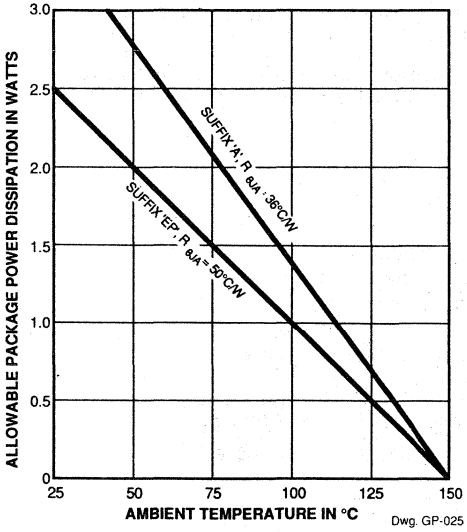


Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219



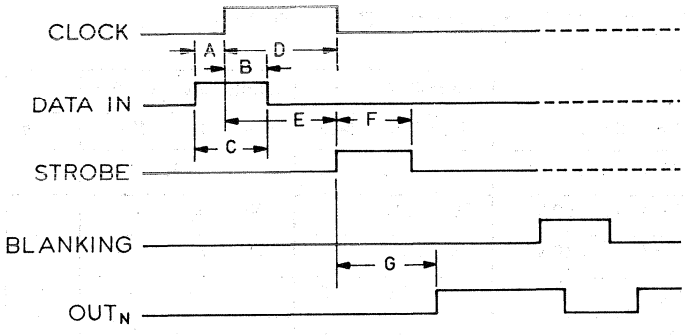
Dwg. GP-025

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{BB} = 60 V (UCN5818AF/EPF) or 80 V (suffix '-1') unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	3.0	6.0	—	3.0	6.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out ot (sourcing) the specified device pin.
* UCN5818AF-1 and UCN5818EPF-1 only.

5818-F
32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS



Dwg. No. 12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
C. Minimum Data Pulse Width ..... **150 ns**
D. Minimum Clock Pulse Width ..... **150 ns**
E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
F. Minimum Strobe Pulse Width ..... **100 ns**
G. Typical Time Between Strobe Activation and Output Transistion ..... **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

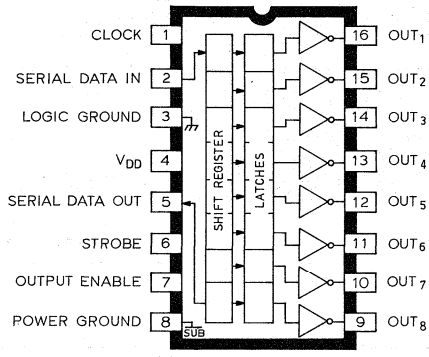
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5821 THRU 5823

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. PP-026

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{OUT}
(UCN5821A) . . . . . **50 V**
(UCN5822A) . . . . . **80 V**
(UCN5823A) . . . . . **100 V**
Logic Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **500 mA**
Package Power Dissipation,
P_D . . . . . **2.08 W***
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*Derate at the rate of 16.7 mW/°C above T_A = +25°C

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

A combination of bipolar and MOS technology gives the Series UCN5820A an interface flexibility beyond the reach of standard logic buffers and power driver arrays. The three devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers. Except for maximum driver output voltage ratings, the UCN5821A, UCN5822A, and UCN5823A are identical.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL and DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

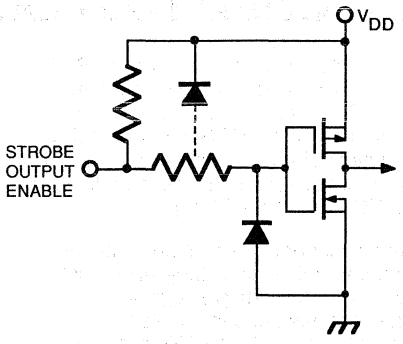
FEATURES

- 3.3 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic & Latches
- High-Voltage Current-Sink Outputs
- 16-Pin Dual In-Line Plastic Package

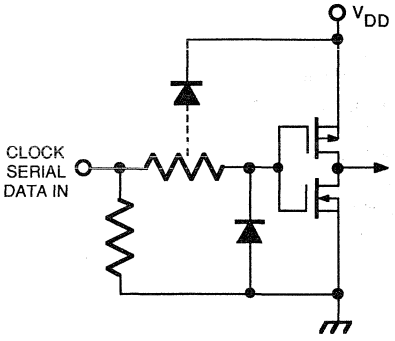
Always order by complete part number:

Part Number	Max. V_{OUT}
UCN5821A	50 V
UCN5822A	80 V
UCN5823A	100 V

TYPICAL INPUT CIRCUITS

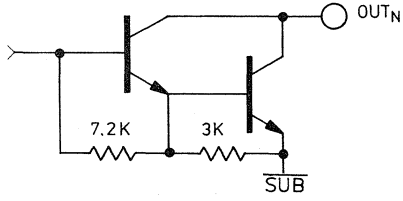


Dwg. No. EP-010-3



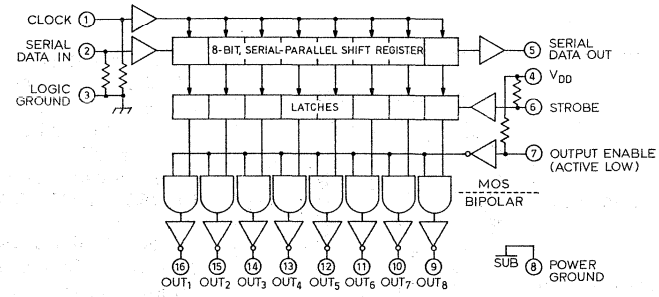
Dwg. No. EP-010-4

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,314

FUNCTIONAL BLOCK DIAGRAM

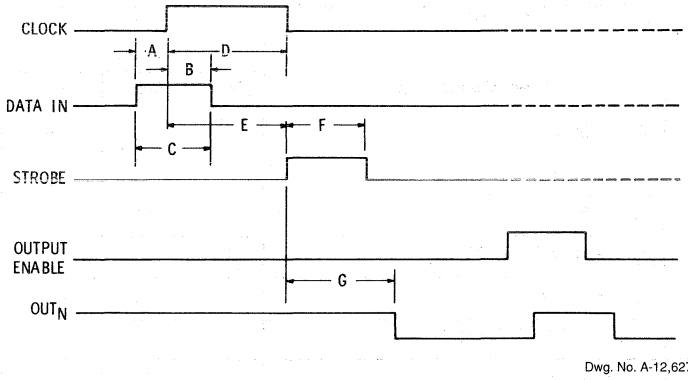


Dwg. FP-013

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	90%	79%	72%	65%	57%
7	100%	90%	82%	74%	65%
6	100%	100%	96%	86%	76%
5	100%	100%	100%	100%	91%
4	100%	100%	100%	100%	100%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, (unless otherwise specified).

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	UCN5821A	V_{OUT} = 50 V	—	50	µA
			V_{OUT} = 50 V, T_A = +70°C	—	100	µA
		UCN5822A	V_{OUT} = 80 V	—	50	µA
			V_{OUT} = 80 V, T_A = +70°C	—	100	µA
		UCN5823A	V_{OUT} = 100 V	—	50	µA
			V_{OUT} = 100 V, T_A = +70°C	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	I_{OUT} = 100 mA	—	1.1	V
			I_{OUT} = 200 mA	—	1.3	V
			I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	V_{DD} = 12 V	10.5	—	V
			V_{DD} = 10 V	8.5	—	V
			V_{DD} = 5.0 V	3.5	—	V
Input Resistance	R_{IN}	ALL	V_{DD} = 12 V	50	—	kΩ
			V_{DD} = 10 V	50	—	kΩ
			V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One Driver ON, V_{DD} = 12 V	—	4.5	mA
			One Driver ON, V_{DD} = 10 V	—	3.9	mA
			One Driver ON, V_{DD} = 5.0 V	—	2.4	mA
	$I_{DD(OFF)}$	ALL	V_{DD} = 5.0 V, All Drivers OFF, All Inputs = 0 V	—	1.6	mA
			V_{DD} = 12 V, All Drivers OFF, All Inputs = 0 V	—	2.9	mA



Dwg. No. A-12,627

TIMING CONDITIONS
(V_{DD} = 5.0 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transition . . . . . **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

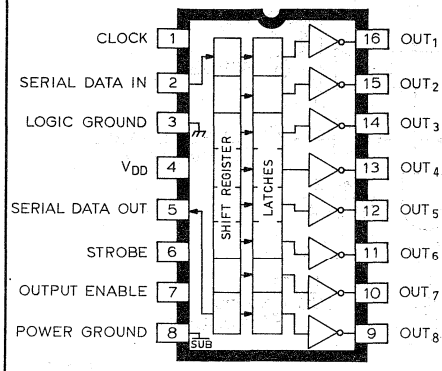
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⊓	H R_1 R_2 ..... R_7	R_7				
L	⊓	L R_1 R_2 ..... R_7	R_7				
X	⊔	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5824

BiMOS II 8-BIT SERIAL-INPUT, LATCHED SATURATED SINK DRIVER



Dwg. PP-026

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{CE} . . . . . **50 V**
Output Current, I_C . . . . . **125 mA**
Logic Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
P_D . . . . . **2.08 W***
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Junction Temperature, T_J . . . . . **+150°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*Derate at the rate of 16.7 mW/°C above T_A = +25°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5824A serial-input, latched sink driver is used in applications where a low output-saturation voltage, minimum parts count, and minimum logic supply current are desirable. The monolithic combination of CMOS logic and bipolar drivers provides an interface flexibility beyond the reach of standard buffers.

This device contains a high-speed 8-bit CMOS shift register, a CMOS data latch for each driver, and open-collector saturated (non-Darlington) drivers. The CMOS shift register and latches allow operation with most microprocessor/LSI-based systems. With a 5 V logic supply, BiMOS II devices will typically operate at a data input rate of better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. Use with TTL may require input pull-up resistors to ensure an input logic high. A CMOS serial data output allows cascading for interface applications requiring additional drive lines. Similar devices, with high-current, high-voltage Darlington outputs, are the UCN5821/22/23A.

The UCN5824A is supplied in a 16-pin plastic dual in-line package with a copper lead frame for improved package power dissipation. Continuous operation under worst-case conditions is permitted without derating.

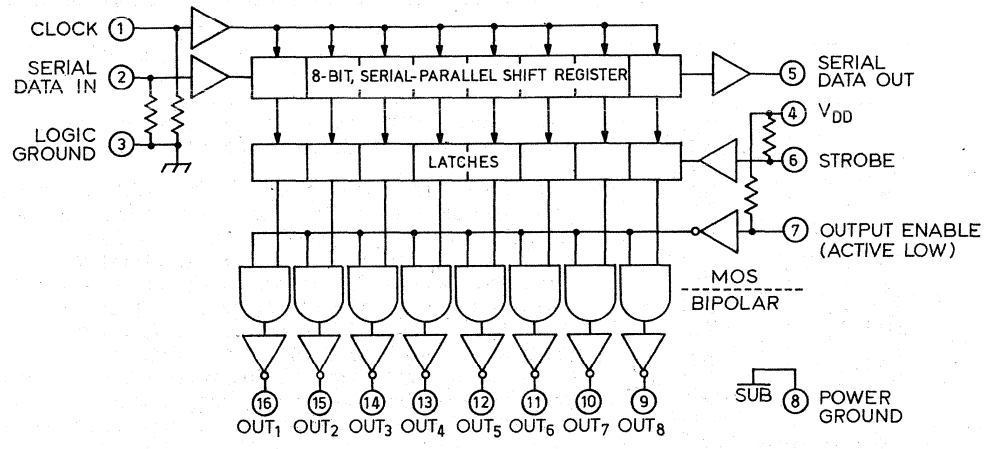
FEATURES

- Low Output Saturation Voltage
- 100 mA Continuous Output Current
- 50 V Minimum Output Breakdown
- 3.3 MHz Minimum Data Input Rate
- Low-Power CMOS Logic & Latches
- Output Enable and Strobe Functions

Always order by complete part number: **UCN5824A**.

5824
BiMOS II 8-BIT SERIAL-INPUT, LATCHED SATURATED SINK DRIVER

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-013

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 ... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 ... I_8	Output Enable	Output Contents I_1 I_2 ... I_8
H	⎍	H R_1 ... R_7	R_7				
L	⎍	L R_1 ... R_7	R_7				
X	⎏	R_1 R_2 ... R_8	R_8				
		X X ... X	X	L	R_1 R_2 ... R_8		
		P_1 P_2 ... P_8	P_8	H	P_1 P_2 ... P_8	L	P_1 P_2 ... P_8
					X X ... X	H	H H ... H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C	–	<1.0	50	µA
		V_{CE} = 50 V, T_A = +70°C	–	<1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	–	250	500	mV
Input Voltage	$V_{IN(1)}$	V_{DD} = 5 V	3.5	–	5.3	V
		V_{DD} = 12 V	10.5	–	12.3	V
	$V_{IN(0)}$		-0.3	–	0.8	V
Input Resistance	R_{IN}		100	800	–	kΩ
Supply Current	I_{DD}	All Outputs OFF, V_{DD} = 5.0 V, Note	–	–	100	µA
		All Outputs OFF, V_{DD} = 12 V, Note	–	–	200	µA
		One Output ON, V_{DD} = 5.0 V	–	4.5	6.0	mA
		One Output ON, V_{DD} = 12 V	–	13	18	mA
Maximum Clock Frequency	f_{clk}	V_{DD} = 5 V	3.3	5.0	–	MHz
		V_{DD} = 12 V	–	7.5	–	MHz
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA, V_{DD} = 5.0 V	4.5	4.7	–	V
		I_{OUT} = -200 µA, V_{DD} = 12 V	11.7	11.8	–	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA, V_{DD} = 5.0 V	–	200	250	mV
		I_{OUT} = 200 µA, V_{DD} = 12 V	–	100	200	mV
Output Enable to Output Delay (Resistive Load)	t_{PHL}	I_C = 100 mA	–	0.5	1.0	µs
	t_{PLH}	I_C = 100 mA	–	2.0	4.0	µs
Clock to Serial Data Out Delay	t_{PD}	C_L = 30 pF	–	–	300	ns

NOTE: $I_{DD(OFF)}$ is measured with $V_{STROBE} = V_{OE} = V_{DD}$, $V_{CLOCK} = V_{IN} = 0$ V.

Negative current is defined as coming out of (sourcing) the specified device terminal.

TIMING CONDITIONS

(T_A = +25°C, V_{DD} = 5 V, Logic Levels are V_{DD} and Ground)

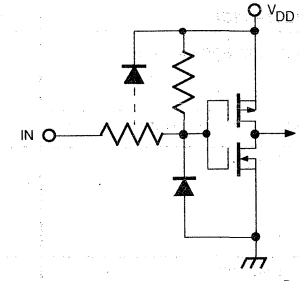
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	**75 ns**
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	**75 ns**
C.	Minimum Data Pulse Width	**150 ns**
D.	Minimum Clock Pulse Width	**150 ns**
E.	Minimum Time Between Clock Activation and Strobe	**300 ns**
F.	Minimum Strobe Pulse Width	**100 ns**
G.	Typical Time Between Strobe Activation and Output Transition	**1.0 µs**

Data present at the SERIAL DATA INPUT is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. The data must appear at the input prior to the rising edge of the clock input waveform. On succeeding clock pulses, the registers shift data information towards the SERIAL DATA OUTPUT.

Information present at any register is transferred to its respective latch when STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as STROBE is held high. In applications where the latches are bypassed (STROBE tied high), the outputs will follow the data stream (shift register data) unless the OUTPUT ENABLE is held high during serial data entry.

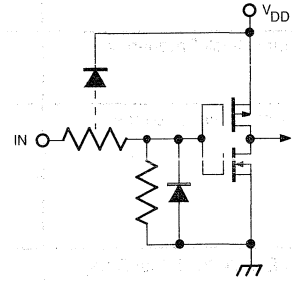
When OUTPUT ENABLE is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or being clocked through the shift register. With OUTPUT ENABLE low, the outputs are controlled by the state of the latches.

OUTPUT ENABLE & STROBE INPUT CIRCUITS



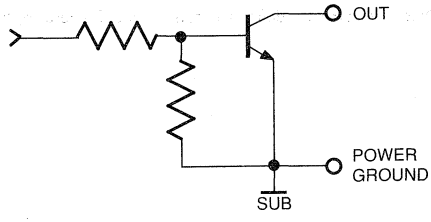
Dwg. EP-010-6

SERIAL DATA IN & CLOCK INPUT CIRCUITS



Dwg. EP-010-7

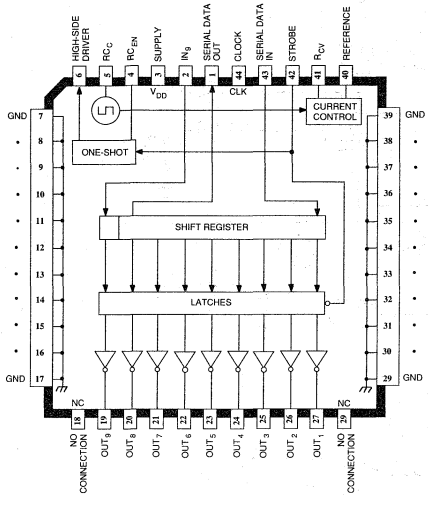
TYPICAL OUTPUT DRIVER



Dwg. EP-021-1

5829

9-BIT SERIAL-INPUT, LATCHED SINK DRIVER



Dwg. PP-028

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{OUT} . . . . . **50 V**
Output Current, I_{OUT}
(Continuous) . . . . . **1.6 A**
(Peak) . . . . . **1.8 A**
Logic Supply Voltage, V_{DD} . . . . . **7.0 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Junction Temperature, T_J . . . . . **+150°C***
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

* Fault conditions which produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Caution: This CMOS device has input static protection but is susceptible to damage when exposed to extremely high static electrical charges.

Intended primarily to drive high-current, dot matrix 9- and 24-wire printer solenoids, the UCN5829EB serial-input, latched sink driver provides a complete driver function with a minimum external parts count. Included on chip are constant-frequency PWM current control for each output driver, a user-defined output enable timeout, current sensing, and thermal shutdown.

The 9-bit CMOS shift register and latches allow operation with most microprocessor/LSI-based systems. With a 5 V logic supply, these BiMOS devices will operate at data input rates greater than 3.3 MHz. The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, NMOS, and TTL circuits. A CMOS serial data output allows cascade connections in applications requiring additional drive lines as required for 24-wire printheads.

The device features nine open-collector Darlington drivers, each rated at 50 V and 1.6 A. Current-control for each output is provided by an internal current-sensing resistor and a constant-frequency chopper circuit. An external high-side driver can be used to optimize print head performance. It is enabled by an on-chip driver during the output enable timeout. Internal logic sequencing prevents false output operation during power up. Other high-current devices for driving dot matrix printheads are the UDN2962W and UDN2974W.

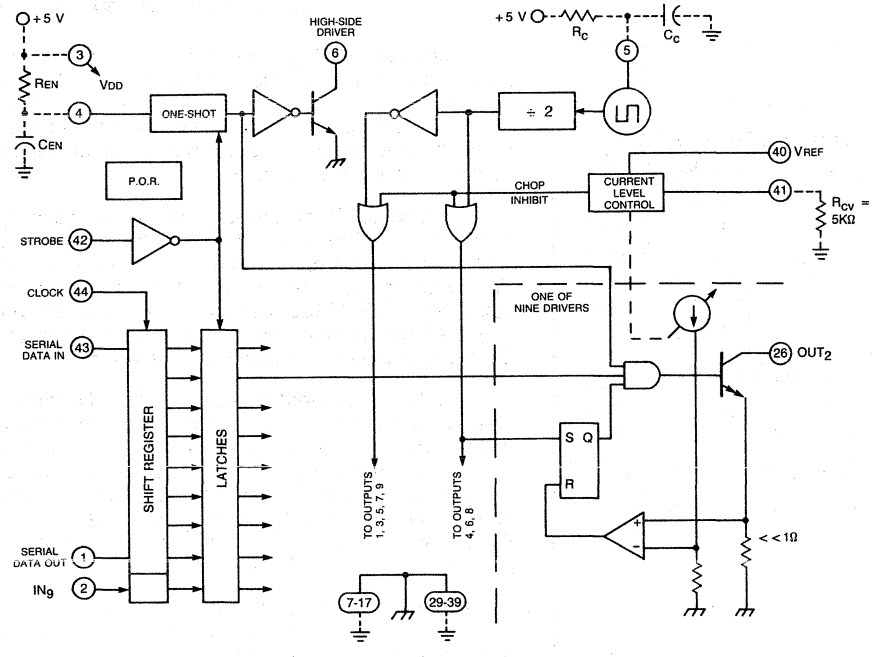
The UCN5829EB is supplied in a 44-lead power PLCC. Its batwing construction provides for maximum package power dissipation in a minimum-area, surface-mountable package.

FEATURES

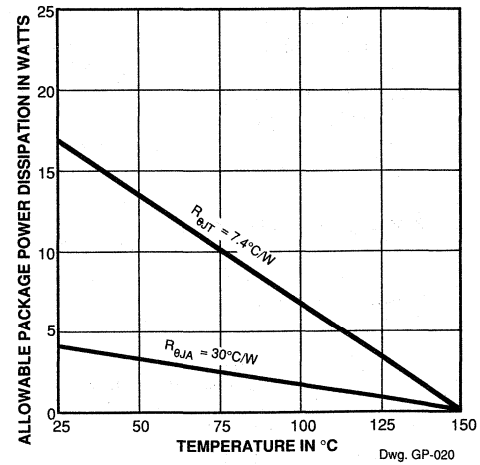
- 1.6 A Continuous Output Current
- 50 V Minimum Sustaining Voltage
- Internal Current Sensing
- Constant-Frequency PWM Current Control
- Control for External High-Side Driver
- 3.3 MHz Guaranteed Data Input Rate
- Low-Power CMOS Logic & Latches
- Internal Pull-Ups for TTL Compatibility
- User-Defined Output Enable Timeout
- Internal Thermal Shutdown Circuitry

Always order by complete part number: **UCN5829EB** .

FUNCTIONAL BLOCK DIAGRAM



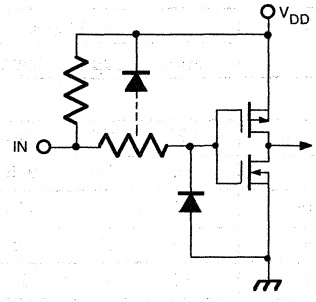
Dwg. FP-015



Dwg. GP-020

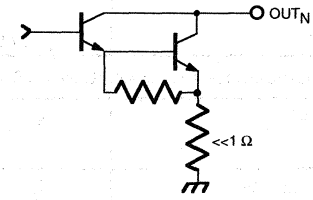
5829
9-BIT SERIAL-INPUT, LATCHED SINK DRIVER

TYPICAL INPUT CIRCUITS



Dwg. EP-010-3

TYPICAL OUTPUT DRIVER



Dwg. EP-021-2

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 4.75 to 5.25 V, in Test Circuit/Typical Application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Power Drivers (OUT_1 through OUT_9) with V_{REF} ≥4.5 V						
Output Leakage Current	I_{OUT}	V_{OUT} = 50 V	—	1.0	100	µA
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 1.0 A	—	1.0	1.5	V
		I_{OUT} = 1.6 A	—	1.5	1.9	V
Output Sustaining Voltage	$V_{OUT(sus)}$	I_{OUT} = 1.6 A, L = 3 mH	50	—	—	V
Control Logic						
HSD Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 20 mA	—	0.5	1.0	V
Logic Input Voltage	$V_{IN(1)}$		3.5	—	5.3	V
	$V_{IN(0)}$		-0.3	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 5.0 V	—	—	1.0	µA
		V_{IN} = 0.8 V	—	—	-180	µA
Reference Input Current	I_{REF}	V_{REF} = 3.0 V	—	500	900	µA
Logic Supply Current (V_{REF} = 2.0 V)	I_{DD}	All Drivers OFF	—	15	25	mA
		All Drivers ON, No Load	—	55	75	mA
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	MHz
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	mV
Clock to Serial Data Out Delay	t_{PD}	C_L = 30 pF	—	—	300	ns
Thermal Shutdown Temperature	T_j		—	165	—	°C

Continued next page...

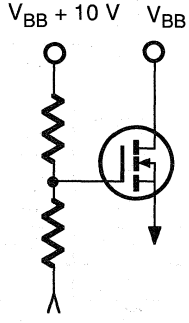
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 4.75 to 5.25 V, in Test Circuit/Typical Application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Chopping Characteristics (T_J = +25°C to +150°C) with Fast Clamp Diodes						
Enable Timeout	t_{EN}	R_{EN} = 20 kΩ, C_{EN} = 0.01 µF	190	200	210	µs
		R_{EN} = 30 kΩ, C_{EN} = 0.01 µF	285	300	315	µs
Chopping Frequency	f_{ch}	R_C = 20 kΩ, C_C = 250 pF	90	100	110	kHz
		R_C = 40 kΩ, C_C = 250 pF	45	50	55	kHz
Duty Cycle Range	dc	t_{on} / t_{on} + t_{off}	15	–	50	%
Chop Current Level	I_{TRIP}	V_{REF} = 2.0 V, f_{ch} < 100 kHz	0.9	1.0	1.1	A
		V_{REF} = 3.0 V, f_{ch} < 100 kHz	1.35	1.5	1.65	A
Output Current Control Range	V_{REF}		1.0	–	3.2	V
	I_{TRIP}		0.5	–	1.6	A
Delay	t_d	I_{TRIP} to $I_{OUT(P)}$, T_A = +25°C	–	300	500	ns
Chop Inhibit Voltage	V_{REF}		4.5	–	–	V

Negative current is defined as coming out of (sourcing) the specified device terminal.

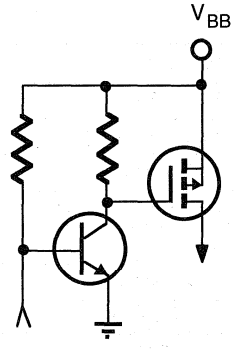
EXTERNAL HIGH-SIDE DRIVERS

NMOS



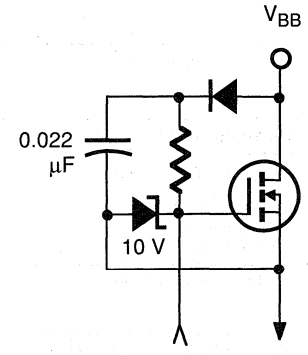
Dwg. EP-027

PMOS



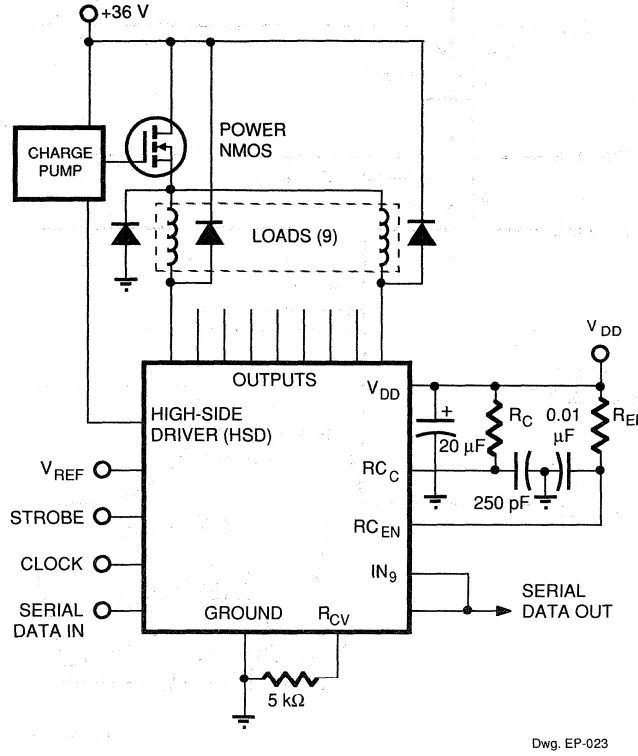
Dwg. EP-028

CHARGE-PUMP CIRCUITRY FOR SINGLE-SUPPLY OPERATION



Dwg. EP-026

TEST CIRCUIT AND TYPICAL APPLICATION

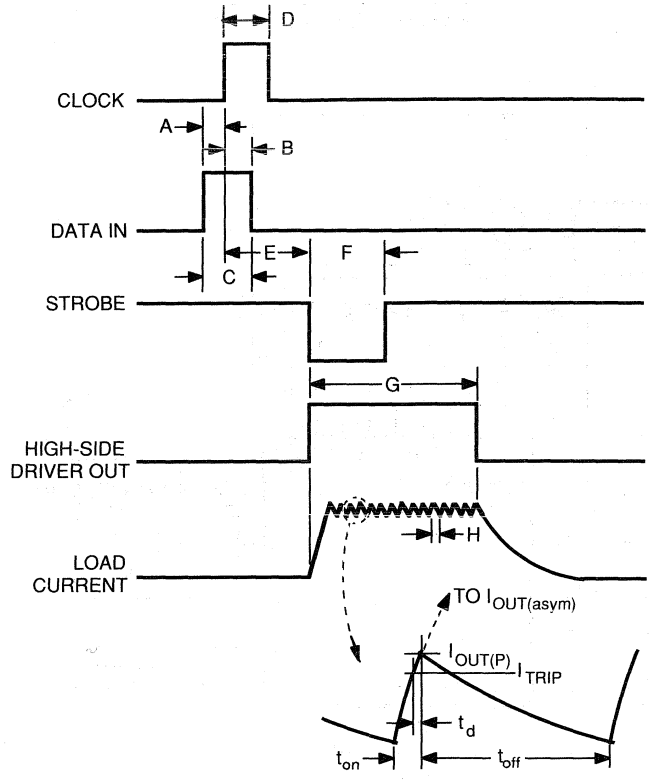


TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents* I_1 I_2 ... I_9	Serial Data Output	Strobe Input	Latch Contents* I_1 I_2 ... I_9	Output Contents* I_1 I_2 ... I_9
H	⌐	H R_1 ... R_8	R_7			
L	⌐	L R_1 ... R_8	R_7			
X	¬	R_1 R_2 ... R_9	R_8			
		X X ... X	X	H	R_1 R_2 ... R_9	
		P_1 P_2 ... P_9	P_8	L	P_1 P_2 ... P_9	P_1 P_2 ... P_9

* Serial Data Output connected to $Input_9$.

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State



Dwg. WP-011

TIMING CONDITIONS

T_A = +25°C, Logic Levels are V_{DD} and Ground

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**

C. Minimum Data Pulse Width . . . . . **250 ns**

D. Minimum Clock Pulse Width . . . . . **250 ns**

E. Minimum Time Between Clock Activation and Strobe . . . . . **500 ns**

F. Minimum Strobe Pulse Width . . . . . **500 ns**

G. Enable Timeout, t_{EN} . . . . . **R_{EN} C_{EN}**

H. Chop Period*, $t_{on} + t_{off}$ . . . . . **2 R_C C_C**

* Chopping is disabled if V_{REF} is greater than 4.5 V.

APPLICATIONS INFORMATION

The UCN5829EB is designed to drive high-current, 9- or 24-wire (3 devices cascaded) dot matrix impact printer solenoids. The internal CMOS control logic:

1) selects the operating channels from a 9- or 24-bit word previously loaded into the shift register,
2) controls the peak load current of the output drivers via nine constant-frequency switch-mode current choppers,
3) sets a user-defined print enable time, and
4) turns ON an external high-side driver during the print enable interval.

Data present at the SERIAL DATA INPUT is transferred to the shift register on the low-to-high transition of the CLOCK input pulse. The data must appear at the input prior to the rising edge of the clock input waveform. On succeeding clock pulses, the registers shift data information towards the SERIAL DATA OUTPUT. Information present at any register is transferred to its respective latch on the high-to-low transition of the STROBE (serial-to-parallel conversion). Drivers that have a logic high stored in their latch will be enabled for a set time interval (t_{EN}) generated by an internal one-shot. The output current is internally sensed and controlled in a fixed-frequency chopper format. Between strobe pulses, a new data word can be clocked in for the next print enable cycle.

PRINT ENABLE TIME

A high-to-low transition of the STROBE input starts an internal one-shot which sets the print enable time (t_{EN}) of the output drivers and the external high-side driver. The print enable time is determined by an external resistor (50 kΩ max) and capacitor (100 pF min) at RC_{EN} as

$$t_{EN} = R_{EN} C_{EN}$$

The print enable time can also be controlled from a microprocessor. In this mode, the internal one-shot is operated as an output disable function. In this mode, R_{EN} and C_{EN} are not used; instead a 10 kΩ series resistor is connected between RC_{EN} and an externally generated output disable pulse. As before, on the high-to-low STROBE transition, the outputs will be enabled. They will remain enabled until a low-to-high logic (≥3.3 V) DISABLE transition at RC_{EN}.

When operating in a continuous chopping mode, and neither print enable timeout nor output disable are desired, RC_{EN} should be grounded.

HIGH-SIDE DRIVER

To reduce the current decay time at the end of a print enable cycle, an external high-side driver can be used and controlled by the HIGH-SIDE DRIVER (HSD) output. The HSD is designed to drive an external N-channel MOSFET (with accompanying charge pump circuitry). During the print enable time (t_{EN}), the internal high-side driver is OFF, allowing the external high-side driver to be ON. If the external high-side driver is a P-channel device (eliminating the need for charge-pump circuitry), the HSD signal must be inverted for correct operation.

If an external high-side driver is used, an external ground clamp diode is also required.

OUTPUT CURRENT CONTROL

Each of the nine channels consists of a power Darlington sink driver, internal low-value current-sensing resistor, comparator, and an R/S flip-flop. The output current is sensed and controlled independently in each channel by means of a fixed-frequency chopper which sets the flip-flop and allows the output to turn ON. As the current increases in the load it is sensed by the internal sense resistor until the sense voltage equals the trip voltage of the comparator. At this time, the flip-flop is reset and the output is turned OFF. Over the range of V_{REF} = 1.0 V to 3.2 V, the output current trip point is a linear function of the reference voltage:

$$I_{TRIP} = V_{REF}/2$$

To ensure an accurate chop current level, an external 5 kΩ resistor (R_{CV}) is used. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays (typically 300 ns). After turn-off, the load current decays, circulating through the load and an external clamp diode. The output driver will stay OFF until the next chop pulse sets the flip-flop, turning ON the output, and allowing load current to rise again. The cycle repeats, maintaining the average printhead current at the desired level.

The chop pulse frequency is determined by an external resistor and capacitor at RC_C:

$$f_{ch} = \frac{1}{2\,R_C\,C_C}$$

To reduce the power supply and ground noise developed when operating nine channels synchronously, the outputs are split into two groups (OUTPUTS 2, 4, 6, 8 and OUTPUTS 1, 3, 5, 7, 9) for chopping pulses.

The chopping function is disabled when V_{REF} > 4.5 V. To prevent operation at higher than allowable current levels, V_{REF} should not exceed 3.2 V, except to disable the chopping function.

DUTY CYCLE LIMITS

For correct operation of the UCN5829EB, the duty cycle must be between 15% and 50%. The lower limit is due to internal lockout circuitry while the upper limit guarantees synchronous operation. The duty cycle (dc) can be calculated as

$$dc = \frac{t_{on}}{t_{on} + t_{off}} \approx \frac{I_{OUT(P)} / I_{OUT(asym)} + v_d / v_c}{1 + v_d / v_c}$$

where $I_{OUT(asym)}$ = the asymptotic current value = v_c/R_L

v_d = discharge voltage across the load = $V_{HSD} + V_{DIODE}$

v_c = charge voltage across the load = $V_{BB} - V_{OUT(SAT)} - V_{HSD}$

For most practical cases, correct operation can be achieved if $I_{OUT(asym)} / I_{OUT(P)} > 2.5$.

GENERAL

For applications with 9-wire printheads, SERIAL DATA OUT should be connected to IN_9. For 24-wire printhead applications, three devices (eight channels per device) are cascaded by connecting SERIAL DATA OUT to the next SERIAL DATA IN.

Each of the CMOS logic inputs have internal pull-up resistors for TTL compatibility.

An external transient-protection flyback diode is required at each output. Fast recovery diodes are recommended to reduce power dissipation in the UCN5829EB. Internal filtering prevents false triggering of the current sense comparator which can be caused by the recovery current spike of the diodes when the outputs turn ON.

The SUPPLY terminal should be well decoupled with a capacitor placed as close as possible to the device. Internal power-ON reset circuitry prevents false output triggering during power up.

Thermal protection circuitry is activated and turns OFF all drivers at a junction temperature of typically +165°C. The thermal shutdown is independent of all other functions. It should not be used as another control input but is intended only to protect the chip from catastrophic failures due to excessive junction temperatures. The output drivers are re-enabled when the junction temperature cools down to approximately +145°C.

TYPICAL APPLICATION

Shown is a typical application with the UCN5829EB controlling a chop current of 1 A through a 3 mH, 9 Ω load. To check the duty cycle and $I_{OUT(asym)}/I_{OUT(P)}$ restrictions

where $v_d = V_{HSD} + V_{DIODE} \approx 1.5 + 1.5 = 3$

$v_c = V_{BB} - V_{OUT(SAT)} - V_{HSD} = 36 - 1.5 - 1.5 = 33$

$I_{OUT(asym)} = v_c / R_L = 33 / 9 = 3.67$

then $I_{OUT(asym)} / I_{OUT(P)} = 3.67 / 1 = 3.67$

The condition of $I_{OUT(asym)} / I_{OUT(P)} > 2.5$ is met and the duty cycle will be within the proscribed limits. The actual duty cycle is

$$dc = \frac{I_{OUT(P)}/I_{OUT(asym)} + v_d/v_c}{1 + v_d/v_c} = \frac{1.0/3.67 + 2.5/33}{1 + 2.5/33} = 32\%$$

For a 50 kHz chopping frequency and a 250 μs print enable time, the remaining component values are

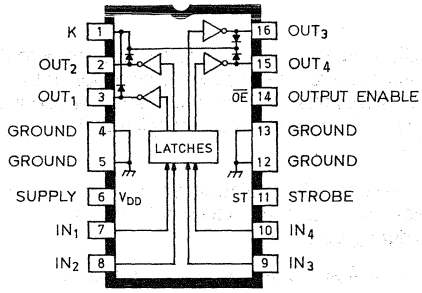
with $C_C = 250$ pF and $C_{EN} = 0.01$ μF

then $R_C = 1/(2 f_{ch} C_C) = 1/(2 \times 50 \times 10^3 \times 250 \times 10^{-12}) = 40$ kΩ

and $R_{EN} = t_{EN} / C_{EN} = 250 \times 10^{-6} / 10 \times 10^{-9} = 25$ kΩ

5830

BiMOS II 4-BIT LATCHED DRIVER



Dwg. PP-025-I

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Output Voltage, V_{CE} . . . . . **50 V**
Output Voltage, $V_{CE(sus)}$ . . . . . **45 V***
Output Current, I_{OUT} (peak) . . . . . **1.2 A**
(continuous) . . . . . **1.0 A**
Logic Supply Voltage, V_{DD} . . . . . **7.0 V**
CMOS Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*For inductive load applications: The sum of the load supply voltage and the clamping voltage.

Output current may be limited by duty cycle, number of drivers operating, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified maximum current rating or a junction temperature of 150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5830B latched driver is a high-current integrated circuit comprised of CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common STROBE and OUTPUT ENABLE functions. Although primarily designed for use with 2-phase unipolar stepper motors, this device can also be used to drive relays, solenoids, or incandescent lamps within its 1.2 A peak output current rating. The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility.

The CMOS inputs cause minimum loading and are compatible with most microprocessor/LSI-based systems. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure an input logic high. The latches will typically accept data at better than a 4.4 MHz rate.

The bipolar power outputs are open-collector 50 V Darlington drivers with a sustaining voltage of 45 V and integral clamp diodes for inductive load transient suppression. Under normal operating conditions, the four outputs can simultaneously sink load currents in excess of 500 mA continuously and without additional heat sinking. A similar device, featuring saturated (non-Darlington) outputs, is the UCN5831B.

The UCN5830B is furnished in a 16-pin plastic dual in-line batwing package with a copper lead frame and heat-sinkable tabs that maximize the device's power-handling capabilities.

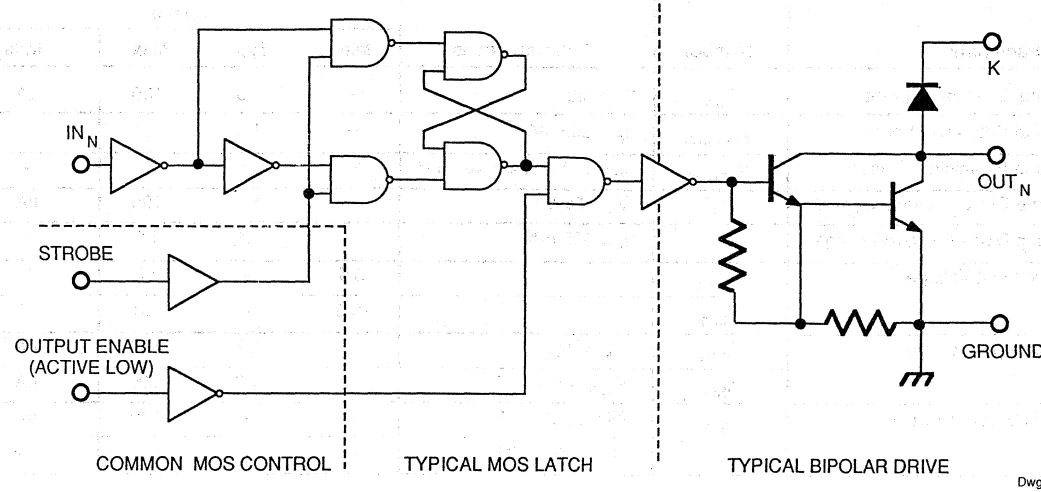
FEATURES

- 50 V Minimum Output Breakdown
- 45 V Minimum Sustaining Voltage
- 1.2 A Peak Output Current
- Reduced Supply Current Requirements
- Internal Transient Suppression
- Low-Power CMOS Latches
- Output Enable and Strobe Functions

Always order by complete part number: **UCN5830B** .

5830
BiMOS II 4-BIT LATCHED DRIVER

FUNCTIONAL BLOCK DIAGRAM

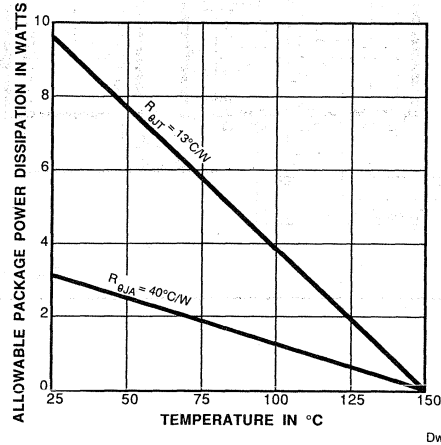


Dwg. FP-016

TRUTH TABLE

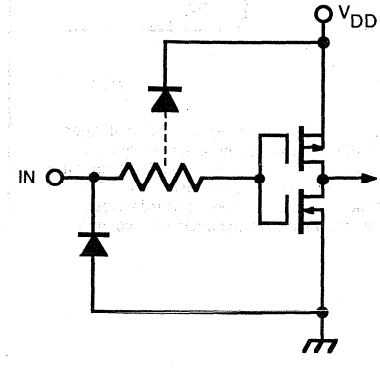
IN_N	STROBE	OUTPUT ENABLE	OUT_N
X	0	0	Prior State
0	1	0	Off
1	1	0	On
X	X	1	Off

X = Irrelevant



Dwg. GP-004-1

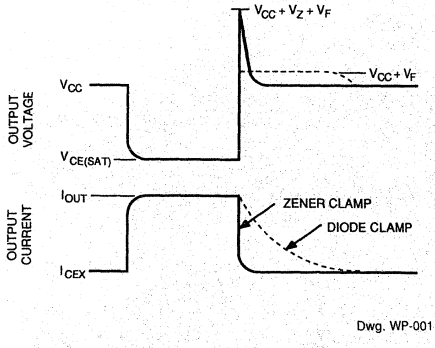
TYPICAL INPUT CIRCUIT



Dwg. EP-010-1

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{DD} = 5 V (unless otherwise noted).

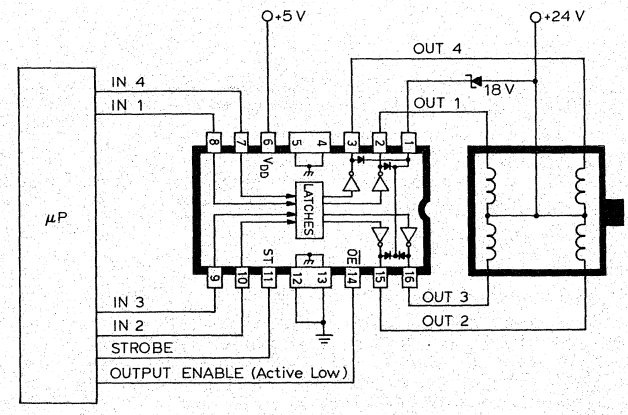
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_C = 50 V	–	1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 800 mA	–	1.0	1.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_C = 800 mA, L = 400 mH	45	–	–	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	–	1.0	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 800 mA	–	1.1	1.2	V
Logic Input Voltage	$V_{IN(1)}$		3.5	–	5.3	V
	$V_{IN(0)}$		-0.3	–	0.8	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	–	50	500	nA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	-50	-500	nA
Logic Supply Current	I_{DD}	All Outputs OFF	–	–	100	µA
		One Output ON	–	1.0	2.0	mA



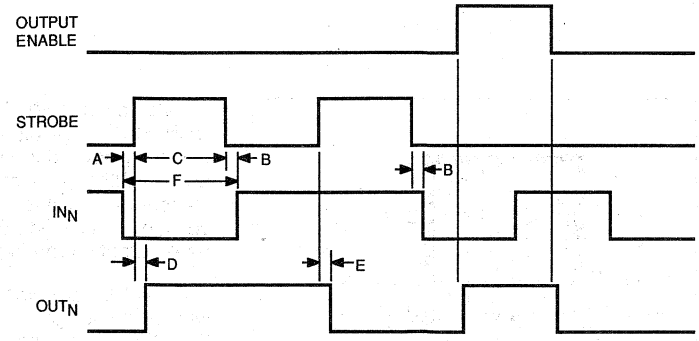
Dwg. WP-001

A typical application is shown driving a unipolar stepper-motor. A Zener diode is used to increase the flyback voltage. This gives a much faster inductive load turn-OFF current decay. The maximum Zener voltage plus the load supply voltage plus the internal diode forward voltage must not exceed the device's rated sustaining voltage.

TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



Dwg. EP-018-1



Dwg. WP-009-1

TIMING CONDITIONS

Logic Levels are V_{DD} and Ground

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**

B. Minimum Data Active Time After Strobe Enabled (Data Hold Time) . . . . . **50 ns**

C. Minimum Strobe Pulse Width . . . . . **125 ns**

D. Typical Time Between Strobe Activation and Output Turn-OFF Transition (Resistive Load) . . . . . **500 ns**

E. Typical Time Between Strobe Activation and Output Turn-ON Transition (Resistive Load) . . . . . **100 ns**

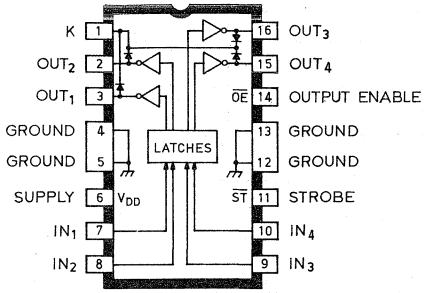
F. Minimum Data Pulse Width . . . . . **225 ns**

Data present at an input is transferred to its respective latch when STROBE is high. The latches will continue to accept new data as long as STROBE is held high. In applications where the latches are by-passed (STROBE tied high), the outputs will follow the data unless the OUTPUT ENABLE is high during data entry.

When OUTPUT ENABLE is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With OUTPUT ENABLE low, the outputs are controlled by the state of the latches.

5831

BiMOS II 4-BIT LATCHED DRIVER



Dwg. PP-025

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Output Voltage, V_{CE} . . . . . **50 V**
Output Voltage, $V_{CE(sus)}$ . . . . . **45 V***
Output Current, I_{OUT} (peak) . . . . . **1.2 A**
(continuous) . . . . . **1.0 A**
Logic Supply Voltage, V_{DD} . . . . . **7.0 V**
CMOS Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*For inductive load applications: The sum of the load supply voltage and the clamping voltage.

Output current may be limited by duty cycle, number of drivers operating, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified maximum current rating or a junction temperature of 150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Combining CMOS logic circuitry and bipolar power drivers, the UCN5831B is a 4-bit latched driver capable of providing an interface capability beyond the reach of standard logic buffers and power driver arrays. Although primarily designed for use with 2-phase unipolar stepper motors, this device can also be used to drive relays, low-voltage multiplexed LED displays, or incandescent lamps within its peak output current rating.

The CMOS inputs cause minimum loading and are compatible with most microprocessor/LSI-based systems. An active-low OUTPUT ENABLE can be used to disable all outputs without affecting the logic inputs or the state of the latches. Use with TTL may require input pull-up resistors to ensure an input logic high. BiMOS latches will typically operate at better than a 4.4 MHz rate.

The bipolar power outputs are open-collector 50 V saturated (non-Darlington) drivers. A sustaining voltage rating of 45 V, and internal clamp diodes, are provided for use with inductive loads. The four outputs can simultaneously sink load currents of almost 800 mA, continuously and without additional heat sinking, over the full operating temperature range. The outputs may be paralleled for increased load current capability. A similar device, featuring Darlington power driver outputs, is the UCN5830B.

The UCN5831B is supplied in a 16-pin plastic dual in-line batwing package with a copper lead frame that maximizes the device's power-handling capabilities.

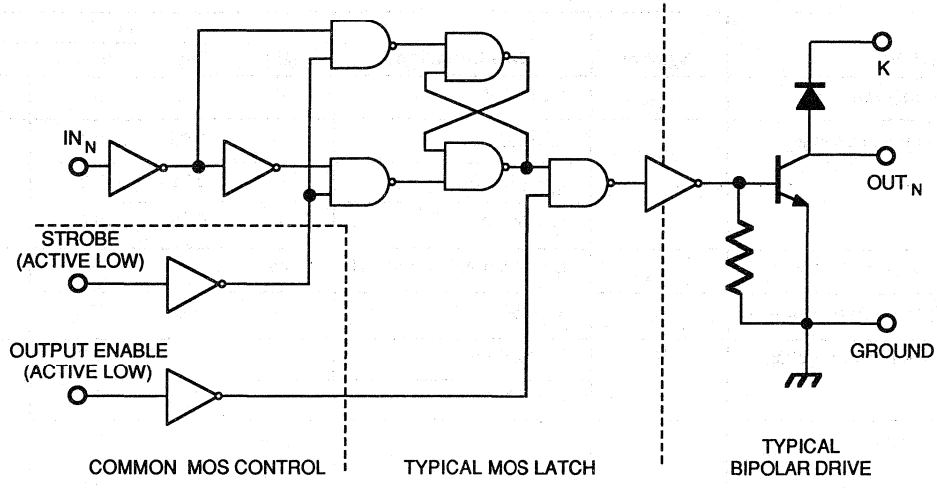
FEATURES

- Low Output Saturation Voltage
- 50 V Minimum Output Breakdown
- 45 V Minimum Sustaining Voltage
- 1.2 A Peak Output Current
- Internal High-Current Clamp Diodes
- Low-Power CMOS Latches
- Output Enable and Strobe Functions

Always order by complete part number: **UCN5831B** .

5831
BiMOS II 4-BIT LATCHED DRIVER

FUNCTIONAL BLOCK DIAGRAM

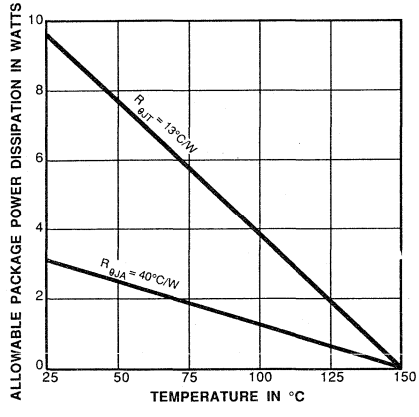


Dwg. FP-012

TRUTH TABLE

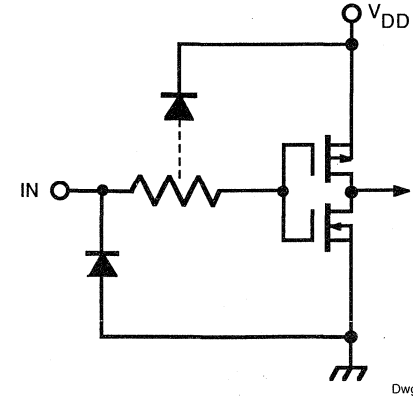
IN_N	STROBE	OUTPUT ENABLE	OUT_N
X	1	0	Prior State
0	0	0	Off
1	0	0	On
X	X	1	Off

X = irrelevant



Dwg. GP-004-1

TYPICAL INPUT CIRCUIT

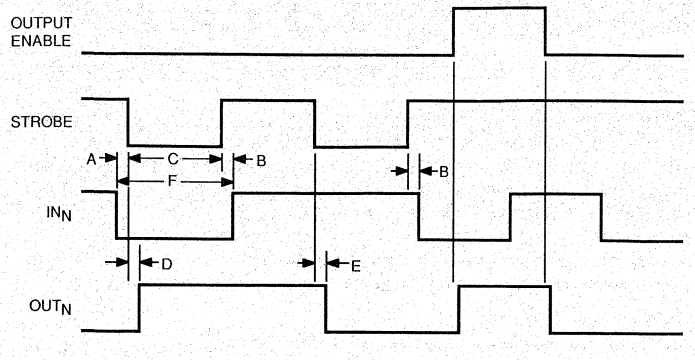


Dwg. EP-010-1

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_C = 50 V	–	1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 300 mA	–	0.25	0.4	V
		I_C = 625 mA	–	0.35	0.5	V
		I_C = 800 mA	–	0.45	0.6	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_C = 625 mA, L = 400 mH	45	–	–	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	–	1.0	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 625 mA	–	1.0	1.2	V
		I_F = 800 mA	–	1.1	1.3	V
Logic Input Voltage	$V_{IN(1)}$		3.5	–	5.3	V
	$V_{IN(0)}$		-0.3	–	0.8	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	–	50	500	nA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	-50	-500	nA
Logic Supply Current	I_{DD}	All Outputs OFF	–	–	100	µA
		One Output ON	–	24	30	mA

5831
BiMOS II 4-BIT LATCHED DRIVER



Dwg. WP-009

TIMING CONDITIONS
Logic Levels are V_{DD} and Ground

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**

B. Minimum Data Active Time After Strobe Enabled (Data Hold Time) . . . . . **50 ns**

C. Minimum Strobe Pulse Width . . . . . **125 ns**

D. Typical Time Between Strobe Activation and Output Turn-OFF Transition (Resistive Load) . . . . . **500 ns**

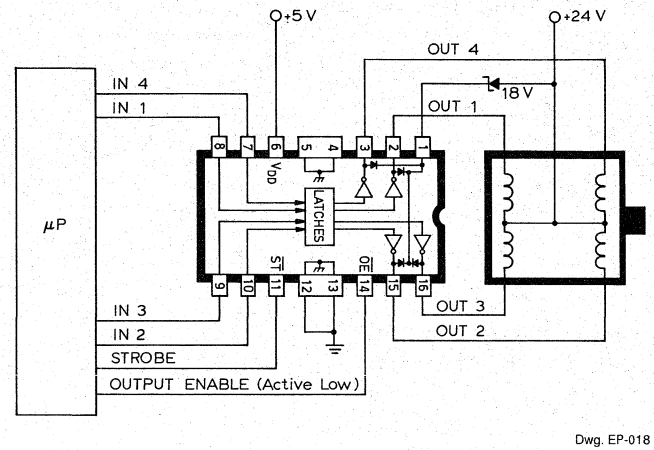
E. Typical Time Between Strobe Activation and Output Turn-ON Transition (Resistive Load) . . . . . **100 ns**

F. Minimum Data Pulse Width . . . . . **225 ns**

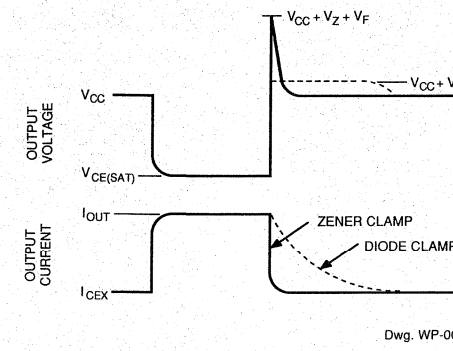
Data present at an input is transferred to its respective latch when STROBE is low. The latches will continue to accept new data as long as STROBE is held low. In applications where the latches are bypassed (STROBE tied low), the outputs will follow the data unless the OUTPUT ENABLE is high during data entry.

When OUTPUT ENABLE is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With OUTPUT ENABLE low, the outputs are controlled by the state of the latches.

TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



Dwg. EP-018



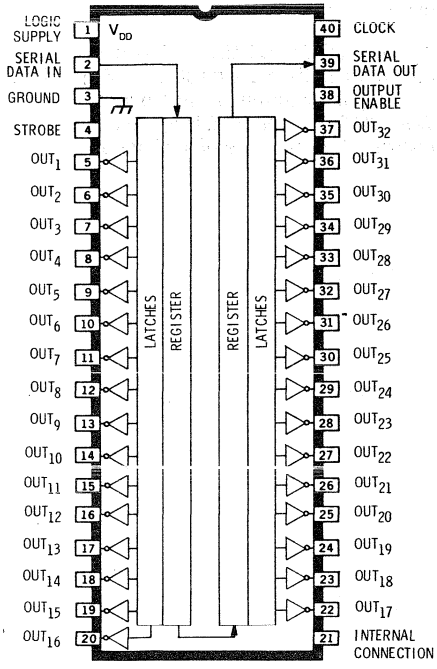
Dwg. WP-001

A typical application is shown driving a unipolar stepper-motor. A Zener diode is used to increase the flyback voltage. This gives a much faster inductive load turn-OFF current decay. The maximum Zener voltage plus the load supply voltage plus the internal diode forward voltage mus not exceed the device's rated sustaining voltage.

5832

BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5832A



Dwg. No. A-12,377A

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **40 V**
Logic Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **150 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Intended primarily to drive thermal printheads, Types UCN5832A and UCN5832EP have been optimized for low output-saturation voltage, high-speed operation, and pin configurations most convenient for the tight space requirements of high-resolution printheads. The integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 150 mA peak current. A combination of bipolar and MOS technologies gives BiMOS II arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high. MOS serial data outputs permit cascading for interface applications requiring additional drive lines.

The UCN5832A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Under normal operating conditions, this device will allow all outputs to sustain 100 mA continuously without derating. The UCN5832EP is supplied in a 44-lead plastic leaded chip carrier for minimum area, surface-mount applications.

Similar 32-bit serial-input latched source drivers are available as UCN5818AF/EPF. High-voltage, high-current 8-bit devices are available in Series UCN5820A and UCN5840A/EP/LW.

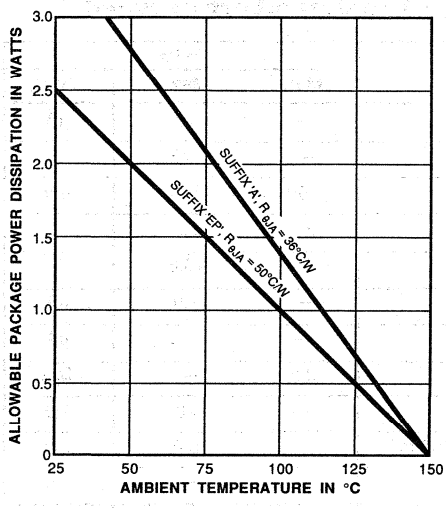
FEATURES

- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current Sink Outputs
- Low Saturation Voltage

Always order by complete part number:

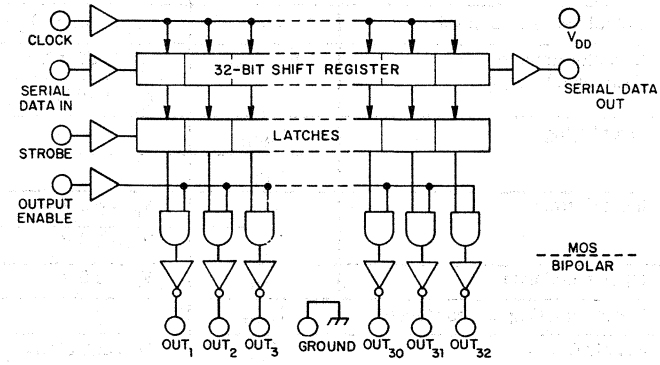
Part Number	Package
UCN5832A	40-Pin DIP
UCN5832EP	44-Lead PLCC

5832
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

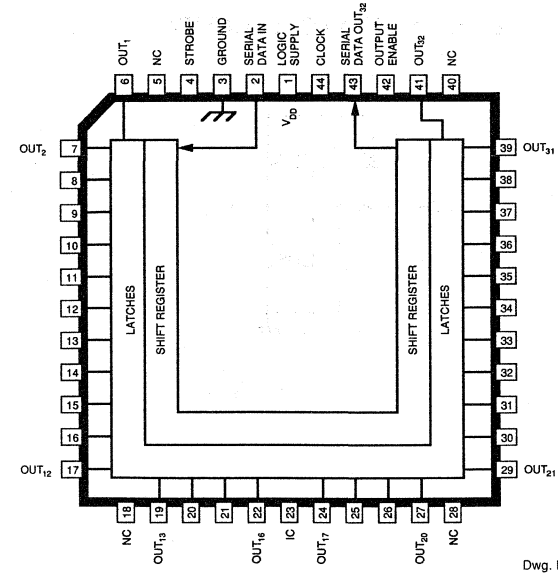


Dwg. GP-025

FUNCTIONAL BLOCK DIAGRAM



UCN5832EP



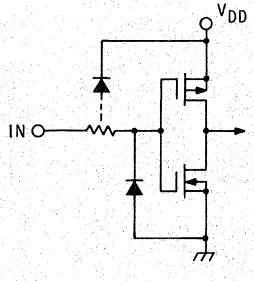
Dwg. No. A-14,36

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 40 V, T_A = 70°C	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	275	mV
		I_{OUT} = 100 mA	250	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 3.5 V	—	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-1.0	µA
Input Impedance	Z_{IN}	V_{IN} = 3.5 V	3.5	—	MΩ
Serial Data Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, I_{OUT} = 100 mA	—	5.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	1.0	µs
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	1.0	µs

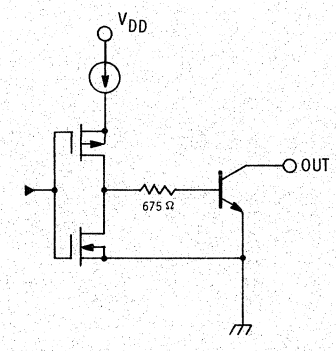
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL INPUT CIRCUIT

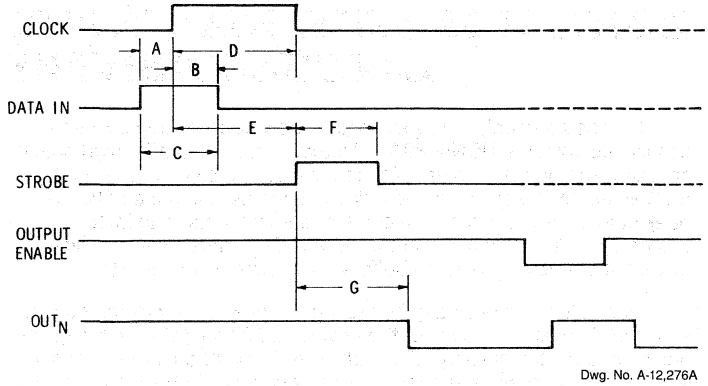


Dwg. No. A-12,379A

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,380A



Dwg. No. A-12,276A

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transition . . . . . **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TRUTH TABLE

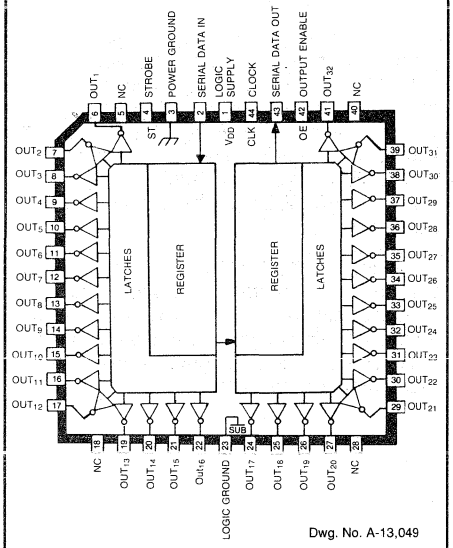
Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Output Enable Input	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	⊥	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⊥	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⊤	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	L	H H H ... H H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5833

BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5833EP



Dwg. No. A-13,049

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **30 V**
Logic Supply Voltage, V_{DD} . . . . . **7.0 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} (each output) . . . . . **125 mA**
Package Power Dissipation, P_D
(UCN5833A) . . . . . **3.5 W***
(UCN5833EP) . . . . . **2.5 W***
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

* Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily to reduce logic supply current, chip size and associated cost, the UCN5833A/EP integrated circuits offer high-speed operation for thermal printers. These devices can also be used to drive multiplexed LED displays or incandescent lamps within their 125 mA peak output current rating. The combination of bipolar and MOS technologies gives BiMOS II smart power ICs an interface flexibility beyond the reach of standard buffers and power driver circuits.

These 32-bit drivers have bipolar open-collector Darlington outputs, a CMOS data latch for each of the drivers, a 32-bit CMOS shift register, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems at data input rates above 3.3 MHz. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

The UCN5833A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. At an ambient temperature of +75°C, all outputs of the DIP-packaged device will sustain 50 mA continuously. For high-density applications, the UCN5833EP is available. This 44-lead plastic chip carrier (quad pack) is intended for surface-mounting on solder lands with 0.050" (1.27 mm) centers. CMOS serial data outputs permit cascading for applications requiring additional drive lines.

FEATURES

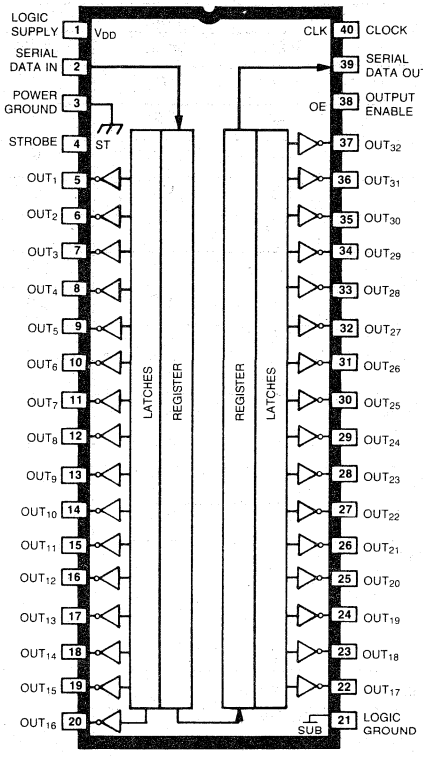
- 5 MHz Typical Data Input Rate
- 30 V Minimum Output Breakdown
- Darlington Current-Sink Outputs
- Low-Power CMOS Logic and Latches

Always order by complete part number:

Part Number	Package
UCN5833A	40-Pin DIP
UCN5833EP	44-Lead PLCC

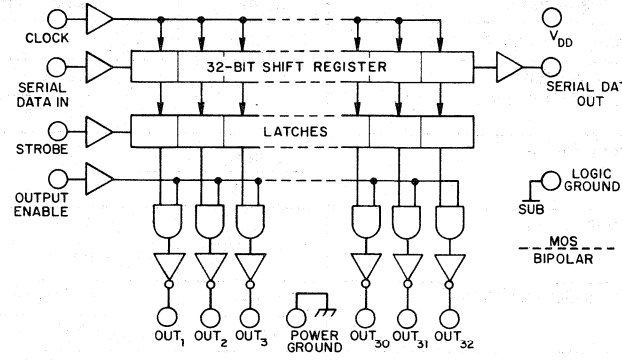
5833
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5833A



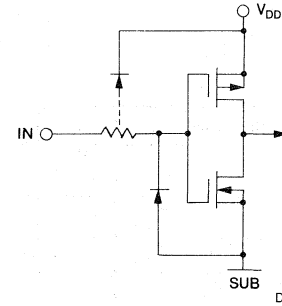
Dwg. No. A-13,048

FUNCTIONAL BLOCK DIAGRAM



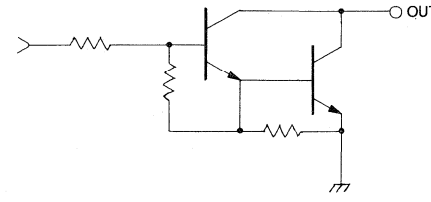
Dwg. No. A-13,057

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,050

TYPICAL OUTPUT DRIVER



Dwg. No. A-13,051

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

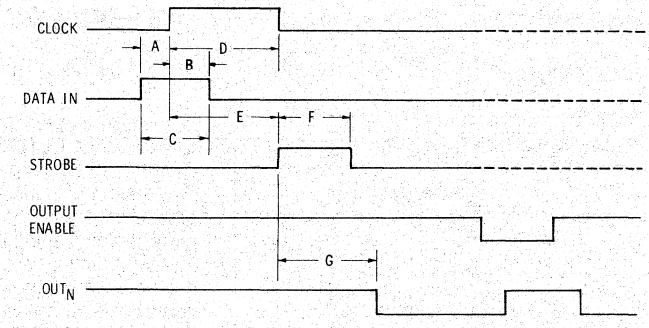
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 30 V, T_A = 70°C	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	1.2	V
		I_{OUT} = 100 mA	—	1.7	V
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	-1.0	µA
Serial Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	0.3	V
Supply Current	I_{DD}	One output ON, I_{OUT} = 100 mA	—	1.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	500	ns
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	500	ns

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable Input	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⊥⌜	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⊥⌜	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⌝⊥	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	L	H H H ... H H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State



Dwg. No. A-12,276A

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transition . . . . . **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

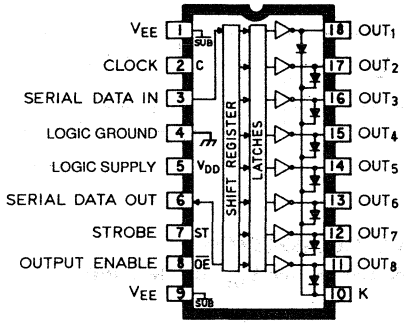
Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

SERIES 5840

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5841A – UCN5843A



Dwg. No. A-12,659

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{CE}
(UCN5841A/EP/LW) . . . . . **50 V**
(UCN5842A/EP/LW) . . . . . **80 V**
(UCN5843A/EP/LW) . . . . . **100 V**
Output Voltage, $V_{CE(sus)}$
(UCN5841A/EP/LW) . . . . . **35 V†**
(UCN5842A/EP/LW) . . . . . **50 V†**
(UCN5843A/EP/LW) . . . . . **50 V†**
Logic Supply Voltage Range,
V_{DD} . . . . . **4.5 V to 15 V**
V_{DD} with Reference to V_{EE} . . . . . **25 V**
Emitter Supply Voltage, V_{EE} . . . . . **-20 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **500 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

†For inductive load applications.

Note that the Series UCN5840A (dual in-line package) and Series UCN5840LW (small-outline IC package) are electrically identical and share a common pin number assignment.

Integrating low-power CMOS logic and bipolar output power drivers permit Series UCN5840A/EP/LW integrated circuits to be used in a wide variety of peripheral power driver applications. The three basic devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers. The 500 mA outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids, and other inductive loads. Except for the maximum driver output voltage ratings, the UCN5841A/EP/LW, UCN5842A/EP/LW, and UCN5843A/EP/LW are identical. The UCN5843A/EP/LW offers premium performance with a minimum output-breakdown voltage rating of 100 V (50 V sustaining). All drivers can be operated with a split supply where the negative supply is up to -20 V.

BiMOS II devices have higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, drivers can be cascaded for interface applications requiring additional drive lines.

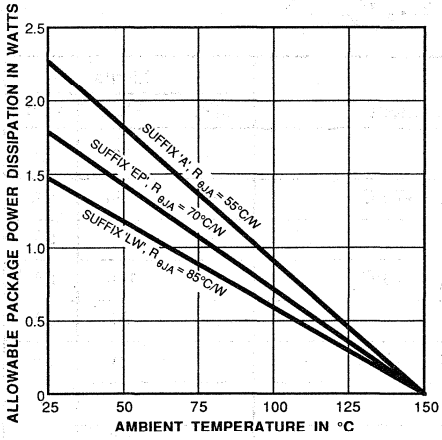
Suffix 'A' devices are furnished in a standard 18-pin plastic DIP; suffix 'EP' indicates a 20-lead PLCC; suffix 'LW' indicates an 18-lead wide-body SOIC.

FEATURES

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches,
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- DIP, PLCC, or SOIC Packaging

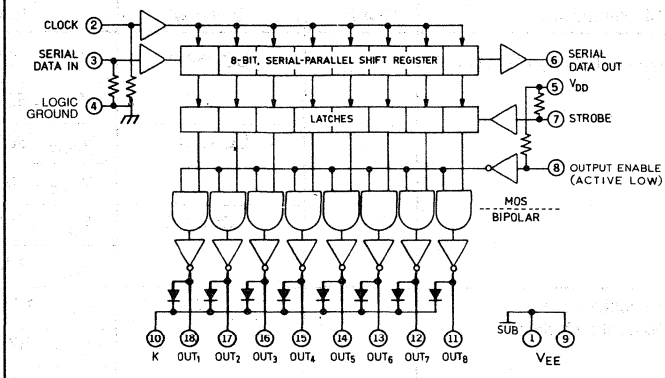
Always order by complete part number, e.g., **UCN5842LW**.

SERIES 5840
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. GP-024

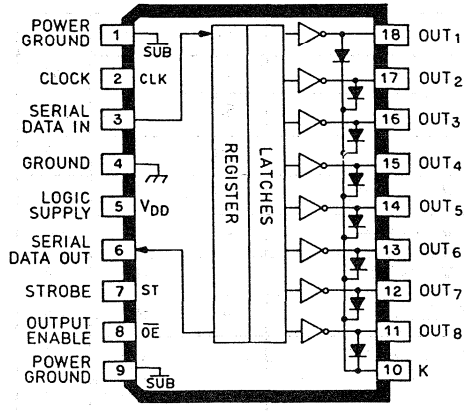
FUNCTIONAL BLOCK DIAGRAM
('A' & 'LW' Package Shown)



Dwg. No. A-12,661A

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

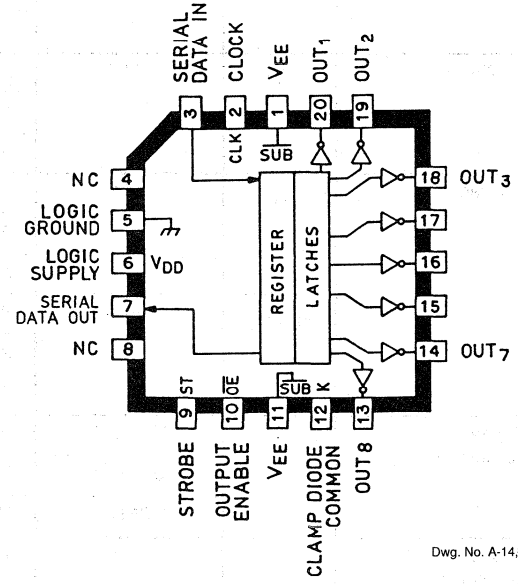
UCN5841LW – UCN5843LW



Dwg. No. A-14,438

Note that the Series UCN5840A (dual in-line package) and Series UCN5840LW (small-outline IC package) are electrically identical and share a common pin number assignment.

UCN5841EP – UCN5843EP



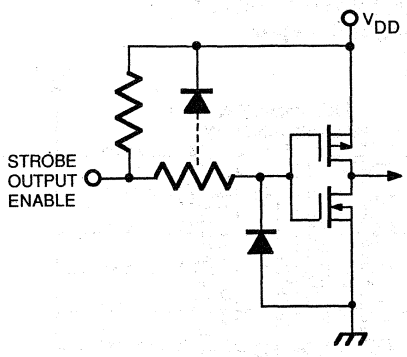
Dwg. No. A-14,362

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, V_{EE} = 0 V (unless otherwise specified).

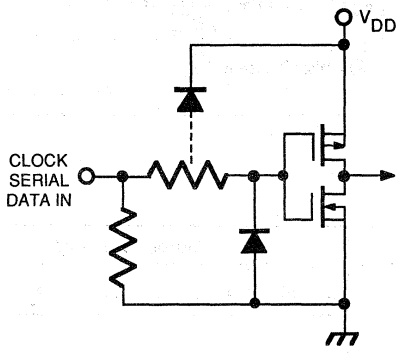
Characteristic	Symbol	Applicable Devices*	Test Conditions	Limits Min.	Limits Max.	Limits Unit
Output Leakage Current	I_{CEX}	UCN5841	V_{OUT} = 50 V	—	50	µA
			V_{OUT} = 50 V, T_A = +70°C	—	100	µA
		UCN5842	V_{OUT} = 80 V	—	50	µA
			V_{OUT} = 80 V, T_A = +70°C	—	100	µA
		UCN5843	V_{OUT} = 100 V	—	50	µA
			V_{OUT} = 100 V, T_A = +70°C	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	I_{OUT} = 100 mA	—	1.1	V
			I_{OUT} = 200 mA	—	1.3	V
			I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Collector-Emitter Sustaining Voltage	$V_{CE(sus)}$	UCN5841	I_{OUT} = 350 mA, L = 2 mH	35	—	V
		UCN5842	I_{OUT} = 350 mA, L = 2 mH	50	—	V
		UCN5843	I_{OUT} = 350 mA, L = 2 mH	50	—	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	V_{DD} = 12 V	10.5	—	V
			V_{DD} = 10 V	8.5	—	V
			V_{DD} = 5.0 V	3.5	—	V
Input Resistance	R_{IN}	ALL	V_{DD} = 12 V	50	—	kΩ
			V_{DD} = 10 V	50	—	kΩ
			V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	All Drivers ON, V_{DD} = 12 V	—	16	mA
			All Drivers ON, V_{DD} = 10 V	—	14	mA
			All Drivers ON, V_{DD} = 5.0 V	—	8.0	mA
	$I_{DD(OFF)}$	ALL	All Drivers OFF, V_{DD} = 12 V	—	2.9	mA
			All Drivers OFF, V_{DD} = 10 V	—	2.5	mA
			All Drivers OFF, V_{DD} = 5.0 V	—	1.6	mA
Clamp Diode Leakage Current	I_R	UCN5841	V_R = 50 V	—	50	µA
		UCN5842	V_R = 80 V	—	50	µA
		UCN5843	V_R = 100 V	—	50	µA
Clamp Diode Forward Voltage	V_F	ALL	I_F = 350 mA	—	2.0	V

* Complete part number includes a suffix to identify package style: A = DIP, EP = PLCC, LW = SOIC.

TYPICAL INPUT CIRCUITS

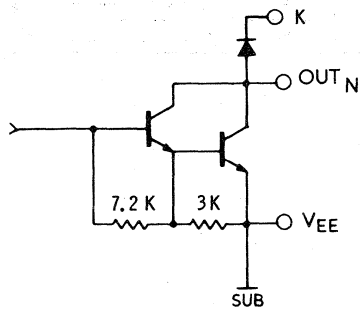


Dwg. No. EP-010-3

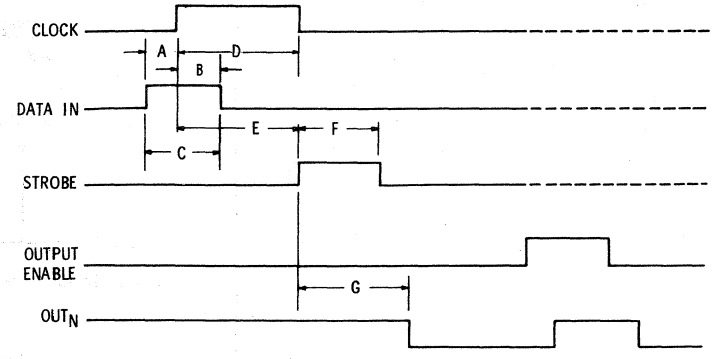


Dwg. No. EP-010-4

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,660



Dwg. No. A-12,627

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

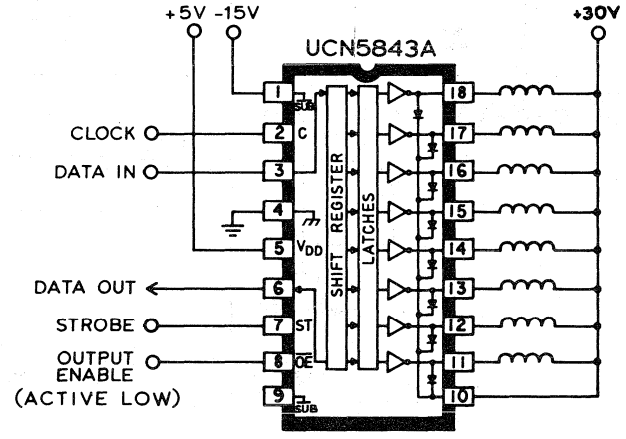
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	**75 ns**
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	**75 ns**
C.	Minimum Data Pulse Width	**150 ns**
D.	Minimum Clock Pulse Width	**150 ns**
E.	Minimum Time Between Clock Activation and Strobe	**300 ns**
F.	Minimum Strobe Pulse Width	**100 ns**
G.	Typical Time Between Strobe Activation and Output Transition	**500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

TYPICAL APPLICATION
RELAY/SOLENOID DRIVER
Using Split Supply



Dwg. No. A-12,547

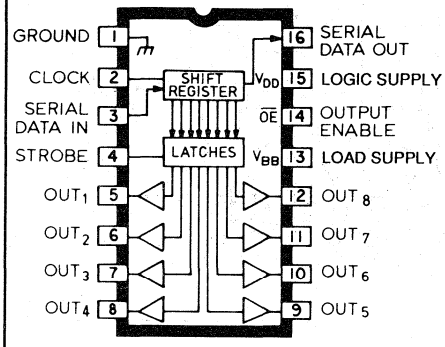
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ..... I_8			I_1 I_2 I_3 ..... I_8		I_1 I_2 I_3 ..... I_8
H	⎍	H R_1 R_2 ..... R_7	R_7				
L	⎍	L R_1 R_2 ..... R_7	R_7				
X	⎏	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5890 AND 5891

BiMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg. No. 12,639

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{OUT}
(UCN5890A) . . . . . **80 V**
(UCN5891A) . . . . . **50 V**
Logic Supply Voltage Range,
V_{DD} . . . . . **4.5 V to 15 V**
Driver Supply Voltage Range, V_{BB}
(UCN5890A) . . . . . **20 V to 80 V**
(UCN5891A) . . . . . **5.0 V to 50 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **-500 mA**
Allowable Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

Primarily designed for use with thermal or electromagnetic printers, the UCN5890A and UCN5891A BiMOS II serial-input, latched drivers combine an 8-bit CMOS shift register, associated latches, and control circuitry (strobe and output enable) with Darlington sourcing outputs. They may also be used with relays or multiplexed LED displays within their output current limitation of -500 mA per driver.

Except for output voltage ratings, the devices are identical. The UCN5890A is rated for operation with load supply voltages of 20 V to 80 V and a minimum output sustaining voltage of 50 V. The UCN5891A is optimized for operation with supply voltages of 5 V to 50 V (35 V sustaining).

BiMOS II devices have higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output, allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

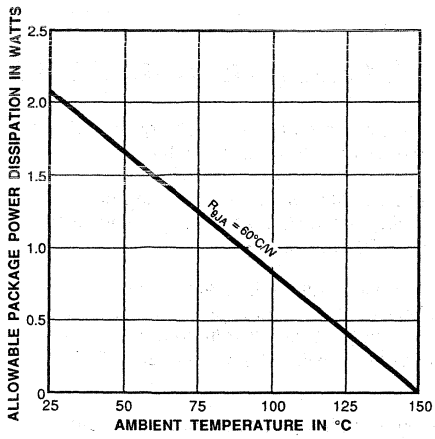
All devices are supplied in a standard dual in-line plastic package with copper lead frame for enhanced package power dissipation characteristics. A similar driver, featuring reduced output saturation voltage, is the UCN5895A. Complementary, 8-bit serial-input, latched sink drivers are the Series UCN5820A.

FEATURES

- 50 V or 80 V Source Outputs
- Output Current to -500 mA
- Output Transient-Suppression Diodes
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic and Latches

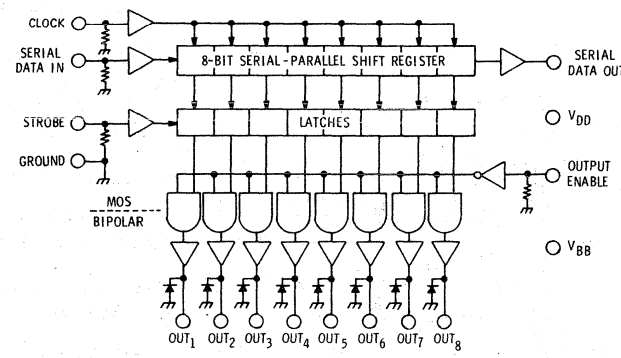
Always order by complete part number:

Part Number	Max. V_{OUT}
UCN5890A	80 V
UCN5891A	50 V



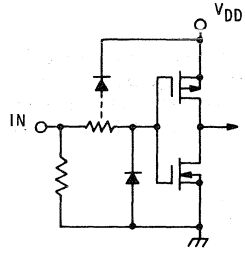
Dwg. GP-016

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,654

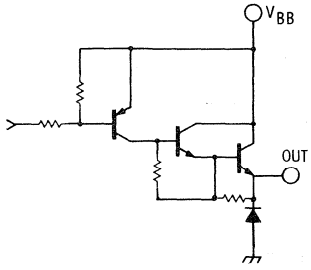
TYPICAL INPUT CIRCUIT



Dwg. No. A-12,520

Number of Outputs ON at I_{OUT} = -200 mA	Max. Allowable Duty Cycle at T_A of		
	50°C	60°C	70°C
8	53%	47%	41%
7	60%	54%	48%
6	70%	64%	56%
5	83%	75%	67%
4	100%	94%	84%
3	100%	100%	100%
2	100%	100%	100%
1	100%	100%	100%

TYPICAL OUTPUT DRIVER

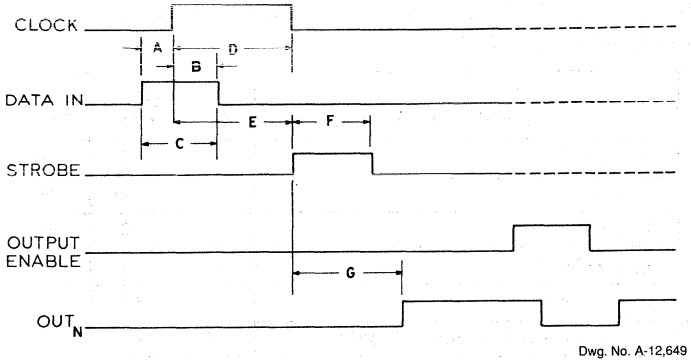


Dwg. No. A-12,648

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 80 V (UCN5890A) or 50 V (UCN5891A), V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	V_{BB}	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	Max.	T_A = +25°C	—	-50	µA
			T_A = +70°C	—	-100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	50 V	I_{OUT} = -100 mA	—	1.8	V
			I_{OUT} = -225 mA	—	1.9	V
			I_{OUT} = -350 mA	—	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	Max.	I_{OUT} = -350 mA, L = 2 mH, UCN5891A	35	—	V
			I_{OUT} = -350 mA, L = 2 mH, UCN5890A	50	—	V
Input Voltage	$V_{IN(1)}$	50 V	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	50 V	V_{DD} = 5 V to 12 V	-0.3	+0.8	V
Input Current	$I_{IN(1)}$	50 V	V_{DD} = V_{IN} = 5.0 V	—	50	µA
			V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	50 V	V_{DD} = 5.0 V	100	—	kΩ
			V_{DD} = 12 V	50	—	kΩ
Clock Frequency	f_c	50 V		3.3	—	MHz
Serial Data Output Resistance	R_{OUT}	50 V	V_{DD} = 5.0 V	—	20	kΩ
			V_{DD} = 12 V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	50 V	Output Enable to Output, I_{OUT} = -350 mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	50 V	Output Enable to Output, I_{OUT} = -350 mA	—	10	µs
Supply Current	I_{BB}	50 V	All outputs ON, All outputs open	—	10	mA
			All outputs OFF	—	200	µA
	I_{DD}	50 V	V_{DD} = 5 V, All outputs OFF, Inputs = 0 V	—	100	µA
			V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
			V_{DD} = 5 V, One output ON, All Inputs = 0 V	—	1.0	mA
			V_{DD} = 12 V, One output ON, All Inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	Max.	T_A = +25°C	—	50	µA
			T_A = +70°C	—	100	µA
Diode Forward Voltage	V_F	Open	I_F = 350 mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



Dwg. No. A-12,649

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
C. Minimum Data Pulse Width ..... **150 ns**
D. Minimum Clock Pulse Width ..... **150 ns**
E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
F. Minimum Strobe Pulse Width ..... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition ..... **1.0 µs**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

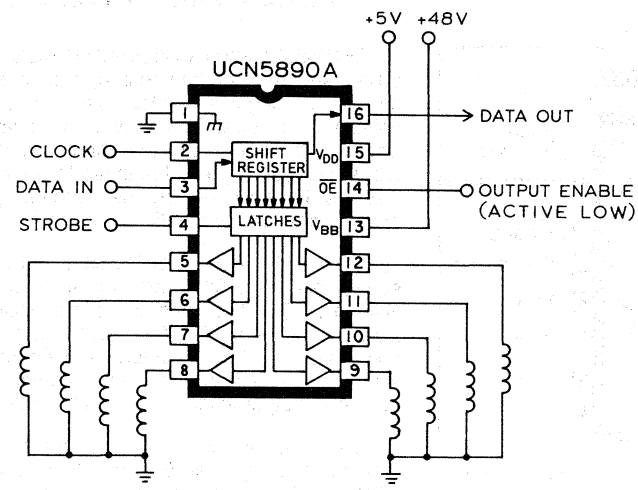
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Output Enable	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	⊓	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⊓	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⊔	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

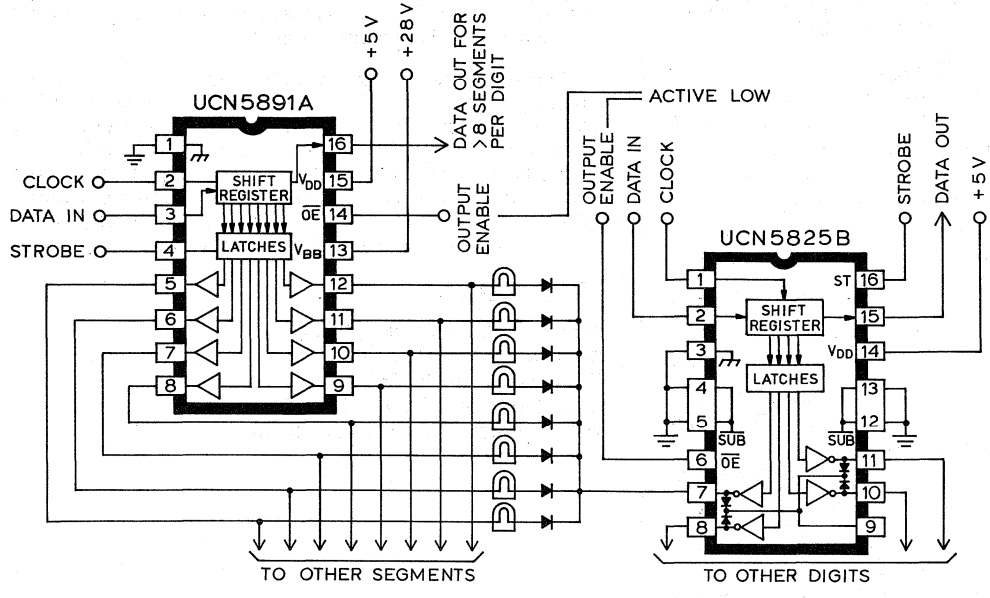
TYPICAL APPLICATIONS

SOLENOID OR RELAY DRIVER



Dwg. No. A- 12,548

MULTIPLEXED INCANDESCENT LAMP DRIVER

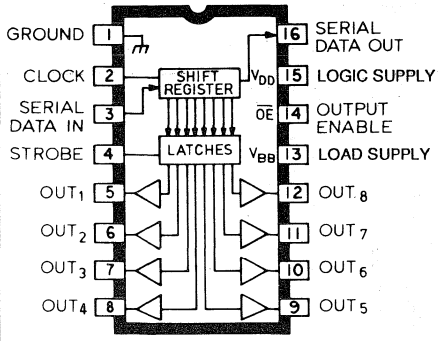


Dwg. EP-024

5895

BiMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

UCN5895A



Dwg. No. A-12,639

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{OUT}
(UCN5895A/EP) . . . . . **50 V**
(UCN5895A-2) . . . . . **25 V**
Logic Supply Voltage Range,
V_{DD} . . . . . **4.5 V to 12 V**
Driver Supply Voltage Range, V_{BB}
(UCN5895A/EP) . . . . . **5.0 V to 50 V**
(UCN5895A-2) . . . . . **5.0 V to 25 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **-250 mA**
Allowable Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

UCN5895A and UCN5895EP BiMOS II serial-input, latched source drivers are designed for use in applications requiring low output-saturation voltages and currents to -250 mA per driver. Each driver combines an 8-bit CMOS register, associated latches and control circuitry (strobe and output enable), with saturated bipolar emitter-follower outputs. Typical loads are low-voltage LEDs and incandescent displays. They can also be used with multiplexed LED displays, thermal printers, or electromagnetic printers within their output limitations.

The UCN5895A and UCN5895EP are rated for operation with supply voltages to 50 V and feature a minimum output sustaining voltage of 35 V. The more economical UCN5895A-2 is for use with supply voltages to 25 V (15 V sustaining). Under normal operating conditions, at +25°C, all outputs will source -120 mA continuously without derating. Similar drivers, featuring Darlington outputs for increased output ratings, are the UCN5890A and UCN5891A.

BiMOS II devices can operate at greatly improved data-input rates. With a 5 V supply, they will typically operate at better than 5 MHz. At 12 V, significantly higher speeds are obtained.

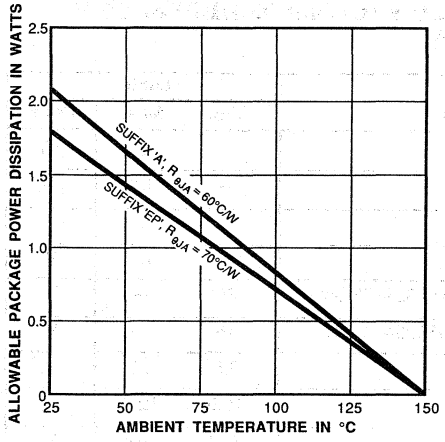
The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

These devices are rated for continuous operation over the temperature range of -20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle. The UCN5895A and UCN5895A-2 are supplied in standard 16-pin dual in-line plastic packages with copper lead frames for increased allowable package power dissipation. The UCN5895EP is supplied in a 20-lead plastic leaded chip carrier for minimum area, surface-mount applications.

FEATURES

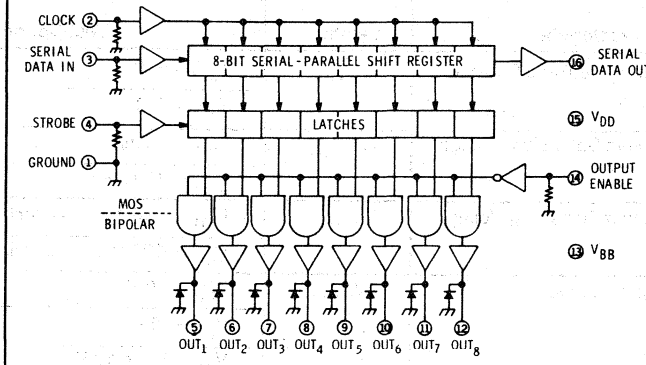
- Low Output-Saturation Voltage
- Source Outputs to 50 V
- Output Current to -250 mA
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic & Latches

Always order by complete part number, e.g., **UCN5895A-2** .



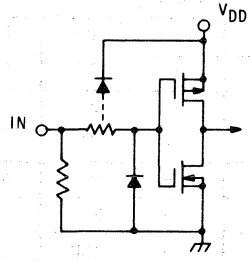
Dwg. GP-026

FUNCTIONAL BLOCK DIAGRAM
('A' Package Pin Numbers Shown)



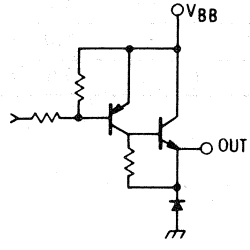
Dwg. No. A-12,654

TYPICAL INPUT CIRCUIT



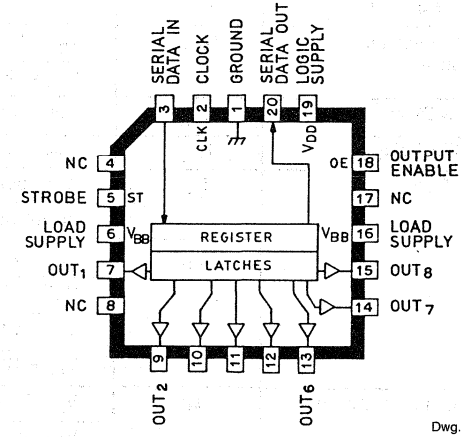
Dwg. No. A-12,520

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,655

UCN5895EP

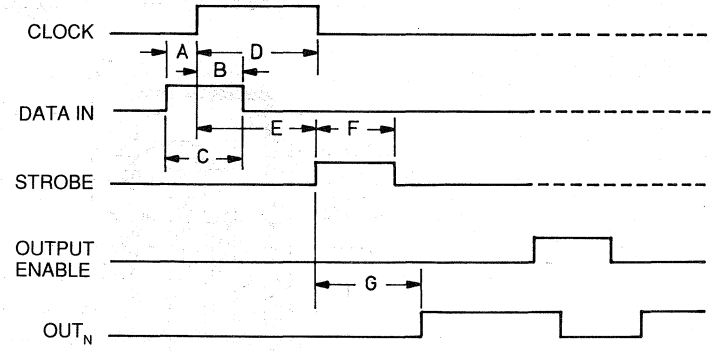


Dwg. No. A-14,368

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V (UCN5895A/EP) or 25 V (UCN5895A-2), V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	T_A = +25°C	—	-50	µA
		T_A = +70°C	—	-100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = -60 mA	—	1.1	V
		I_{OUT} = -120 mA	—	1.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = -120 mA, L = 2 mH, UCN5895A/EP only	35	—	V
		I_{OUT} = -120 mA, L = 2 mH, UCN5895A-2 only	15	—	V
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	V_{DD} = 5 V to 12 V	-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	50	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	100	—	kΩ
		V_{DD} = 12 V	50	—	kΩ
Clock Frequency	f_{CLK}		3.3	—	MHz
Serial Data-Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	Output Enable to Output, I_{OUT} = -120 mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	Output Enable to Output, I_{OUT} = -120 mA	—	10	µs
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10	mA
		All outputs OFF	—	200	µA
	I_{DD}	V_{DD} = 5 V, All outputs OFF, Inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
		V_{DD} = 5 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	V_R = 25 V, T_A = +25°C	—	50	µA
		V_R = 25 V, T_A = +70°C	—	100	µA
Diode Forward Voltage	V_F	I_F = 120 mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



Dwg. No. A-12,649A

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transition . . . . . **1.0 µs**

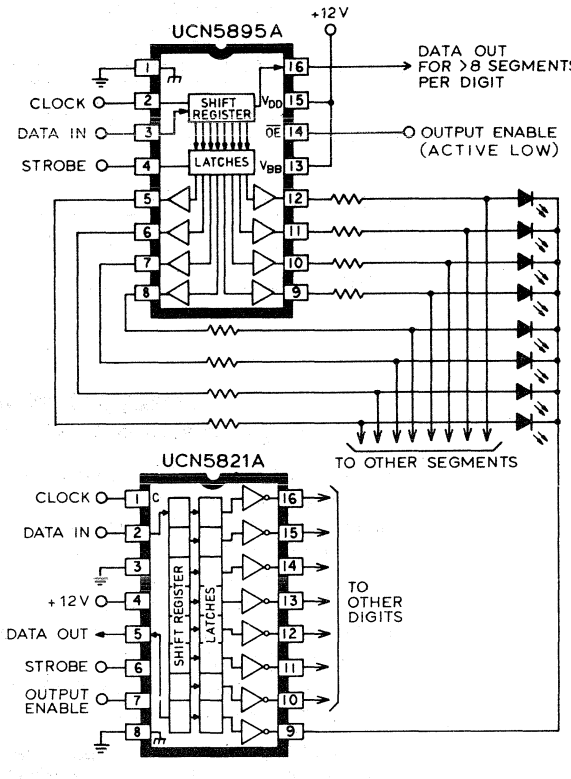
Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

5895
BiMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

TYPICAL APPLICATION



Dwg. No. B-1541

TRUTH TABLE

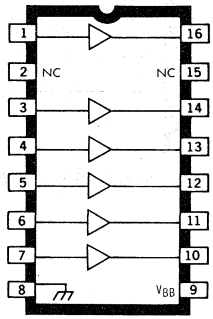
Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

6116 AND 6118

FLUORESCENT DISPLAY DRIVERS

UDN6116A/R



Dwg. No. A-9643A

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Supply Voltage, V_{BB}
(suffix A, LW, or R) . . . . . **85 V**
(suffix A-1) . . . . . **115 V**
(suffix A-2 or R-2) . . . . . **65 V**
Input Voltage, V_{IN} . . . . . **20 V**
Output Current, I_{OUT} . . . . . **-40 mA**
Allowable Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: The high input impedance of these devices makes them susceptible to static discharge damage associated with handling and testing. Techniques similar to those used for handling MOS devices should be employed.

Consisting of six or eight NPN Darlington output stages and the associated common-emitter input stages, these drivers are designed to interface between low-level digital logic and vacuum fluorescent displays. All devices are capable of driving the digits and/or segments of these displays and are designed to permit all outputs to be activated simultaneously. Pull-down resistors are incorporated into each output and no external components are required for most fluorescent display applications. The highest voltage parts (suffix A-1) are also used in gas-discharge display applications as anode (digit) drivers.

Eleven standard devices are listed, so that a circuit designer may select the optimum device for his application. Input characteristics, number of drivers, package style, and output voltage are tabulated for each device in the Device Type Number Designation chart. With any device, the output load is activated when the input is pulled towards the positive supply (active 'high'). All units operate over the temperature range of -20°C to +85°C.

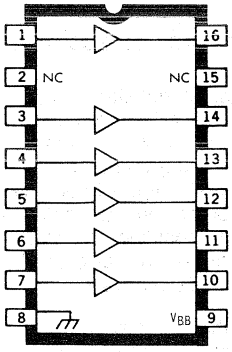
FEATURES

- Digit or Segment Drivers
- Low Input Current
- Integral Output Pull-Down Resistors
- High Output Breakdown Voltage
- Single or Split Supply Operation

Always order by complete part number, e.g., **UDN6118R-2** . See matrix on third page. Note that all devices are not available in all package types.

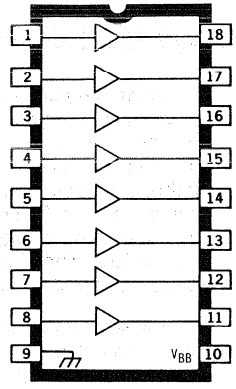
6116 AND 6118
FLUORESCENT DISPLAY DRIVERS

UDN6116A/R*



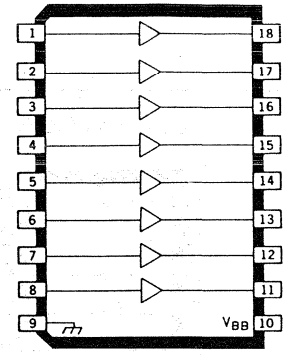
Dwg. No. A-9643A

UDN6118A/R*



Dwg. No. A-9641A

UDN6118LW

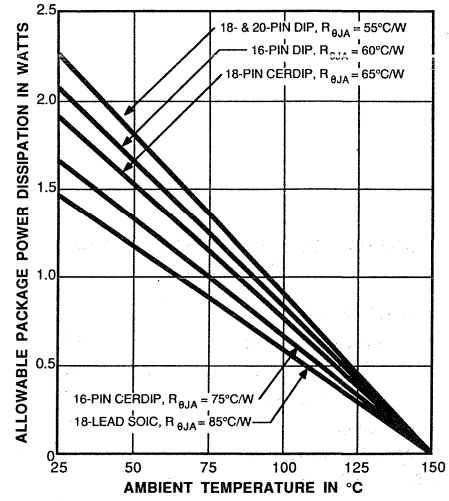


Dwg. No. A-14,370

* Always specify complete part number, such as:

UD N 6116 A – 2

- **INSTRUCTIONS:** SELECTED VERSION. SEE TYPE NUMBER DESIGNATION, NEXT PAGE
- **PACKAGE:** A = PLASTIC DIP; LW = PLASTIC SOIC; R = CERAMIC DIP
- **DEVICE TYPE.**
- **OPERATING TEMPERATURE RANGE.** N = -20°C to +85°C
- **FAMILY.** UD = DIGITAL DRIVERS



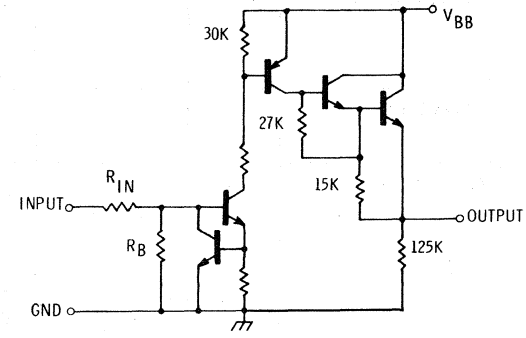
Dwg. GP-022

6116 AND 6118
FLUORESCENT DISPLAY DRIVERS

DEVICE TYPE NUMBER DESIGNATION

Input Compatibility	No. of Drivers	V_{OUT}	No. of Pins	Type Number		
				Plastic DIP	Ceramic DIP	Plastic SOIC
5 V TTL, CMOS	6	60 V	16	UDN6116A-2	UDN6116R-2	—
		80 V	16	UDN6116A	UDN6116R	—
		110 V	16	UDN6116A-1	—	—
	8	60 V	18	UDN6118A-2	UDN6118R-2	—
		80 V	18	UDN6118A	UDN6118R	UDN6118LW
		110 V	18	UDN6118A-1	—	—

PARTIAL SCHEMATIC
ONE DRIVER (ALL TYPES)



Dwg. No. A-10,592C

R_{IN}	R_B
10 kΩ	30 kΩ

ELECTRICAL CHARACTERISTICS (over operating temperature range).

Note: All Values Specified At —

Suffixes	A	LW	R	A-1	A-2	R-2	
V_{BB} =	80	80	80	110	60	60	Volts

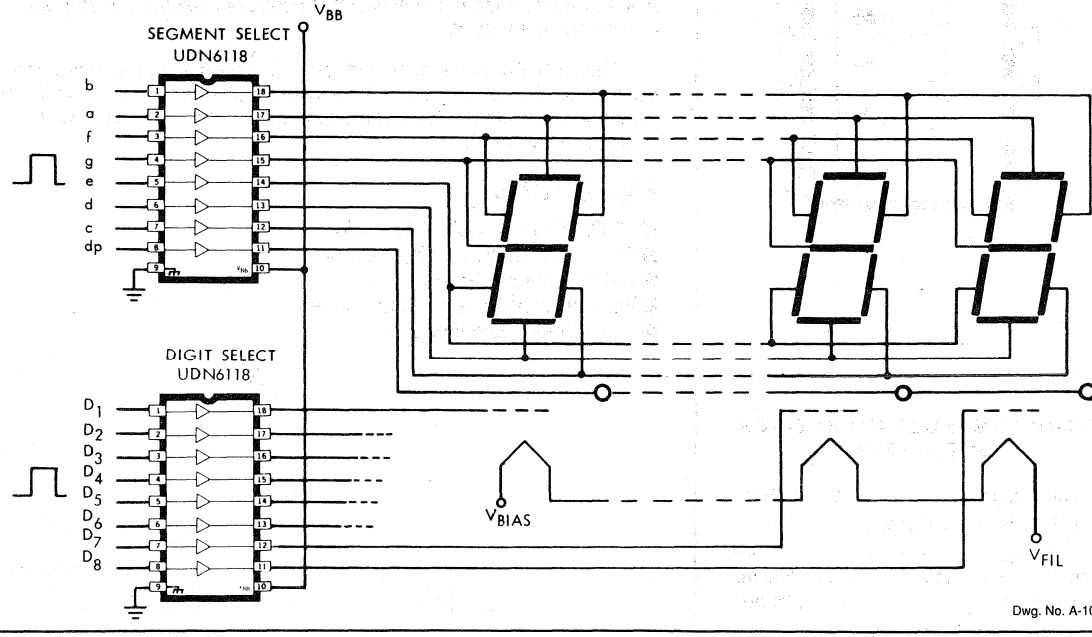
Characteristic	Symbol	Applicable Devices		Test Conditions	Limits			
		Basic Part. No.	Suffix		Min.	Typ.	Max.	Units
Output Leakage Current	I_{OUT}	All	All	V_{IN} = 0.4 V	—	—	15	µA
Output OFF Voltage	V_{OUT}	All	All	V_{IN} = 0.4 V	—	—	1.0	V
Output Pull-Down Current	I_{OUT}	All	A, LW, or R	Input Open, $V_{OUT} = V_{BB}$	450	650	1100	µA
			A-1		600	900	1500	µA
			A-2 or R-2		350	500	775	µA
Output ON Voltage	V_{OUT}	All	A, LW, or R	V_{IN} = 2.4 V, I_{OUT} = -25 mA	77	78	—	V
			A-1		107	108	—	V
			A-2 or R-2		57	58	—	V
Input ON Current	I_{IN}	All	All	V_{IN} = 2.4 V	—	120	225	µA
				V_{IN} = 5.0 V	—	375	650	µA
Supply Current	I_{BB}	All	All	All Inputs Open	—	10	100	µA
		UDN6116	A or R	All Inputs = 2.4 V	—	5.0	7.5	mA
			A-1	Two Inputs = 2.4 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 2.4 V	—	4.0	6.0	mA
		UDN6118	A, LW, or R	All Inputs = 2.4 V	—	6.0	9.0	mA
			A-1	Two Inputs = 2.4 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 2.4 V	—	5.5	8.0	mA

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Applicable Devices		Test Conditions	Limits			
		Basic Part. No.	Suffix		Min.	Typ.	Max.	Units
Supply Voltage	V_{BB}	UDN6116/18	A, LW, or R		5.0	—	70	V
			A-1		5.0	—	100	V
			A-2 or R-2		5.0	—	50	V
Input ON Voltage	V_{IN}	UDN6116/18	All		2.4	—	15	V
Output ON Current	I_{OUT}	All	All		—	—	-25	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

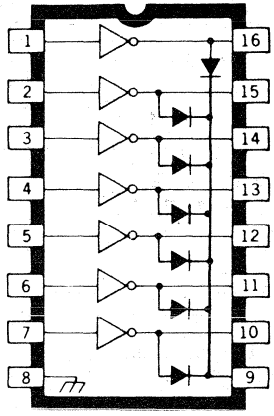
TYPICAL MULTIPLEXED FLUORESCENT DISPLAY



Dwg. No. A-10,261B

7003

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAY



Dwg. No. A-9594

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{CEX} . . . . . **150 V**
Output Sustaining Voltage,
$V_{CE(sus)}$ . . . . . **90 V**
Output Current, I_C . . . . . **300 mA**
Input Current, I_{IN} . . . . . **25 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Output current may be limited by duty cycle, number of drivers operating, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified maximum current rating or a junction temperature of 150°C.

Containing seven high-voltage, high-current Darlington power drivers, the ULN7003A is designed for interfacing between TTL or MOS logic and a variety of peripheral loads such as relays, stepper motors, print heads, and lamps. The four open-collector Darlington outputs feature 150 V minimum breakdowns (90 V sustaining) and integral power diodes for switching inductive loads.

The ULN7003A includes input current-limiting resistors for operation from TTL or CMOS operating at a nominal supply voltage of 5 V.

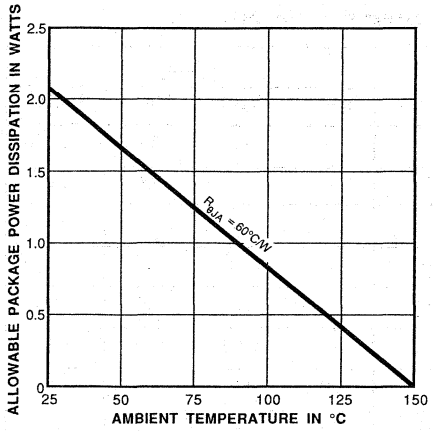
The high sustaining voltage rating of this device makes it ideal for inductive load applications where Zener diode flyback techniques are used. The increased flyback voltage provides a much faster inductive load turn-OFF current decay which is especially useful with stepper motors and printheads.

The ULN7003A is pinned with outputs opposite inputs to facilitate ease of circuit board layout. It is supplied in a 16-pin plastic dual in-line package with a copper lead frame to maximize their device power dissipation capabilities.

FEATURES

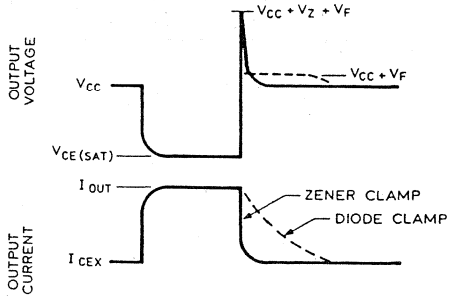
- 150 V Minimum Output Breakdown
- 90 V Minimum Sustaining Voltage
- 300 mA Output Current
- Internal High-Current Clamp Diodes
- Logic-Compatible Inputs

Always order by complete part number: **ULN7003A** .



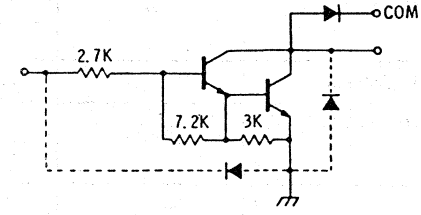
Dwg. GP-016

A Zener diode can be used to increase the flyback voltage. This gives a much faster inductive load turn-OFF current decay. The maximum Zener voltage plus the load supply voltage plus the internal diode forward voltage must not exceed the device's rated sustaining voltage.



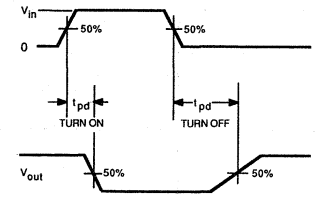
Dwg. WP-001

PARTIAL SCHEMATIC
(ONE OF SEVEN DRIVERS)



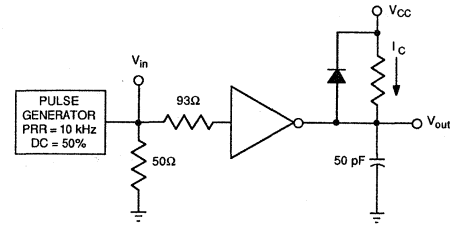
Dwg. No. A-9651

SWITCHING DELAY TEST CIRCUIT



Dwg. WP-010

V_{in} = 3.5 V for ULN7003A



Dwg. EP-020

7003
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAY

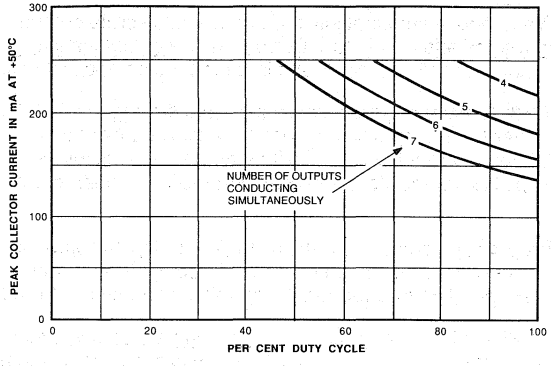
ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 150 V	—	—	50	µA
		V_{CE} = 150 V, T_A = +70°C	—	—	100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_C = 200 mA, L = 2 mH	90	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA, I_{IN} = 250 µA	—	1.1	1.3	V
		I_C = 250 mA, I_{IN} = 350 µA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	V_{IN} = 3.85 V	—	0.93	1.35	mA
	$I_{IN(OFF)}$	I_C = 500 µA, T_A = +70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
		V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
Input Capacitance	C_{IN}		—	15	25	pF
Switching Delay	t_{pd}	Turn On, I_C = 250 mA	—	0.05	0.5	µs
		Turn Off, I_C = 250 mA	—	0.5	1.0	µs
Clamp Diode Leakage Current	I_R	V_R = 150 V	—	—	50	µA
		V_R = 150 V, T_A = +70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 250 mA	—	1.7	2.0	V

Typical Data is for design information only.

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

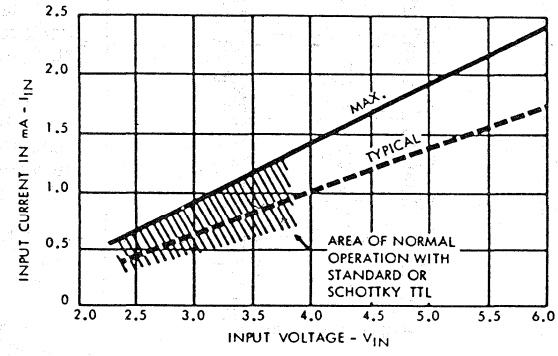
at T_A = +50°C



Dwg. GP-015

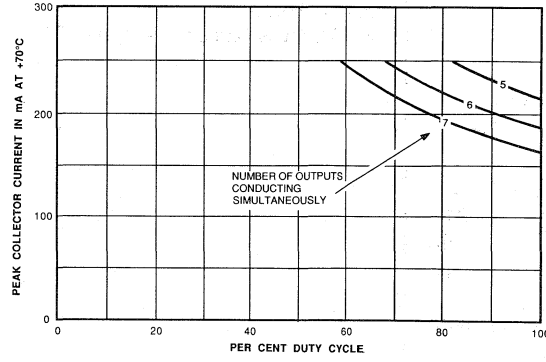
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

at T_A = +25°C



Dwg. No. A-9756B

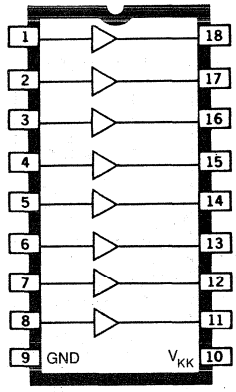
at T_A = +70°C



Dwg. GP-015-1

7180

GAS-DISCHARGE DISPLAY SEGMENT DRIVER



Dwg. No. A-9640A

ABSOLUTE MAXIMUM RATINGS at + 25°C

Supply Voltage, V_{KK} . . . . . **-115 V**
Input Voltage, V_{IN} . . . . . **+20 V**
Output Current, I_{OUT} . . . . . **20 mA**
Power Dissipation, P_D . . . . . **2.2 W***
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

*Derate at the rate of 18 mW/°C above 25°C

Due to the high input impedance of these devices, they are susceptible to static discharge damage sometimes associated with handling and testing. Therefore, techniques similar to those used for handling MOS devices should be employed.

The UDN7180A segment driver is a monolithic high-voltage bipolar integrated circuit for intertacing between MOS or other low-voltage circuits and the cathode of gas-discharge display panels.

These drivers reduce substantially the number of discrete components required with panels (Beckman, Burroughs, Dale, Matsushita, NEC, Pantek, etc) in calculator, clock and instrumentation applications.

The UDN7180A driver requires external current limiting and is intended for higher-current applications or where individual outputs are operated at different current levels (i.e. with alpha-numeric displays). All inputs have pull-down resistors for direct connection to open-drain PMOS logic.

This device provides output currents suitable for display segments in a wide variety of display sizes and number of display digits. Either a fixed split supply operation or a feedback-controlled scheme is allowed.

The UDN7180A driver can be used in a wide variety of low-level to high-voltage applications utilizing gas-discharge displays such as those found in calculators, clocks, point-of sale terminals, and instruments. Its high reliability combined with minimum size, ease of installation, and the cost advantages of a complete monolithic interface make it the ideal choice in many applications.

FEATURES

- Reliable Monolithic Construction
- High Output Breakdown Voltage
- Low Power
- TTL/MOS Compatible Inputs

Always order by complete part number: **UDN7180A** .

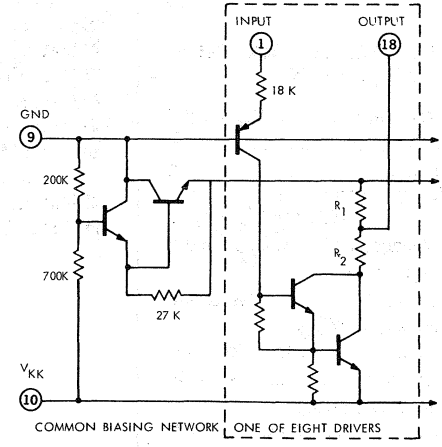
7180
GAS-DISCHARGE DISPLAY SEGMENT DRIVER

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{KK} = 110 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output ON Voltage	V_{ON}	All inputs at 2.4 V, I_{ON} = 14 mA	-105	-108	—	V
Output OFF Voltage	V_{OFF}	All inputs at 0.4 V, Reference V_{KK}	76	84	—	V
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.4 V, V_{KK} = -110 V, Test output held at -66 V	-95	-120	-155	µA
Input High Current	I_{IH}	Test input at 2.4 V, Other inputs at 0 V	—	100	200	µA
Input Low Current	I_{IL}	Test input at 0.4 V, One input at 2.4 V, Other inputs at 0.4 V	—	1.0	10	µA
Supply Current	I_{KK}	All inputs at 0 V	—	-125	-175	µA

NOTES: 1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ DVM or VTVM.
3. Recommended V_{KK} operating range -85 to -110 V.
4. Positive (negative) current is defined as going into (coming out of) the specified device pin.

PARTIAL SCHEMATIC

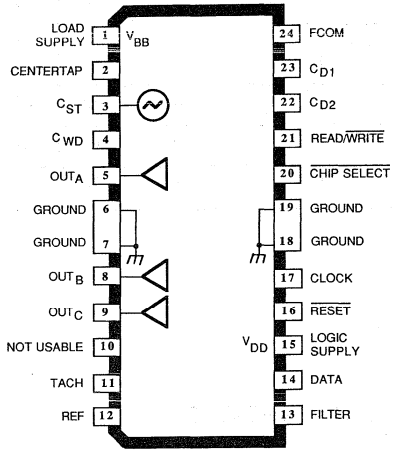


R_1 = 350 kΩ
R_2 = 0 Ω

Dwg. No. A-9644C

8901

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH BACK-EMF SENSING



Dwg. PP-032

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB} ..... V_{DD} + 1.0 V
Output Current, I_{OUT} (peak) ..... ±1.5 A
(continuous) ..... ±1.1 A
Logic Input Voltage Range, V_{IN} ..... -0.3 V to V_{DD} + 0.3 V
Logic Supply Voltage, V_{DD} ..... 6.0 V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range T_A ..... -20°C to +85°C
Junction Temperature, T_J ..... +150°C†
Storage Temperature Range, T_S ..... -55°C to +150°C

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

The A8901SLB is a three-phase DMOS back-EMF sensing spindle motor driver for use in 5 V Winchester disc drives. The power output stages are capable of 1 A output currents and have 1.4 Ω (total resistance) DMOS power outputs for low power dissipation. Intrinsic ground clamp and flyback diodes are provided for driving inductive loads. Thermal shutdown circuitry is provided to protect the device from excessive junction temperatures.

Internal logic and analog detection circuitry provide complete sequencing of the outputs during start-up and run modes without the need for external Hall-effect position-sensing devices. Internal linear control of the output current is used in conjunction with external circuitry to provide frequency- or phase-locked loop speed control. A serial port allows the user flexibility in programming the maximum start-up current level, sleep mode, and system diagnostics.

The A8901SLB is provided in a 24-lead wide-body, small-outline plastic power package (SOIC) for surface-mount applications. The copper batwing provides for maximum package power dissipation in the smallest possible construction.

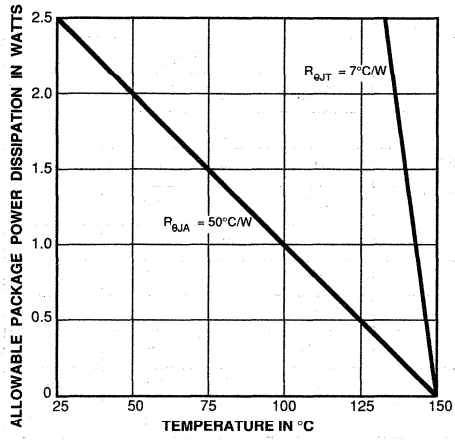
FEATURES

- DMOS Outputs
- Low $r_{DS(on)}$ -1.4 Ω Maximum Total
- Back-EMF Commutation Circuitry
- Programmable Start-Up Current
- Diagnostics Mode
- Sleep Mode
- Linear Current Control
- Internal Thermal Shutdown Circuitry
- Power Surface-Mount Package

Always order by complete part number: **A8901SLB**.

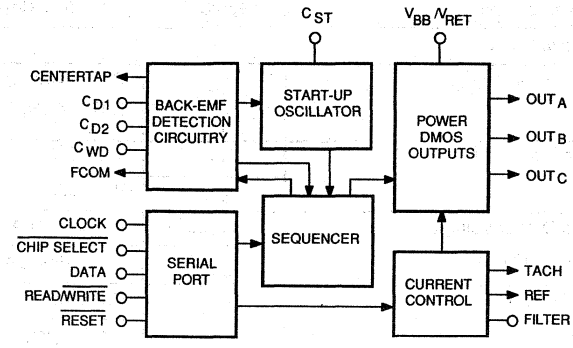
PRELIMINARY

8901
3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER



Dwg. GP-019

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-017A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = V_{DD} = 5.0 V

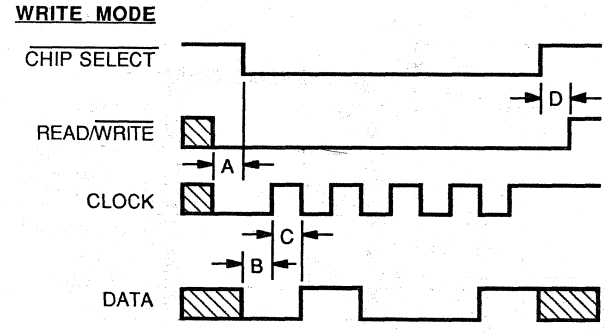
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Supply Current	I_{DD}	Operating	—	7.5	10	mA
		Sleep Mode	—	—	500	µA
Load Supply Voltage	V_{BB}	Operating	—	—	V_{DD} + 1	V
Thermal Shutdown	T_J		—	165	—	°C
Thernal Shutdown Hysteresis	ΔT_J		—	20	—	°C
Output Drivers						
Output Leakage Current	I_{DSX}	V_{OUT} = 7.0 V	—	—	300	µA
		V_{OUT} = 0 V	—	—	-300	µA
Total Output ON Resistance (Source + Sink + R_S)	$r_{DS(on)}$	I_{OUT} = 900 mA, Pulse Test	—	1.2	1.4	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	I_{OUT} = 900 mA, L = 3 mH	6.0	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.0	1.5	V

Continued next page...

ELECTRICAL CHARACTERISTICS continued

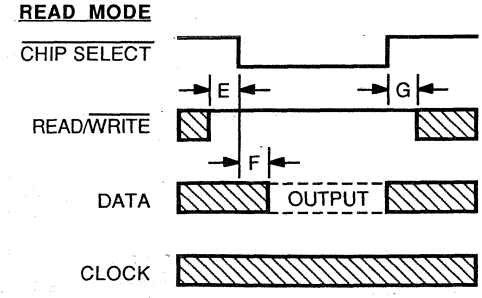
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	DATA, RESET, CLK, REF, R/W, TACH, CHIP SELECT	-0.3	—	1.5	V
	$V_{IN(1)}$		3.5	—	5.3	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-0.5	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	1.0	µA
Logic Output Voltage (DATA and FCOM)	$V_{OUT(0)}$	I_{OUT} = 500 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -500 µA	3.5	—	—	V
C_{ST} Current	I_{CST}	Charging	16	20	28	µA
		Discharging	-16	-20	-28	µA
Filter Current	I_{FILTER}	Charging	8.0	10	15	µA
		Discharging	-8.0	-10	-15	µA
C_D Current (C_{D1} or C_{D2})	I_{CD}	Charging	16	20	30	µA
		Discharging	-35	-44	-72	µA
C_D Current Matching	—	$I_{CD(DISCHRG)}/I_{CD(CHRG)}$	2.0	2.2	2.4	—
C_{WD} Current	I_{CWD}	Charging	16	20	28	µA
C_{WD} Trip Voltage	V_{TL}		0.45	0.50	0.55	V
	V_{TH}		2.25	2.50	2.75	V
Clock Frequency	f_{CLK}		3.3	—	—	MHz
I_{OUT}(MAX) Accuracy	—	I_{OUT}(MAX) = 0.8 A or 1.0 A	—	—	±20	%
Transconductance Gain	g_m		0.40	0.50	0.60	A/V
Centertap Resistors	R_{CT}		5.5	10	12	kΩ

SERIAL PORT TIMING CONDITIONS



p/o Dwg. WP-014

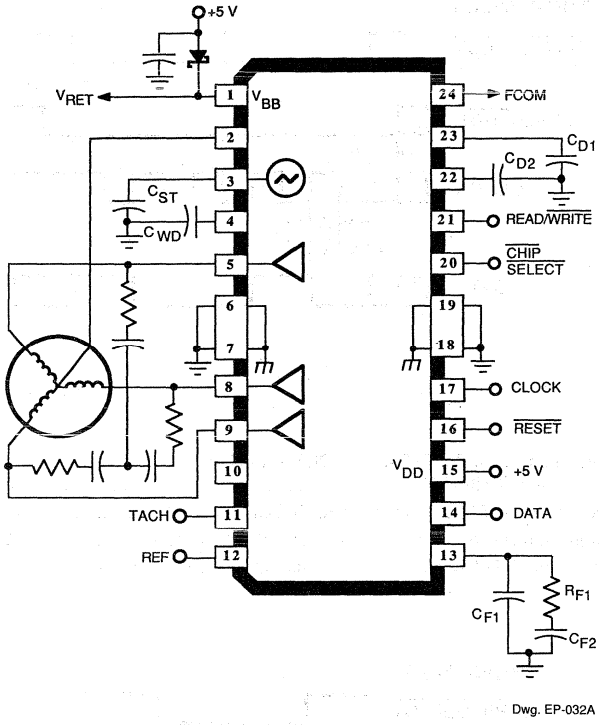
A. Minimum READ/WRITE and CLOCK setup time before CHIP SELECT ..... **150 ns**
B. Minimum DATA setup time before CLOCK rising edge ..... **150 ns**
C. Minimum DATA hold time before CLOCK falling edge ..... **150 ns**
D. Minimum READ/WRITE hold time after CHIP SELECT disable ..... **150 ns**



p/o Dwg. WP-014

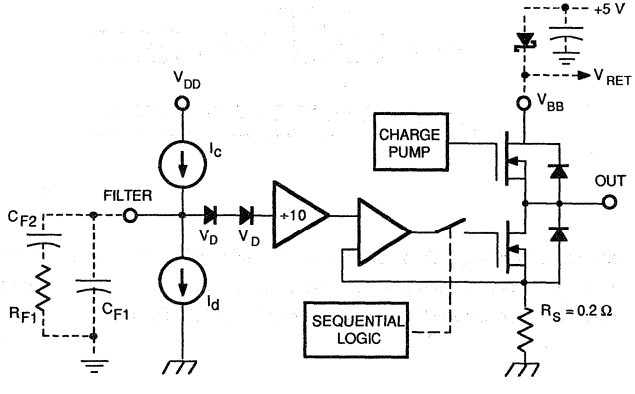
E. Minimum READ/WRITE setup time before CHIP SELECT ..... **150 ns**
F. Minimum time until output DATA valid ..... **150 ns**
G. Minimum READ/WRITE hold time after CHIP SELECT disable ..... **150 ns**

TYPICAL APPLICATION



Dwg. EP-032A

FIGURE 1



Dwg. EP-031

FUNCTIONAL DESCRIPTION

Power Outputs. The power outputs of the A8901SLB are DMOS transistors with a total source plus sink $r_{DS(on)}$ of less than 1.4 Ω. Intrinsic ground clamp and flyback diodes (see Figure 1) clamp transient voltage spikes when switching inductive loads. Internal charge pump circuitry is used to drive the gates of the N-channel source drivers to their required gate voltages. The truth table for the output drivers sequencing is:

SEQUENCER STATE	OUT_A	OUT_B	OUT_C
1	HIGH	LOW	Z
2	Z	LOW	HIGH
3	LOW	Z	HIGH
4	LOW	HIGH	Z
5	Z	HIGH	LOW
6	HIGH	Z	LOW

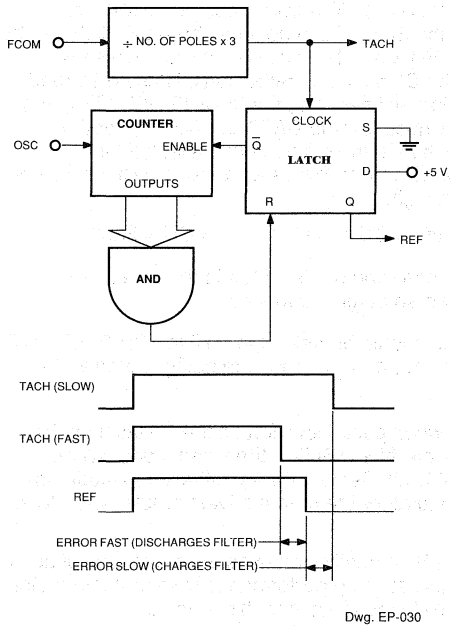
Current Control. The A8901SLB provides linear current control of the sink drivers during start-up and running modes. In the start up mode, the maximum load current can be programmed via the serial port (see Serial Port). During the running mode, the output current is linearly controlled for low noise in frequency-locked or phase-locked speed-control systems. To accomplish this, the load current is monitored by an internal sense resistor (R_S). The voltage across the sense resistor is compared to one-tenth the voltage at the FILTER pin less two diode drops, generating an error voltage to drive the gate of the appropriate output sink transistor. This creates a load current that is proportional to the voltage at the FILTER pin less two diode drops. This transconductance function is $I_{OUT} = (V_{FILTER}-2\ V_D)/10\ R_S$. Where R_S is approximately 0.2 Ω and V_D is approximately 0.7 V.

Speed Control. The A8901SLB has been configured to operate in conjunction with external digital circuitry to provide frequency-locked loop speed control of spindle motors. The TACH and REF inputs are used to turn ON current sources I_c and I_d to charge and discharge a lead/lag loop filter compensation network (see Figure 2). The truth table for this function is:

REF	TACH	I_c	I_d
0	0	off	off
0	1	on	off
1	0	off	on
1	1	off	off

The external circuitry required for implementation of the speed control loop is shown in Figure 2. The operation of this circuit is as follows: the FCOM signal is a logic signal that changes state every time the A8901SLB self commutates. By dividing the FCOM signal by three times the number of poles in the motor, a TACH signal is developed that changes state every mechanical revolution. This is done to develop a low-jitter tachometer signal. The low jitter is achieved because each time the TACH signal changes state the back-EMF circuitry is looking at the same magnet pole pair.

FIGURE 2



Dwg. EP-030

The derived TACH signal is compared to the desired time (REF) for one revolution. This is done by using the positive-going edge of the tach signal to trigger a latch that enables a counter. The counter is driven by an accurate oscillator signal and (in conjunction with an AND gate) is used to count the desired number of oscillator cycles in a single revolution. When the counter reaches its desired number the latch is reset and the REF signal goes low (see Figure 2). The TACH and REF signals are fed back to the A8901SLB to charge and discharge the filter compensation network. If the TACH signal goes low before REF an Error-Fast signal turns ON I_d lowering the current in the motor and thereby reducing its speed. If the REF signal goes low before TACH an Error-Slow signal turns ON I_c which increases the load current and thereby the speed of the motor. The loop filter components are used to dampen the response of the loop and achieve optimal settling time.

Response time to disturbances in speed can be improved by synchronizing to sector data once information is being read from the disc. This change can be made by changing the count number in the counter and switching TACH to a sector tachometer signal. This should be done when TACH and REF are in the low state so as not to generate an erroneous error signal.

Microprocessor-controlled phase-locked loop speed-control systems can use the FILTER pin as a transconductance input by omitting the loop filter components and connecting TACH and REF to ground.

Start-up and Back-EMF Commutation Circuitry. The A8901SLB provides sensorless operation of three-phase bipolar brushless dc motors. This is done by randomly energizing one of the six output commutation states to start the motor moving. The motor's back-EMF is then quickly examined to determine if the motor is moving in the correct direction and if the drivers are in their correct output states. If they are not, the output drivers are advanced to the next state in the output sequence and the process repeats itself. If the motor is synchronized to the correct output commutation state, and moving in the right direction, the back-EMF circuitry disables the start-up circuitry and continues to commutate the motor off the back-EMF signals in the windings.

Serial Port. The serial port functions to both read and write information to and from the A8901SLB. The serial port is enabled/disabled by the CHIP SELECT pin. When CHIP SELECT is high, the serial port is disabled and the chip is not affected by changes in data at the DATA, CLOCK, or READ/WRITE pins. When the CHIP SELECT is low, the serial port functions in the read or write mode depending on the READ/WRITE pin.

Write Mode (READ/WRITE Low). To write data to the serial port, the READ/WRITE pin and the CLOCK pin should be low prior to the CHIP SELECT pin going low. Once CHIP SELECT goes low, information on the DATA pin is read into the shift register on the positive-going transition of the CLOCK. There are five bits in the serial input port. Their functions are:

D0 - Sleep/Run Mode; LOW = Sleep, HIGH = Run
This bit allows the A8901SLB to be powered down when not in use.

D1 - Step Mode; LOW = Normal Operation, HIGH = Step Only
When in the step-only mode, the back-EMF detection circuitry is disabled and the power outputs are stepped through their normal commutation sequence by the start-up oscillator. This mode is intended to facilitate device and system testing.

D2 - Read Output Select; LOW = Thermal Shutdown Status, HIGH = Sequencer Pulse.

D3 and D4 - These two bits set the maximum output current according to the following truth table:

D3	D4	I_{OUT} (MAX)
0	0	1 A
0	1	800 mA
1	0	600 mA
1	1	400 mA

Data written into the serial port is latched and becomes active upon the low-to-high transition of the CHIP SELECT pin at the end of the write cycle. D0 will be the last bit written to the serial port.

Read Mode (READ/WRITE High). The transitions of the start-up oscillator or the status of the thermal shutdown of the A8901SLB can be read from the serial port DATA pin. The choice between these two functions is selected by the D2 bit in the serial port's latches. To read data the READ/WRITE pin must be high prior to CHIP SELECT going low. When CHIP SELECT goes low the DATA pin will register the status of the selected function. If the status of the selected function is changing, the data output will reflect this as long chip select is held low and READ/WRITE is held high.

Thermal Shutdown Status: LOW = No Fault, HIGH = Fault

Oscillator: Each change represents a step to the next state in the six-step output sequence.

The READ/WRITE pin should be held high until the CHIP SELECT pin has returned to high to avoid erroneous data being written to the device.

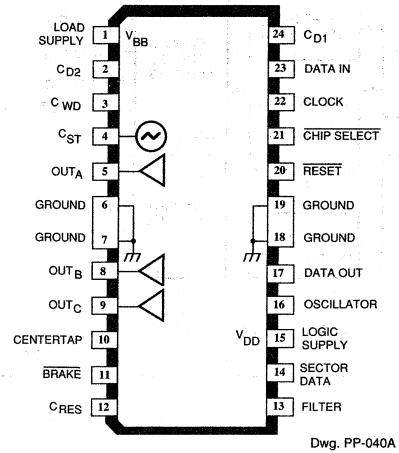
Reset. The RESET pin, when pulled low, forces the D0 latch on the serial port low which puts the A8901SLB in the sleep mode. When RESET is high, the D0 bit is unaffected. When in the sleep mode, the FILTER pin is pulled high to allow the output drivers to fully saturate at startup.

Centertap. The A8901SLB internally simulates the centertap voltage of the motor. To obtain reliable start-up performance from motor to motor, the motor centertap should be connected to this terminal.

External Component Selection. Information regarding the selection of external component values is available.

8902 AND 8903

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING



Dwg. PP-040A

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB}
A8902SLB ..... V_{DD} + 1.0 V
A8903SLB ..... 14 V
Output Current, I_{OUT} (peak) ..... ±1.5 A
(continuous) ..... ±1.1 A
Logic Input Voltage Range,
V_{IN} ..... -0.3 V to V_{DD} + 0.3 V
Logic Supply Voltage, V_{DD} ..... 6.0 V
Package Power Dissipation,
P_D ..... See Graph
Operating Temperature Range,
T_A ..... -20°C to +85°C
Junction Temperature, T_J ..... +150°C†
Storage Temperature Range,
T_S ..... -55°C to +150°C

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

The A8902SLB and A8903SLB are three-phase DMOS back-EMF sensing spindle motor drivers for use in 5 V and 12 V Winchester disc drives, respectively. The power output stages are capable of ±1 A output currents and have 1 Ω (total resistance, typical) DMOS power outputs for low power dissipation. Intrinsic ground clamp and flyback diodes are provided for driving inductive loads. Thermal shutdown circuitry is provided to protect the devices from excessive junction temperature.

Internal logic and analog detection circuitry provide complete sequencing of the outputs during start-up and run modes without the need for external Hall-effect position-sensing devices. Internal linear control of the output current is used to provide frequency-locked loop speed control. A serial port allows the user flexibility in programming the reference frequency count number which determines motor speed. Additionally, the serial port provides user programmability of maximum start-up current levels, a sleep mode, and system diagnostics.

Both devices are provided in 24-lead wide-body, small-outline plastic power packages (SOICs) for surface-mount applications. The copper batwing provides for maximum package power dissipation in the smallest possible construction.

FEATURES

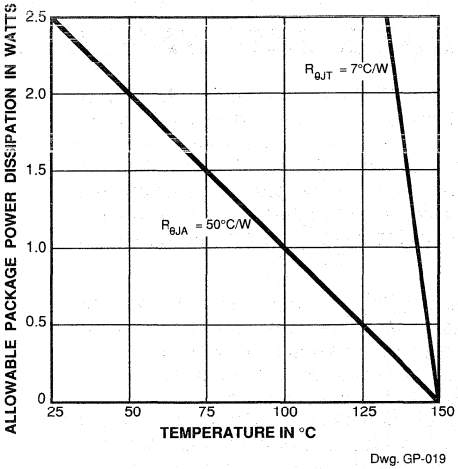
- DMOS Outputs
- Low $r_{DS(on)}$ - 1 Ω Typical Total
- Back-EMF Commutation Circuitry
- Frequency-Locked Loop Speed Control
- Sector Data Tachometer Signal Input
- Programmable Start-Up Current
- Diagnostics Mode
- Sleep Mode
- Linear Current Control
- Dynamic Braking With Delay
- System Diagnostics Data Out
- Internal Thermal Shutdown Circuitry
- Power Surface-Mount Package

Always order by complete part number:

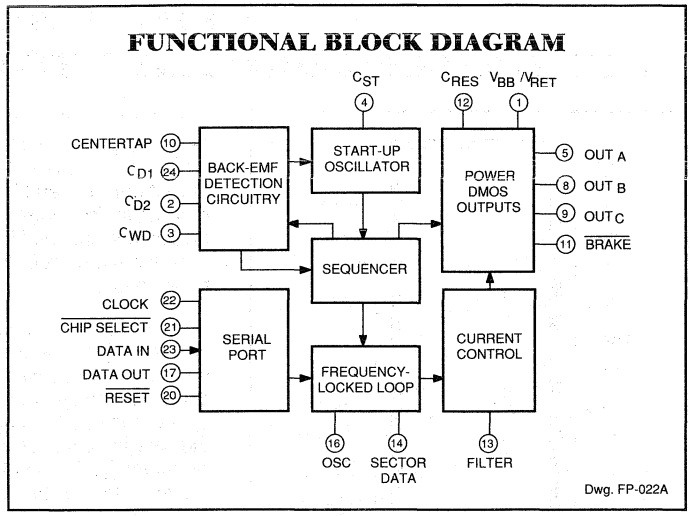
A8902SLB	**5 Volt Drive**
A8903SLB	**12 Volt Drive**

PRELIMINARY

8902 AND 8903
3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING



Dwg. GP-019



Dwg. FP-022A

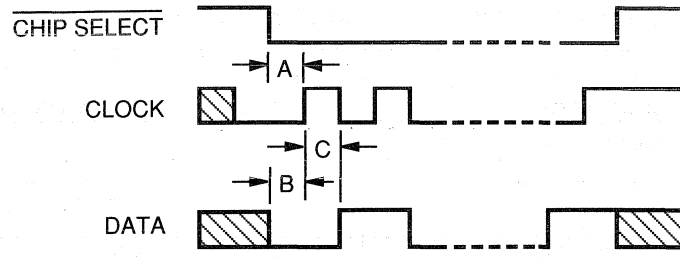
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V, V_{BB} = 5.0 V (A8902SLB) or 12 V (A8903SLB)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Supply Current	I_{DD}	Operating	—	7.5	10	mA
		Sleep Mode	—	—	500	µA
Load Supply Voltage	V_{BB}	A8902SLB, Operating	—	5.0	6.0	V
		A8903SLB, Operating	—	12	14	V
Thermal Shutdown	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	20	—	°C
Output Drivers						
Output Leakage Current	I_{DSX}	A8902SLB, V_{OUT} = 6.0 V	—	100	300	µA
		A8903SLB, V_{OUT} = 14 V	—	100	300	µA
		V_{OUT} = 0 V	—	-100	-300	µA
Total Output ON Resistance (Source + Sink + R_S)	$r_{DS(on)}$	I_{OUT} = 900 MA, Pulse Test	—	1.1	1.4	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	A8902SLB, I_{OUT} = 900 mA, L = 3 mH	7.0	—	—	V
		A8903SLB, I_{OUT} = 900 mA, L = 3 mH	14	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.25	1.5	V

Continued next page...

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	DATA, RESET, CLK, CHIP SELECT	-0.3	—	1.5	V
	$V_{IN(1)}$	DATA, RESET, CLK, CHIP SELECT	3.5	—	5.3	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-0.5	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	1.0	µA
DATA Output Voltage	$V_{OUT(0)}$	I_{OUT} = 500 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -500 µA	3.5	—	—	V
C_{ST} Current	I_{CST}	Charging	16	20	24	µA
		Discharging	-16	-20	-24	µA
Filter Current	I_{FILTER}	Charging	8.0	10	12	µA
		Discharging	-8.0	-10	-12	µA
C_D Current (CD_1 or C_{D2})	I_{CD}	Charging	16	20	24	µA
		Discharging	-35	-44	-53	µA
C_D Current Matching	—	$I_{CD(DISCHRG)}/I_{CD(CHRG)}$	2.1	2.2	2.3	—
C_{WD} Current	I_{CWD}	Charging	16	20	24	µA
C_{WD} Trip Voltage	V_{TL}		0.45	0.50	0.55	V
	V_{TH}		2.25	2.50	2.75	V
Clock Frequency	f_{CLK}		3.3	—	—	MHz
FLL Oscillator Frequency	f_{OSC}		—	>10	—	MHz
I_{OUT}(MAX) Accuracy	—		—	±10	—	%
Transconductance Gain	g_m		0.45	0.50	0.55	A/V
Centertap Resistors	R_{CT}		8.0	10	12	kΩ



Dwg. WP-014-1

SERIAL PORT TIMING CONDITIONS

A. Minimum CHIP SELECT setup time before CLOCK rising edge ..... **150 ns**
B. Minimum DATA setup time before CLOCK rising edge ..... **150 ns**
C. Minimum DATA hold time before CLOCK falling edge ..... **150 ns**

FUNCTIONAL DESCRIPTION

Power Outputs. The power outputs of the A8902/03SLB are DMOS transistors with a total source plus sink $r_{DS(on)}$ of typically 1.1 Ω. Intrinsic ground clamp and flyback diodes clamp transient voltage spikes when switching inductive loads. Internal charge-pump circuitry is used to drive the gates of the N-channel source drivers to their required gate voltages. The truth table for the output drivers sequencing is:

SEQUENCER STATE	OUT_A	OUT_B	OUT_C
1	High	Low	Z
2	Z	Low	High
3	Low	Z	High
4	Low	High	Z
5	Z	High	Low
6	High	Z	Low

Braking. Dynamic braking of the motor, where all source drivers are turned OFF and all sink drivers are turned ON, is achieved by activating the BRAKE input or through the serial port - DATA IN. During power-down conditions, the external charge-pump storage capacitor is used to provide power to turn ON the three sink drivers which, due to their inherent capacitive input, will remain activated until the device is reset.

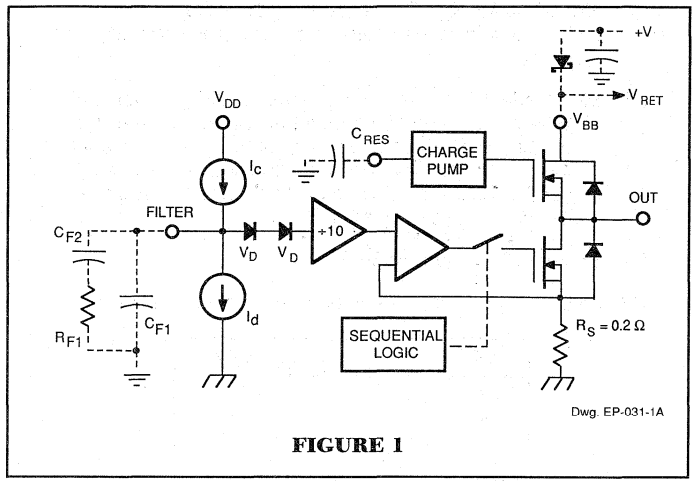


FIGURE 1

An external resistor/capacitor can be utilized in conjunction with the BRAKE input to provide a delay on braking (100 ms max.) during power down to ensure retraction of the voice coil head before spindle-motor braking is activated.

Current Control. The A8902SLB and A8903SLB provide linear current control of the sink drivers during start-up and running modes. In the start-up mode, the maximum load current can be programmed via the serial port (see Serial Port). During the running mode, the output current is linearly controlled for low noise in frequency-locked speed-control systems. Current control is achieved by monitoring the load current with an internal sense resistor (R_S). The voltage across the sense resistor is compared to one-tenth the voltage at the FILTER terminal less two diode drops, generating an error voltage to drive the gate of the appropriate output sink transistor. This creates a load current that is proportional to the voltage at the FILTER terminal less two diode drops. This transconductance function is $I_{OUT} = (V_{FILTER} - 2V_D)/10R_S$, where R_S is approximately 0.2 Ω and V_D is approximately 0.7 V.

Speed Control. The A8902/03SLB include a frequency-locked loop speed control system. This system operates by generating motor speed (TACH) and desired speed reference (REF) signals which are compared to provide a speed error signal, which is then used to turn ON current sources I_c and I_d, to charge or discharge a lead/lag loop filter compensation network at the FILTER terminal.

The circuitry implementing the speed control loop is shown in Figure 2. The operation of this circuit is as follows: the FCOM signal is a logic signal that changes state every time the A8902/03SLB detects a back-EMF zero crossing. By dividing the FCOM signal by three times the number of poles in the motor, a TACH signal is developed that changes state every mechanical revolution. This is done to develop a low-jitter tachometer signal.

The derived TACH signal is compared to the desired time (REF) for one revolution. This is done by using the positive-going edge of the TACH signal to trigger a latch that enables a programmable counter. The counter, driven by an accurate external oscillator signal, counts the desired number of oscillator cycles in a single revolution. The desired number of oscillator cycles is programmed via the serial port DATA IN.

$$\text{desired total count} = \frac{120 \times f_{osc}}{\text{desired motor speed (rpm)}}$$

When the counter reaches its desired number, the latch is reset and the REF signal goes low (see Figure 2). The TACH and REF signals are fed to the switchable current sources to charge and discharge the loop compensation network at the FILTER terminal. If the TACH signal goes low before REF an Error-Fast signal turns ON I_d lowering the current in the motor and thereby reducing its speed. If the REF signal goes low before TACH an Error-Slow signal turns ON I_c which

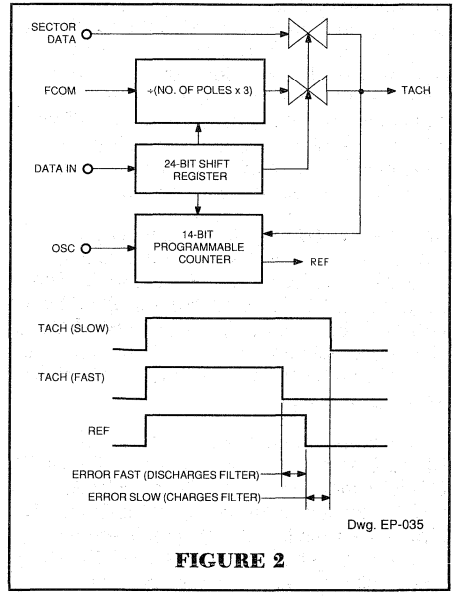


FIGURE 2

increases the load current and thereby the speed of the motor. The loop filter components are used to dampen the response of the loop and achieve optimal settling time.

Response time to disturbances in speed can be improved by synchronizing to sector data once information is being read from the disc. This change can be made by changing the count number in the programmable counter (see Serial Port) and switching TACH to a sector tachometer signal. This should be done when TACH and REF are in the low state so as not to generate an erroneous error signal. This can be achieved by programming the serial port to provide the SYNC signal (high) on the DATA OUT terminal which will indicate exact timing for the switch to sector data.

Start-Up and Back-EMF Commutation Circuitry. The A8902/03SLB provide sensorless operation of three-phase bipolar brushless dc motors. This is done by randomly energizing one of the six output commutation states to start the motor moving. The motor's back EMF is then quickly examined to determine if the motor is moving in the correct direction and if the drivers are in their correct output states. If they are not, the output drivers are advanced to the next state in the output sequence and the process repeats itself. If the motor is synchronized to the correct output commutation state, and moving in the right direction, the back-EMF circuitry disables the start-up circuitry and continues to commutate the motor off the back-EMF signals in the windings.

Serial Port - DATA IN. The serial port functions to write various operational and diagnostic modes to the A8902/03SLB. The serial port DATA IN is enabled/disabled by the CHIP SELECT input. When CHIP SELECT is high the serial port is disabled and the chip is not affected by changes in data at the DATA IN or CLOCK inputs.

To write data to the serial port, the CLOCK input should be low prior to the CHIP SELECT input going low. Once CHIP SELECT goes low, information on the DATA IN terminal is read into the shift register on the positive-going transition of the CLOCK. There are 23 bits in the serial input port. Their functions are:

D0 - Sleep/Run Mode; LOW = Sleep, HIGH = Run
This bit allows the device to be powered down when not in use.

D1 - Step Mode; LOW = Normal Operation, HIGH = Step Only
When in the step-only mode the back-EMF detection circuitry is disabled and the power outputs are stepped through their normal commutation sequence by the start-up oscillator. This mode is intended to facilitate device and system testing.

D2 - Brake; LOW = Run, HIGH = Brake.

D3 and D4 - These two bits set the maximum output current:

D4	D5	I_{OUT}(MAX)
0	0	1 A
0	1	800 mA
1	0	600 mA
1	1	400 mA

D5 thru D18 - This 14-bit word programs the REF time to set desired motor speed. The user provides the OSC input for the master clock to the 18-bit counter.

Bit Number	Count Number
D5	16
D6	32
D7	64
D8	128
D9	256
D10	512
D11	1 024
D12	2 048
D13	4 096
D14	8 192
D15	16 384
D16	32 768
D17	65 536
D18	131 072

D19 - This bit sets the frequency-locked loop synchronization;

LOW = Internal once-around speed signal, HIGH = External sector data.

D20 and D21 - These bits program the number of motor poles for the once-around FCOM counter:

D20	D21	Motor Poles
0	0	8
0	1	—
1	0	16
1	1	12

D22 and D23 - Controls the multiplexor for DATA OUT:

D22	D23	DATA OUT
0	0	Tach. (once around or sector)
0	1	Thermal Shutdown
1	0	Sync. (tach.-sector switch)
1	1	FCOM

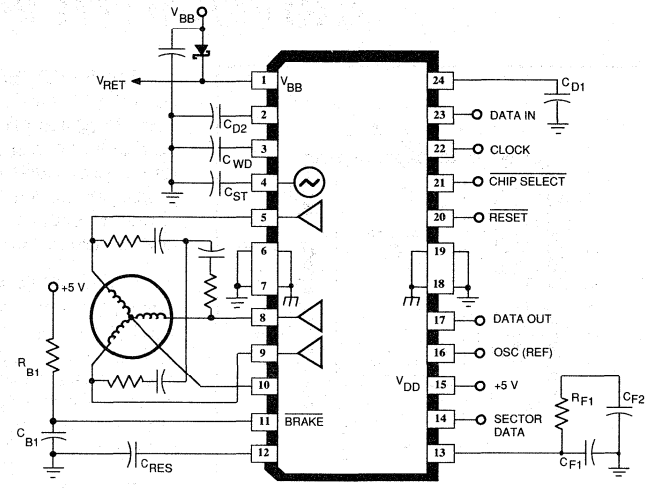
Data written into the serial port is latched and becomes active upon the low-to-high transition of the CHIP SELECT input at the end of the write cycle. D0 will be the last bit written to the serial port.

Reset. The RESET terminal when pulled low clears all serial port bits, including the DO latch which puts the A8902/03SLB in the sleep mode. When in the sleep mode, the FILTER terminal is pulled high to allow the output drivers to fully saturate at startup.

Centertap. The A8902/03SLB internally simulate the centertap voltage of the motor. To obtain reliable start-up performance from motor to motor, the motor centertap should be connected to this terminal.

External Component Selection. Applications information regarding the selection of external component values is available.

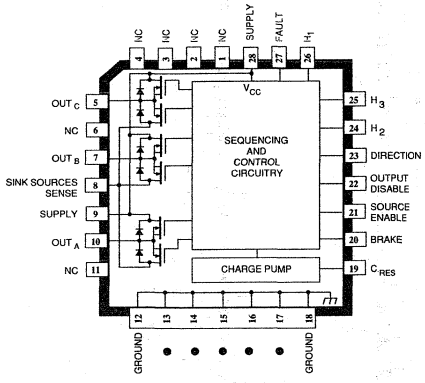
TYPICAL APPLICATION



Dwg. EP-036A

8922

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/ DRIVER WITH POWER DMOS OUTPUTS



Dwg. PP-033

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} ..... **14 V**
Output Current, I_{OUT} (≤ 500 ms) ..... **±3.0 A**
(continuous) ..... **±2.0 A**
Logic Input Voltage Range, V_{IN} ..... **-0.3 V to +6.0 V**
Package Power Dissipation, P_D ..... **See Graph**
Operating Temperature Range, T_A ..... **-20°C to +85°C**
Junction Temperature, T_J ..... **+150°C†**
Storage Temperature Range, T_S ..... **-55°C to +150°C**

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

The A8922SEA is a DMOS three-phase brushless dc motor controller/driver designed for use in streaming tape drives and other data storage applications. The power output stages are capable of ±2 A output currents and have less than 0.3 Ω DMOS power outputs for low power dissipation. Intrinsic ground clamp and flyback diodes protect the output drivers when switching inductive loads. Thermal shutdown circuitry is provided to protect the device from excessive junction temperatures.

The A8922SEA's CMOS commutation logic is compatible with motors that have digital Hall-effect sensors with 120° of electrical separation. Digital inputs to the device control direction, brake, and fast- or slow-decay PWM current control functions. The sources of the sink drivers are brought out to allow the user to sense current in the load with an external sense resistor. Internal charge-pump circuitry is provided to drive the N-channel DMOS source drivers to their required gate voltages.

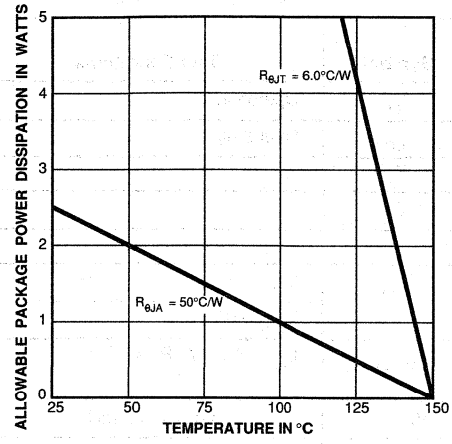
The A8922SEA is provided in a 28-lead PLCC power package for surface-mount applications. The copper half-batwing provides for maximum allowable package power dissipation in the smallest possible construction.

FEATURES

- DMOS Outputs
- Low $r_{DS(on)}$ - 0.6 Ω Maximum (source + sink)
- Fault Output Flag
- Internal Commutation Logic
- Brake Function
- Fast- or Slow-Decay PWM Current Control
- Internal Thermal Shutdown Circuitry
- Power Surface-Mount Package

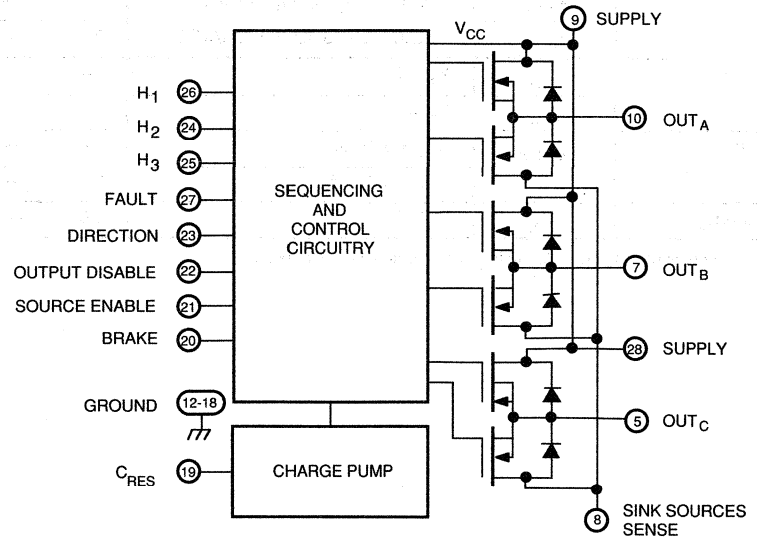
Always order by complete part number: **A8922SEA** .

PRELIMINARY



Dwg. GP-033

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-023

NOTE: There is an indeterminate resistance between terminals 9 and 28 and they must both be connected externally to the supply.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 12 V

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage	V_{CC}	Operating	10	12	14	V
Supply Current	I_{CC}	Operating	—	15	20	mA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	20	—	°C
Output Drivers						
Output Leakage Current	I_{DSX}	V_{OUT} = 14 V	—	10	200	µA
		V_{OUT} = 0 V	—	-10	-200	µA
Output ON Resistance (one transistor)	$r_{DS(on)}$	I_{OUT} = ± 2.0 A, Pulse Test	—	0.25	0.30	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	I_{OUT} = ± 3.0 A, L = 2 mH	15	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 2.0 A	—	1.25	1.5	V
Output Switching Time	t_r	I_{OUT} = ± 2.0 A , Resistive Load	—	1.5	—	µs
	t_f	I_{OUT} = ± 2.0 A , Resistive Load	—	1.5	—	µs
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	DISABLE, H_1, H_2, H_3, BRAKE,	—	—	0.8	V
	$V_{IN(1)}$	DIRECTION, SOURCE ENABLE	3.5	—	—	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-0.5	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	1.0	µA
FAULT Output Voltage	$V_{OUT(0)}$	I_{OUT} = 500 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -500 µA	3.5	—	—	V
Maximum PWM Frequency	f_{MAX}		30	—	—	kHz

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

COMMUTATION TRUTH TABLE

DISABLE = Low, SOURCE ENABLE = High.

Hall Sensor Inputs						Outputs		
H_1	H_2	H_3	DIRECTION	BRAKE	FAULT	OUT_A	OUT_B	OUT_C
High	Low	High	Low	Low	Low	High	Low	Z
High	Low	Low	Low	Low	Low	High	Z	Low
High	High	Low	Low	Low	Low	Z	High	Low
Low	High	Low	Low	Low	Low	Low	High	Z
Low	High	High	Low	Low	Low	Low	Z	High
Low	Low	High	Low	Low	Low	Z	Low	High
High	Low	High	High	Low	Low	Low	High	Z
High	Low	Low	High	Low	Low	Low	Z	High
High	High	Low	High	Low	Low	Z	Low	High
Low	High	Low	High	Low	Low	High	Low	Z
Low	High	High	High	Low	Low	High	Z	Low
Low	Low	High	High	Low	Low	Z	High	Low
High	High	High	X	Low	High	Z	Z	Z
Low	Low	Low	X	Low	High	Z	Z	Z
X	X	X	X	High	Low	Low	Low	Low

X = Irrelevant
Z = High Impedance

FUNCTIONAL DESCRIPTION

Power Outputs (OUT_A, OUT_B, and OUT_C). The power outputs of the A8922SEA are DMOS transistors each with a maximum $r_{DS(on)}$ of 0.3 Ω. Intrinsic ground clamp and flyback diodes clamp transient voltage spikes when switching inductive loads. Internal charge-pump circuitry is used to drive the gates of the N-channel source drivers to their required gate voltages. Load current may be sensed with an external sense resistor between SENSE and ground.

C_{RES}. A 0.22 µF capacitor should be connected from this terminal to ground. This capacitor serves as a charge-pump reservoir to allow the power outputs to be turned ON rapidly.

SOURCE ENABLE. The SOURCE ENABLE input when low disables the source drivers. When SOURCE ENABLE is high the output state of the source drivers is given in the Commutation Truth Table.

OUTPUT DISABLE. The OUTPUT DISABLE terminal when high turns OFF all the power output drivers. The OUTPUT DISABLE function is over-ridden by the BRAKE command when BRAKE is high.

DIRECTION. The DIRECTION input controls the order of sequencing of the output drivers. These states are given in the commutation truth table.

Hall Inputs (H_1, H_2, and H_3). The Hall inputs are configured to accept CMOS digital logic input levels. When using open-collector Hall effect devices, pull-up resistors to five volts will be required.

FAULT. The FAULT terminal when high indicates the presence of an invalid condition on the Hall inputs or the presence of a thermal shutdown condition. The thermal shutdown circuitry disables the output drivers in the event of excessive junction temperature.

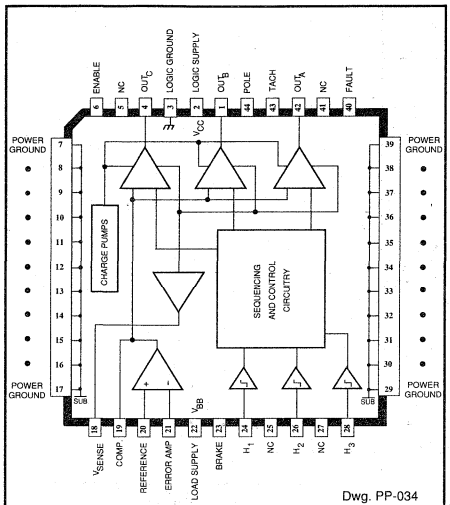
SENSE. The drains of the three sink drivers are brought out to this terminal to allow the user to connect a small-value sense resistor (typically 0.1 Ω) between this terminal and ground for sensing current in the load. If current sensing is not required, this terminal must be connected to ground.

SUPPLY (V_{CC}). These are the supply terminals for the A8922SEA. For correct operation both terminals should be connected together externally. Care should be taken to decouple this connection with a large-value capacitor as close to the package as possible to absorb load currents dumped back into the supply during the de-energization of the motor windings. These currents can cause the supply voltage to exceed the maximum voltage rating of the device if not properly decoupled.

GROUND. Terminals 12 through 18 are webbed together and attach to the die mounting area to form a low thermal resistance path to allow heat to be conducted out of the device. The power dissipation of the package can be further enhanced by soldering these terminals to a large area of copper foil on the printed wiring board.

8925

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH LINEAR CURRENT CONTROL AND POWER DMOS OUTPUTS



Dwg. PP-034

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Load Supply Voltage, V_{BB} ..... **14 V**
Output Current, I_{OUT} ..... **±4.0 A**
Logic Supply Voltage, V_{CC} ..... **14 V**
Logic Input Voltage Range,
V_{IN} ..... **-0.3 V to +6.0 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Junction Temperature, T_J ..... **+150°C†**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

† Fault conditions which produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

The A8925SEB is a DMOS three-phase brushless dc motor controller/driver designed for use in Winchester disc drives and other data storage applications. The power output stages are capable of ±4 A output currents and have DMOS power outputs with less than 0.25 Ω $r_{DS(on)}$ for low power dissipation. Intrinsic ground clamp and flyback diodes protect the output drivers when switching inductive loads. Thermal shutdown circuitry is provided to protect the device from excessive junction temperature.

A transconductance amplifier is used to linearly regulate the load current and control motor speed. Internal current-sensing circuitry eliminates the need for external sense resistors. Analog and digital control circuitry provide complete sequencing of the output drivers as well as providing brake, disable, and tachometer functions. A FAULT output flag indicates the presence of an under-voltage condition on the 12 V supply, excessive junction temperature, or an invalid Hall input combination. The A8925SEB's commutation logic is compatible with motors that have digital Hall effect sensors with 120° of electrical separation. Internal charge-pump circuitry is provided to drive the N-channel DMOS source drivers to their required gate voltages.

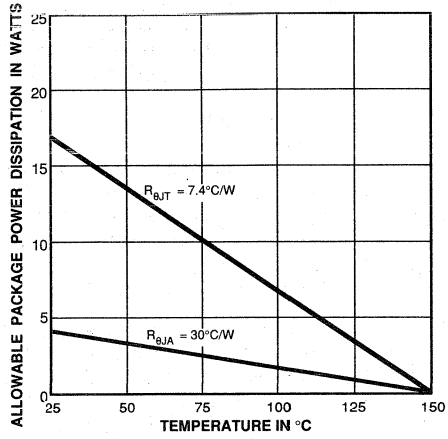
The A8925SEB is provided in a 44-lead PLCC power package for surface-mount applications. The copper batwing provides for maximum allowable package power dissipation in the smallest possible construction.

FEATURES

- DMOS Outputs
- Low $r_{DS(on)}$ - 0.25 Ω Maximum
- Linear Current Control
- Internal Commutation Circuitry
- Internal Current Sensing
- Thermal Shutdown Circuitry
- Under-Voltage Detection Circuitry
- Fault Output Flag
- Power Surface-Mount Package

Always order by complete part number: **A8925SEB** .

PRELIMINARY



Dwg. GP-020

ELECTRICAL CHARACTERISTICS AT T_A = +25°C, V_{CC} = V_{BB} = 12 V

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Logic Supply Voltage	V_{CC}	Operating	10	12	14	V
Load Supply Voltage	V_{BB}	Operating	10	12	14	V
Supply Current	I_{CC}	Operating	—	40	50	mA
		Standby, V_{ENABLE} = 0	—	2.0	4.0	mA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	20	—	°C
Output Drivers						
Output ON Resistance	$r_{DS(on)}$	I_{OUT} = 4.0 A, Pulse Test	—	0.20	0.25	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	I_{OUT} = 4.0 A, L = 2 mH	14	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 4.0 A	—	1.25	1.5	V
Output Switching Time	t_r	I_{OUT} = ±4.0 A, Resistive Load	—	12	—	µs
	t_f	I_{OUT} = ±4.0 A, Resistive Load	—	12	—	µs
Output Leakage Current	I_{DSX}	V_{OUT} = 14 V	—	100	300	µA
		V_{OUT} = 0 V	—	-100	-300	µA

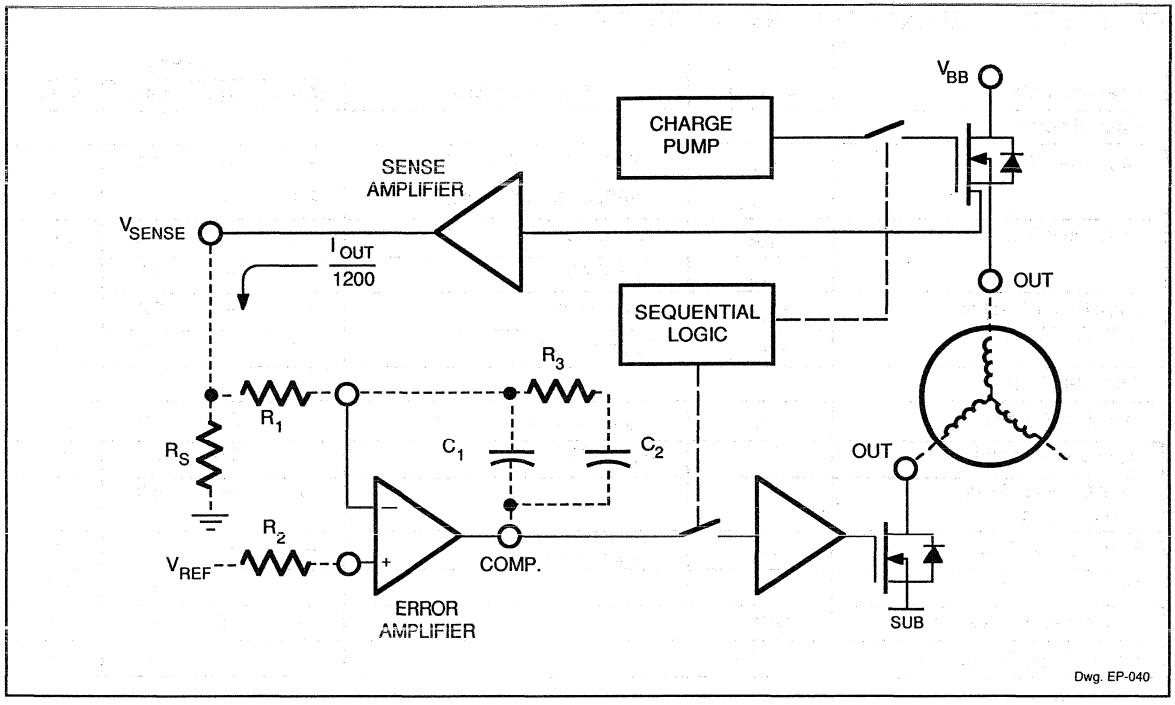
NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

Continued next page...

ELECTRICAL CHARACTERISTICS CONTINUED

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	ENABLE, BRAKE, POLE	—	—	0.8	V
	$V_{IN(1)}$	ENABLE, BRAKE, POLE	2.4	—	—	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0.8 V	—	—	-1.0	µA
	$I_{IN(1)}$	V_{IN} = 2.4 V	—	—	1.0	µA
Logic Output Voltage (FAULT, TACH)	$V_{OUT(0)}$	I_{OUT} = 4 mA	—	—	0.8	V
	$V_{OUT(1)}$	I_{OUT} = -100 µA	2.0	—	—	V
Error Amplifier						
Input Bias Current	I_B	$V_{IN(+)} - V_{IN(-)} = 0$	—	5.0	10	µA
Input Offset Voltage	V_{OS}	A_{VD} = 100	—	3.0	5.0	mV
Input Common-Mode Voltage Range	V_{IC}		0	—	6.0	V
Error Voltage Gain	A_{VD}	$V_{S\,OUT} / V_{S\,IN}$	—	80	—	dB
Unity Gain Bandwidth	BW		—	1.0	—	MHz
Common-Mode Rejection Ratio	CMRR		—	80	—	dB
Power Supply Rejection Ratio	PSRR		—	50	—	dB
Miscellaneous						
Current Sense Gain	A_{iCS}	I_{OUT} = 1.0 A	—	1/1200	—	—
Under-Voltage Trip Point	V_{CC}		8.0	—	9.5	V
Hall Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	-500	-1000	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	-250	-500	µA
Hall Input Threshold	V_{IN}		—	3.8	—	V
Hall Input Pull-Up Resistance	R_{PU}		15	20	25	kΩ

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.



FUNCTIONAL DESCRIPTION

Power Outputs (OUT_A, OUT_B, and OUT_C). The power outputs of the A8925SEB are DMOS transistors with a maximum $r_{DS(on)}$ of 0.25 Ω. Intrinsic ground clamp and flyback diodes clamp transient voltage spikes when switching inductive loads. Internal charge-pump circuitry is used to drive the gates of the N-channel source drivers to their required gate voltages.

Current Control. Current in the load is monitored by an internal sense amplifier that produces an output current that is approximately one twelve hundredth that of the load current (see Figure). This current is output to the V_{SENSE} terminal and develops a voltage across R_S that equals $R_S \cdot I_{LOAD}/1200$. This sense voltage (V_{SENSE}) is compared to a reference voltage (V_{REF}) and an error voltage is developed that is gated in by the sequential control logic to drive the gate of the appropriate output sink transistor. A transconductance control function is thus realized where $I_{OUT} = V_{REF} \cdot 1200/R_S$. External components C_1, C_2, R_1, R_2, and R_3 are compensation components used to obtain optimal response and settling of the current control loop. Information on how to select these components is available.

8925
3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH LINEAR CURRENT CONTROL AND POWER DMOS OUTPUTS

FAULT. The FAULT terminal when low indicates the presence of one of three fault conditions:

A) An under-voltage condition on the logic supply. The trip point for this function is between 8 and 9 volts.

B) An invalid Hall input combination ... all inputs High or all inputs Low.

C) An excessive device junction temperature. The thermal shut-down circuitry disables the output drivers in addition to forcing the FAULT output signal low.

TACH and POLE. In order to develop a low-jitter tachometer signal (TACH) for use in controlling motor speed the A8925SEB divides the frequency of the H_1 input by the number of poles in the motor. This eliminates the jitter caused by variations in Hall effect device placement, sensitivity, and magnet strengths by always changing state when looking at the same magnet/sensor pair. The resulting TACH signal changes state every mechanical revolution of the motor. The POLE input sets the TACH signal for four-pole motors when Low or eight-pole motors when High.

Hall Inputs (H_1, H_2, H_3). The A8925SEB is configured for use with open-collector Hall effect devices. Internal 20 kΩ pull-up resistors to 10 volts are connected to these inputs.

ENABLE. The ENABLE terminal when Low puts the device in a low current consumption, power-down mode. When ENABLE is High the device is active.

BRAKE. When the BRAKE input goes Low the output source drivers are disabled and the gates of the sink drivers are pulled high and left floating. This achieves optimum passive braking performance since the sink power DMOS output drivers are ON until the motor has fully completed braking. The braking control circuitry operates off the load supply (V_{BB}) to allow it to remain operational during power loss by using the back-EMF voltage of the motor as its supply.

LOAD SUPPLY (V_{BB}). This terminal is the power supply connection for the power output drivers and braking control circuitry. A series diode should be used to isolate this terminal from the logic supply (V_{CC}) to avoid clamping the motor's back-EMF voltage through the intrinsic ground clamp and flyback diodes during power loss. This terminal should be decoupled with a large-value capacitor to absorb load currents dumped back into the supply during the de-energization of motor windings. These currents can cause the supply voltage to exceed the maximum voltage rating of the device if not properly decoupled.

LOGIC SUPPLY (V_{CC}). This is the 12 volt supply terminal for the A8925SEB and powers all circuitry except the power outputs and brake control circuitry.

LOGIC GROUND. This must be connected to the power ground terminals in systems that do not use separate power and logic grounds.

POWER GROUND. Terminals 7 through 17 and 29 through 39 are webbed together and attach to the die mounting area to form a low thermal resistance path to allow heat to be conducted out of the device. The power dissipation of the package can be further enhanced by soldering these terminals to a large area of copper foil on the printed wiring board.

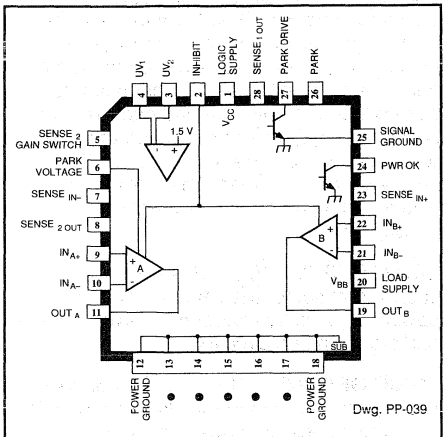
COMMUTATION TRUTH TABLE

Hall Sensor Inputs					Outputs		
H_1	H_2	H_3	BRAKE	FAULT	OUT_A	OUT_B	OUT_C
High	Low	High	High	High	High	Low	Z
High	Low	Low	High	High	High	Z	Low
High	High	Low	High	High	Z	High	Low
Low	High	Low	High	High	Low	High	Z
Low	High	High	High	High	Low	Z	High
Low	Low	High	High	High	Z	Low	High
High	High	High	High	Low	Z	Z	Z
Low	Low	Low	High	Low	Z	Z	Z
X	X	X	Low	X	Low	Low	Low

X = Irrelevant
Z = High Impedance

8931

VOICE COIL MOTOR DRIVER



Dwg. PP-039

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Supply Voltages, V_{BB} and V_{CC} ..... **16 V**
Output Current, I_{OUT} ..... **±1.0 A**
Park Drive Output Current, I_{PARK}
Continuous ..... **250 mA**
Peak ..... **1.0 A**
Amplifier Input Voltage Range,
V_{IN} ..... **-2.0 V to V_{CC}**
Sense Input Voltage Range,
$V_{SENSE\ IN}$ ..... **-0.3 V to V_{CC}**
Comparator and Digital Inputs,
V_{IN} ..... **-0.3 V to 10 V**
I_{IN} ..... **±10 mA**
Open Collector Outputs, V_{CEX} ..... **20 V**
I_C ..... **30 mA**
Output Clamp Diode Current,
I_F (pulsed) ..... **1.0 A**
Package Power Dissipation, P_D .. **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Junction Temperature, T_J ..... **150°C***
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Providing control and drive of the voice coil motor used for head positioning in disk drive applications, the A8931SEA is a full-bridge driver which can be configured so that its output current is a direct function of an externally applied control voltage or current. This linear current control function is supplemented by additional circuitry to protect the heads and the data disk during system failure or normal system shutdown.

The two ±800 mA driver outputs provide very-low saturation voltage drops and precise current control utilizing a single current-sensing resistor connected in series with the load. Under-voltage lockout disables the system in a controlled sequence if a fault condition occurs.

When activated by the under-voltage comparator, or a park command, the output power drivers change from a controlled current to a user-determined constant park voltage. Other features include a 4:1 transconductance gain switch for improved on-track performance, a power ok flag, an over-riding output disable to shut down both power amplifiers and reduce quiescent supply current, and internal thermal shutdown which disables the load (but still allowing the head to be parked) in the event of excessive junction temperature. The load is re-enabled when the junction temperature returns to a safe level.

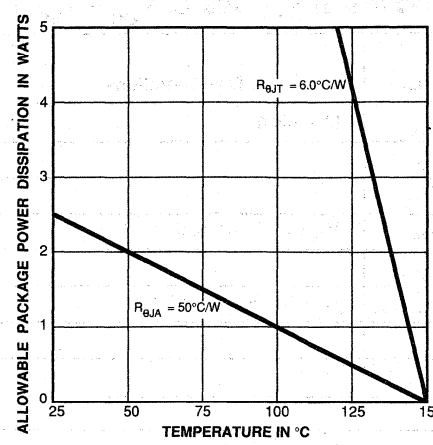
The A8931SEA is supplied in a 28-lead power PLCC for surface-mount applications. The copper half-batwing construction provides for maximum package power dissipation in a minimum package size. It is rated for continuous operation over the temperature range of -20°C to +85°C.

FEATURES

- Controlled-Velocity Head Parking
- 4 V to 15 V Operation
- Zero Deadband
- High Transconductance Bandwidth
- User-Adjustable Transconductance Gain
- 4:1 Digital Transconductance Gain Switch
- ±800 mA Load Current
- Dual Under-Voltage Monitors with Flag and User-Selectable Trip Points
- Internal Thermal Shutdown Circuitry

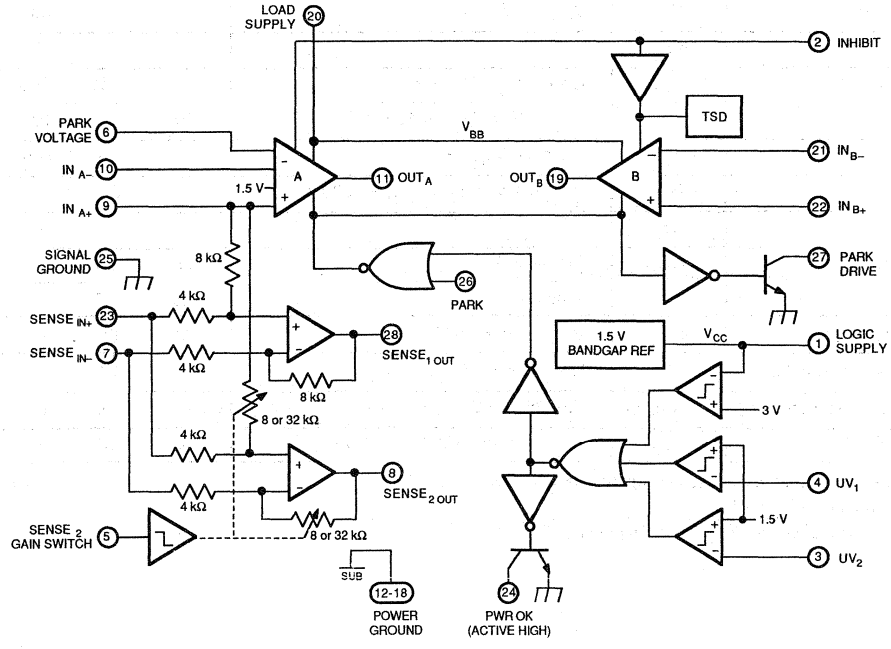
Always order by complete part number: **A8931SEA** .

PRELIMINARY



Dwg. GP-033

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-021

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{BB} = 12 V

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage Range	V_{CC}	Operating	3.0	12	16	V
Logic Supply UV Threshold	V_{CC}		—	2.8	3.0	V
Logic Supply UV Hysteresis	ΔV_{CC}		—	200	—	mV
Supply Current	I_{BB}	V_{OUT} = 6 V, no load	—	20	—	mA
	I_{CC}		—	1.0	—	mA
Output Disabled Supply Current	—	$I_{BB} + I_{CC}$, $V_{INHIBIT} \geq 1.7$ V	—	3.0	6.0	mA
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	8.0	—	°C
Power Amplifiers						
Output Saturation Voltage	V_{SAT}	I_{OUT} = 250 mA	—	250	—	mV
		I_{OUT} = 800 mA	—	450	—	mV
		i_{OUT} = -250 mA	—	750	—	mV
		I_{OUT} = -800 mA	—	950	—	mV
Total Saturation Voltage	V_{SAT}	I_{LOAD} = 250 mA	—	1.0	1.2	V
		I_{LOAD} = 800 mA	—	1.4	1.6	V
Input Offset Voltage	V_{IO}	V_{CM} = 6 V	—	—	8.0	mV
Input Offset Drift *	ΔV_{IO}		—	—	25	µV/°C
Input Bias Current	I_{IN}	Except IN_{A+}, V_{CM} = 6 V	—	-150	-500	nA
		IN_{A+} to $SENSE_{IN+}$ = 12 kΩ, T_J = 25°C	69	84	105	µA/V
Input Offset Current	I_{IO}	IN_B only, V_{CM} = 6 V	—	—	200	nA
Large Signal Gain	A_{VS}	V_{OUT} = 1 V to 11 V, I_{OUT} = ±500 mA	1.5	5.0	—	V/mV
Slew Rate	SR		—	1.0	—	V/µs
Unity Gain Bandwidth	BW	Amplifier A	0.5	2.0	—	MHz
		Amplifier B	0.5	1.0	—	MHz
Common-Mode Rejection	k_{CMR}	V_{CM} = 1 V to 10 V	70	90	—	dB
Clamp Diode Forward Voltage	V_F	I_F = 800 mA, $V_{INHIBIT} \geq 1.7$ V	—	1.0	1.2	V
High-Side Current Limit	I_{OUT}	T_J = 25°C	—	1.0	1.2	A
Power Supply Rejection	k_{SVR}	V_{CC} = 4 V to 15 V, V_{CM} = 1.5 V	70	90	—	dB

Negative current is defined as coming out of (sourcing) the specified device terminal.

Continued next page...

Typical Data is for design information only.

* This parameter, although guaranteed, is not tested in production.

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Current Sense Amplifiers						
Input Offset Voltage	V_{IO}	V_{CM} = 6 V	—	—	2.0	mV
Input Offset Drift	ΔV_{IO}	V_{CM} = 0 V to 12 V	—	—	1500	µV/V
		See *	—	—	8.0	µV/°C
GAIN SWITCH Threshold	V_{GS}		0.7	1.1	1.7	V
GAIN SWITCH Input Current	I_{GS}	V_{GS} = 1.7 V	—	—	100	µA
Voltage Gain	A_{VS1}	V_{ID} = -1 V to +1 V, V_{CM} = 6 V	1.95	2.00	2.05	—
	A_{VS2}	V_{ID} = -1 V to +1 V, V_{CM} = 6 V, V_{GS} = 0	1.95	2.00	2.05	—
		V_{ID} = -1 V to +1 V, V_{CM} = 6 V, V_{GS} = 1.7 V	7.8	8.0	8.2	—
Output Saturation Voltage	V_{SAT}	V_{OUT}, I_{OUT} = 1.5 mA	—	300	500	mV
		V_{CC} - V_{OUT}, I_{OUT} = -1.5 mA	—	400	700	mV
Park Function						
PARK DRIVE Leakage Current	I_{CEX}	V_{CEX} = 20 V	—	—	100	µA
PARK DRIVE Saturation Voltage	$V_{CE(SAT)}$	I_C = 200 mA	—	300	500	mV
PARK Input Threshold	V_{PARK}		0.7	1.1	1.7	V
PARK Input Current	I_{PARK}	V_{PARK} = 1.7 V	—	—	100	µA
PARK VOLTAGE Input Current	$I_{PARK\ V}$		—	-150	-500	nA
Under-Voltage Protection						
UV Threshold	V_{UV}	Low-to-High Trans., Other Input = 6 V	1.48	1.50	1.52	V
UV Threshold Hysteresis	ΔV_{UV}		15	25	40	mV
UV Input Current	I_{UV}	V_{UV} = 1 V	—	-0.5	-1.5	µA
PWR OK Saturation Voltage	$V_{CE(SAT)}$	I_C = 5 mA	—	—	450	mV
PWR OK Leakage Current	I_{CEX}	V_{CEX} = 20 V	—	—	5.0	µA
Inhibit Function						
INHIBIT Input Threshold	$V_{INHIBIT}$		0.7	1.1	1.7	V
INHIBIT Input Current	$I_{INHIBIT}$	$V_{INHIBIT}$ = 1.7 V	—	—	200	µA

Negative current is defined as coming out of (sourcing) the specified device terminal.

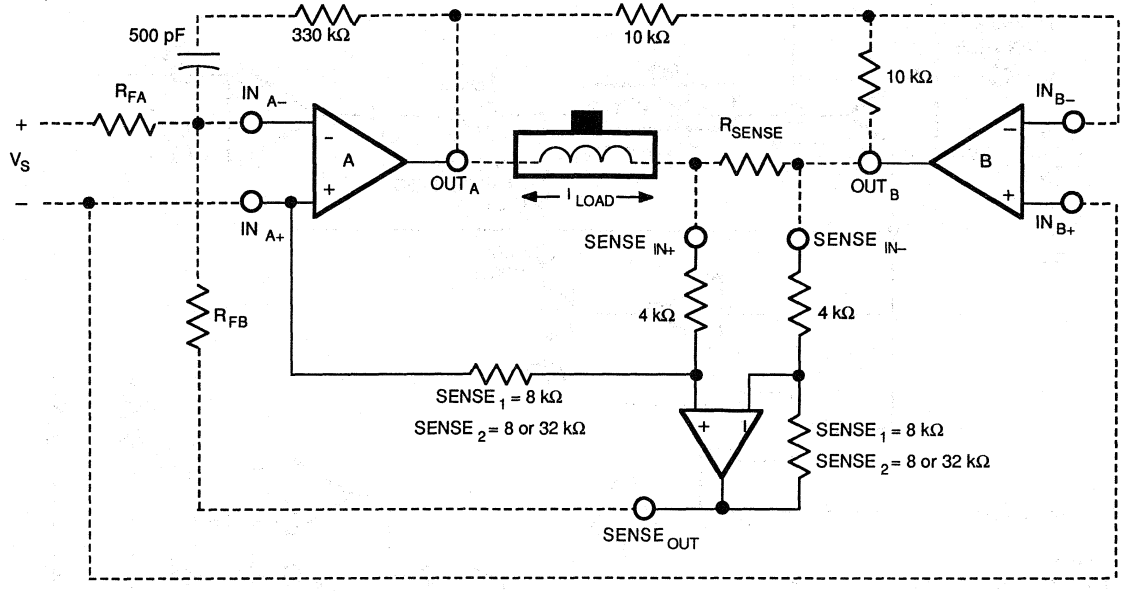
Typical Data is for design information only.

* This parameter, although guaranteed, is not tested in production.

TERMINAL FUNCTIONS

Terminal Number	Terminal Name	Function
1	LOGIC SUPPLY	V_{CC}; logic supply voltage in the range of +3 V to +16 V.
2	INHIBIT	An active-high input that inhibits the output stages without initiating a park.
3 and 4	UV_1 and UV_2	Under-voltage detection inputs. If not used, these terminals must be connected to the logic supply (V_{CC}).
5	$SENSE_2$ GAIN SWITCH	An active-high input that changes the gain of current sense error amplifier number 2 from 2 to 8 (typical).
6	PARK VOLTAGE	Auxiliary inverting input to power amplifier A.
7	$SENSE_{IN-}$	Inverting input to current sense error amplifers.
8	$SENSE_{2\ OUT}$	Output of current sense error amplifier number 2.
9	IN_{A+}	Non-inverting input to power amplifier A.
10	IN_{A-}	Inverting input to power amplifier A.
11	OUT_A	Power amplifier A output to voice coil motor.
12-18	POWER GROUND	High-level power ground and thermal heat sink.
19	OUT_B	Power amplifier B output to voice coil motor.
20	LOAD SUPPLY	V_{BB}; load supply voltage in the range of +3 V to +16 V.
21	IN_{B-}	Inverting input to power amplifier B.
22	IN_{B+}	Non-inverting input to power amplifier B.
23	$SENSE_{IN+}$	Non-inverting input to current sense error amplifiers.
24	PWR OK	A logic low at this output indicates an under-voltage condition.
25	SIGNAL GROUND	Low-level signal and logic ground; circuit reference.
26	PARK	An active-high logic input that activates the park function.
27	PARK DRIVE	Power transistor for retract current control on power down or park command.
28	$SENSE_{1\ OUT}$	Output of current sense error amplifier number 1.

CURRENT SENSING



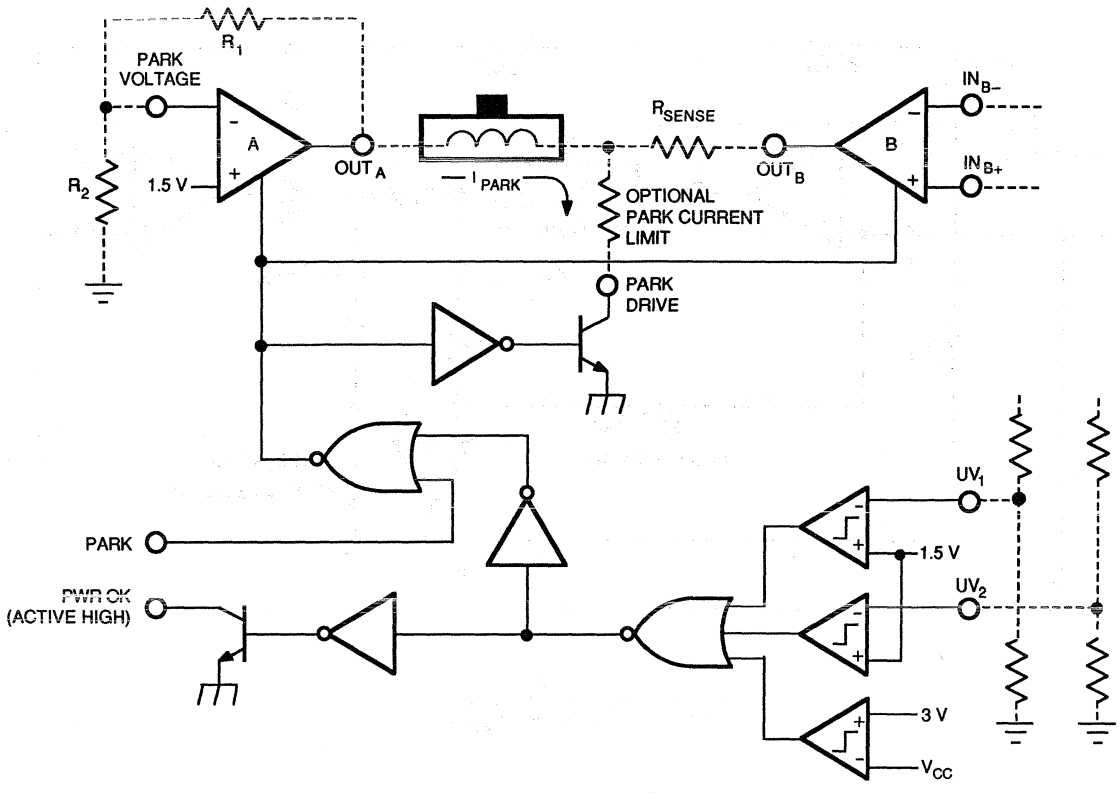
$$I_{LOAD} = g_m V_S = \frac{R_{FB} V_S}{R_{FA} A_{VS} R_{SENSE}}$$

Dwg. EP-034-1

where $A_{VS1} = 2$

$A_{VS2} = 2$ or 8

PARKING FUNCTION

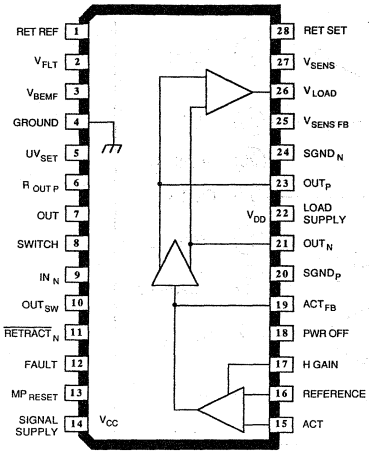


$$V_{OUT\ A} = \frac{1.5\ (R_1 + R_2)}{R_2}$$

Dwg. EP-039

8932

VOICE COIL MOTOR DRIVER



Dwg. PP-042

ABSOLUTE MAXIMUM RATINGS

Supply Voltages, V_{CC} and V_{DD} ..... **6.0 V**
Output Current, I_{OUT} (peak) ..... **±600 mA**
(continuous) ..... **±400 mA**
Analog Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{CC}**
Logic Input Voltage Range,
V_{IN} ..... **-0.3 V to +6.0 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **0°C to +70°C**
Junction Temperature, T_J ..... **+150°C†**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation the specified maximum junction temperature should not be exceeded.

Providing control and drive of the voice coil motor used for head positioning in 5 V disk drive applications, the A8932CLW is a full-bridge driver which can be configured so that its output current is a direct function of an externally applied control voltage or current. This linear current control function is supplemented by additional circuitry to protect the heads and the data disk during system failure or normal system shutdown.

The two ±500 mA MOS driver outputs provide very low saturation voltage and minimal power dissipation. Additional headroom is achieved by the sense-FET structure eliminating the need for an external current-sense resistor. Internal circuitry can be configured to provide closed-loop velocity control of the actuator by utilizing the generated back-EMF of the voice coil motor. Thermal protection and under-voltage lockout disables the system in a controlled sequence if a fault condition occurs.

The A8932CLW is supplied in a 28-lead SOIC for surface-mount applications.

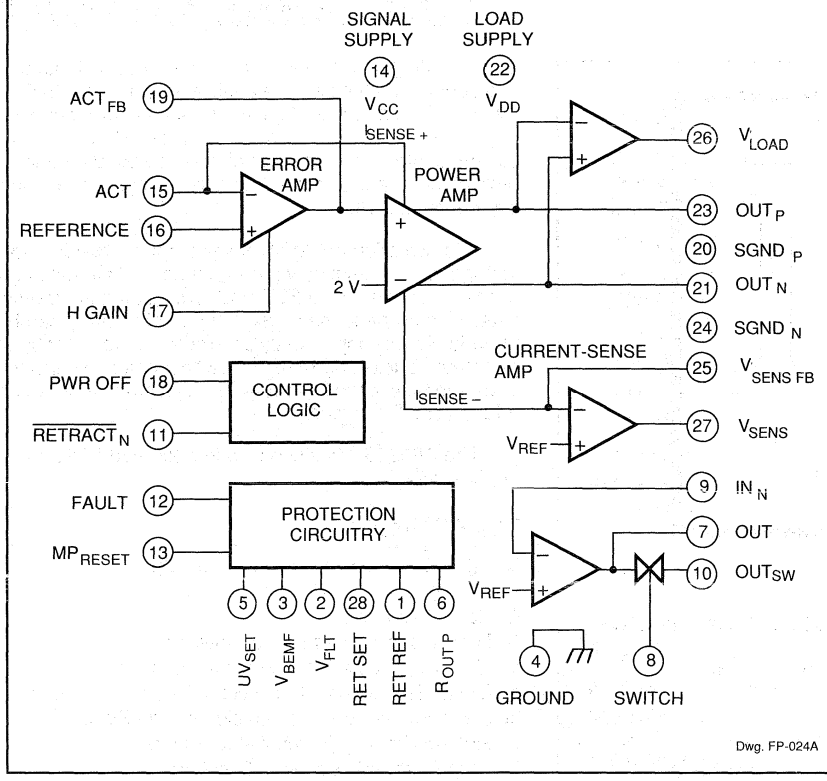
FEATURES

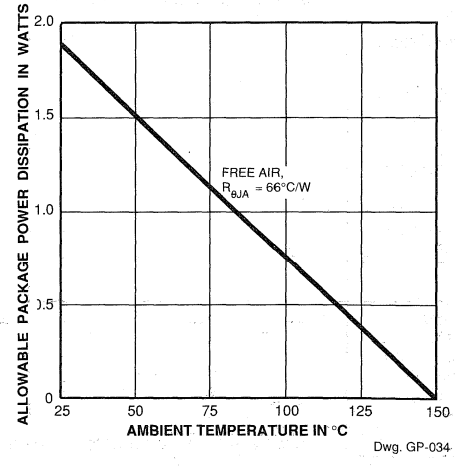
- Internal Back-EMF Velocity Loop Option
- Lossless Current Sensing
- Zero Deadband
- High Transconductance Bandwidth
- User-Adjustable Transconductance Gain
- Digital Transconductance Gain Switch (4:1 Ratio)
- 5 Volt Monitor with Selectable UV Trip Point
- Retract Circuitry Functional to 0 Volts
- Chip Enable/Sleep Mode Function
- 1 V at 500 mA Output Saturation Voltage
- Internal Thermal Shutdown Circuitry

Always order by complete part number: **A8932CLW** .

PRELIMINARY

FUNCTIONAL BLOCK DIAGRAM





ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{DD} = 4.5 V to 5.5 V, V_{REF} = 2.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Input Bias Current	I_{IB}		—	500	—	nA
Input Offset Voltage	V_{IO}		—	5.0	—	mV
Input Resistance	R_{IN}		—	100	—	Ω
Current Gain	A_i	H GAIN ≥ V_{CC}/2	—	6240	—	—
		H GAIN ≤ V_{CC}/2	—	1560	—	—
Reference Voltage Range	V_{REF}		0.5	—	3.0	V
Power Supply Rejection Ratio	k_{SVR}		—	60	—	dB
Output Saturation Voltage (Source + Sink)	$V_{DS(SAT)}$	I_{LOAD} = 100 mA	—	0.2	—	V
		I_{LOAD} = 500 mA	—	1.0	—	V
Retract Output Voltage	$V_{DS(SAT)}$	I_{OUT} ≤ 150 mA	—	0.5	—	V
Output Current	I_{OM}	Pulse Test, ±600 mA Limited	—	—	±500	mA
Gain Bandwidth	BW	-3 dB	—	100	—	kHz
Miscellaneous						
Under-Voltage Lockout Voltage	V_{CC}		4.24	4.30	4.38	V
Supply Current	I_{CC}	Outputs Balanced, No Load	—	—	10	mA
Logic Input Voltage	$V_{IN(0)}$		—	—	0.7	V
	$V_{IN(1)}$		3.5	—	—	V
Thermal Shutdown Temperature	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	20	—	°C

Negative current is defined as coming out of (sourcing) the specified device terminal.
Typical Data is for design information only.

TERMINAL FUNCTIONS

Term.	Terminal Name	Function
1	RET REF	The reference supply for setting the voltage across the load during retract.
2	V_{FLT}	Reservoir (energy storage) capacitor used to operate fault circuitry.
3	V_{BEMF}	Back-EMF voltage from spindle motor used to retract heads during loss of power.
4	GROUND	Circuit reference.
5	UV_{SET}	Under-voltage trip point reference input. Set internally to 4.3 V but may be overridden by external resistor divider. (Equation 6).
6	$R_{OUT\,P}$	Source driver used for retract; externally connected to OUT_P.
7	OUT	Output of uncommitted operational amplifier.
8	SWITCH	Logic input for transmission gate; a high level connects OUT to OUT_{SW}.
9	IN_N	Inverting input to uncommitted operational amplifier.
10	OUT_{SW}	Transmission-gated output of uncommitted operational amplifier.
11	$RETRACT_N$	An active-low logic input that initiates the retract sequence.
12	FAULT	A logic low at this MOS output indicates a thermal shutdown, under-voltage fault, or retract command.
13	MP_{RESET}	(Power-On Reset) A logic low at this open-collector output may be used to reset the system on under-voltage fault or power ON.
14	SIGNAL SUPPLY	V_{CC}; low-current supply voltage in the range of 4.5 V to 5.5 V.
15	ACT	Input which controls the current in the load. Transconductance gain is set with an external resistor in series with this input (Equation 1).
16	REFERENCE	V_{REF}; reference input for all amplifiers; ac ground.
17	H GAIN	Logic input to switch the error amplifier transconductance gain: LOW = 1560, HIGH = 6240.
18	PWR OFF	An active-high logic input that puts the device in a "sleep mode". All fault circuitry remains active.
19	ACT_{FB}	Input connection for feedback network which sets the error amplifier gain and bandwidth (Equations 2 and 3).
20	$SGND_P$	Power ground for the OUT_P sink driver.
21	OUT_N	Power output. Sinks current when $V_{ACT} < V_{REF}$.
22	LOAD SUPPLY	V_{DD}; high-current supply voltage for the voice-coil motor.
23	OUT_P	Power output. Sinks current when $V_{ACT} > V_{REF}$.
24	$SGND_N$	Power ground for the OUT_N sink driver.
25	$V_{SENS\,FB}$	Input connection for feedback network which sets the current-sense amplifier gain and bandwidth.
26	V_{LOAD}	An output voltage proportional to the load voltage. Used in conjunction with closed-loop velocity control.
27	V_{SENS}	Voltage output representing load current (Equation 4).
28	RET SET	An external resistor divider to set the retract voltage across the load. Used in conjunction with $V_{RET\text{-}REF}$ (Equation 5).

DEVICE DESCRIPTION

Current Amplifier. The A8932CLW voice coil motor driver features a wide transconductance bandwidth and no measurable crossover distortion. The transconductance gain is user selectable:

$$g_m = \frac{A_i}{R_{gm}} \qquad \text{(Equation 1)}$$

where A_i is either 1560 (H GAIN = Low) or 6240 (H GAIN = High)

The error amplifier's bandwidth and load compensation zero are set utilizing external resistor and capacitor feedback components around the amplifier.

$$R_Z = \frac{L_{LOAD}}{C_Z \times R_{LOAD}} \qquad \text{(Equation 2)}$$

$$C_Z = \frac{5.4}{A_i}\left(\frac{1}{2\pi \times f_{BW} \times R_{LOAD}}\right) \qquad \text{(Equation 3)}$$

with R_Z as above, and H GAIN = Low, the bandwidth is less than 100 kHz. With H GAIN = High, the bandwidth is reduced to less than 25 kHz.

Current and Voltage Sensing. The load current is sensed internally. Three auxiliary amplifiers are also included to allow various control functions to be implemented. The first of these amplifiers provides a voltage output that is proportional to the load current:

$$V_{SENSE} = \frac{R_S I_{LOAD}}{A_i} \qquad \text{(Equation 4)}$$

The second and third auxiliary amplifiers may be used in conjunction with the first to provide a closed-loop velocity control system for the actuator arm during a controlled retract for head parking. This is achieved by determining the back-EMF voltage generated by the voice coil and feeding back this information to the main actuator control input. The back-EMF feedback voltage can be switched in as required by means of the SWITCH logic input.

The back EMF-voltage represents the velocity of the actuator. By subtracting the $I_{LOAD}R_{LOAD}$ voltage component from the voltage across the load, the back-EMF term can be isolated and fed back to close a velocity control loop.

The amplifier output voltage V_{LOAD} is proportional to the voltage across the load ($0.4(V_{OUTN} - V_{OUTP})$). R_S is selected so that V_{SENSE} represents I_{LOAD} while R_3 is dependent on R_{LOAD} as shown in the following equations:

$$V_{LOAD} = -0.4\left((I_{LOAD}/R_{LOAD}) + V_{BEMF}\right)$$

$$V_{SENSE} = R_S\, I_{LOAD}\, A_i$$

where A_i = 1560 (H GAIN = logic Low)

$$OUT_{SW} = -V_{BEMF}\, R_1/R_2$$

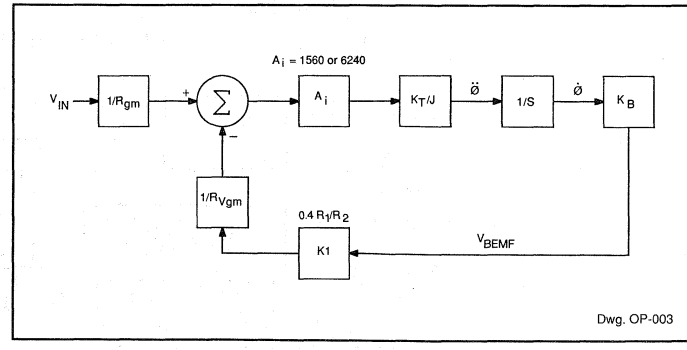
$$R3 = \frac{R_2\, R_S}{0.4\, A_i\, R_{LOAD}}$$

$$\frac{V_{BEMF}}{V_{IN}} = \frac{R_{gm}\, R_2}{R_{VGM}\, R_1}$$

$$BW = \frac{R_1\, K_B\, K_T\, A_i}{2\pi\, R_{VGM}\, R_2\, J}$$

where J is the moment of inertia, K_B is the back-emf motor constant, and K_T is the torque constant.

$$\text{Velocity loop compensation} = L_{LOAD}/R_{LOAD} = R_1\, C_1 = R_3\, C_2$$



Retract and Brake. A retract-brake sequence is initiated on receiving a fault indication from the internal thermal shutdown (TSD), or under-voltage lockout (UVLO), or an externally applied logic High at the RETRACT input.

If the velocity control scheme is implemented, the head can be retracted under the full control of INPUT in conjunction with OUT_{SW} back-EMF voltage if no fault condition exists. If a fault condition were to occur however, the retract velocity would be controlled by applying a constant user-defined voltage across the load:

$$V_{RET\text{-}REF} = \frac{0.58\ (R_7 + R_8)}{R_8} \qquad \text{(Equation 5)}$$

where $R_8 \geq 130\ k\Omega$.

When the sequence is operated, the output voltage is forced to approximately $V_{PARK\text{-}REF}$ to retract the heads, and then a fault command ("brake") is sent to the spindle motor driver. The user determines the total time for the retract sequence, before the spindle brake is enabled, by the choice of an external resistor and capacitor at the FAULT output.

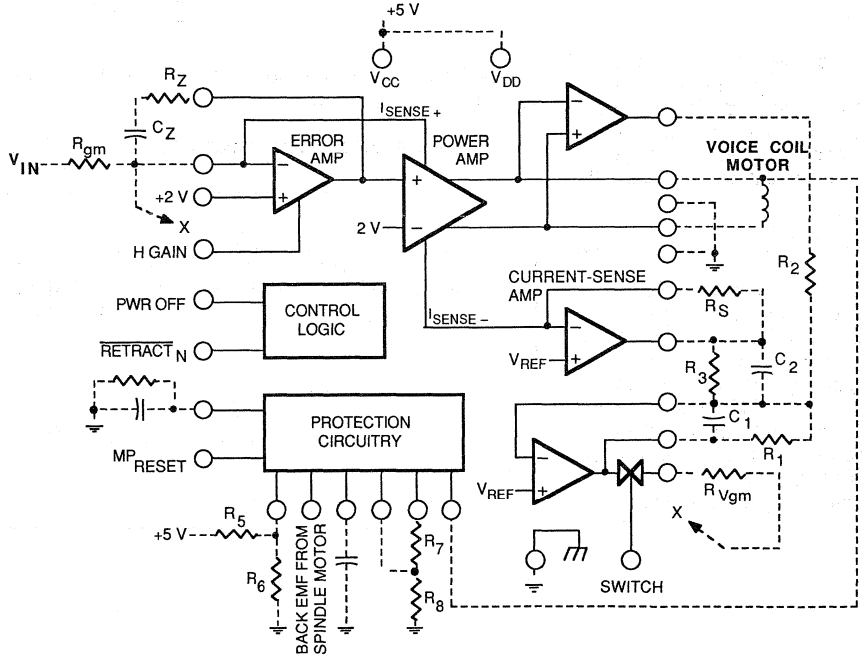
Power for the retract function is provided by the rectified back EMF of the spindle motor by way of the V_{BEMF} terminal. The A8932CLW will perform the retract function under low supply conditions (nominally down to 2 V). Operation down to almost 0 V requires an energy-storage capacitor at the V_{FLT} terminal.

Protective Features. The A8932CLW has a number of protective features incorporated into the design. Under-voltage lockout provides system protection in the event of reduced primary supply voltages. The under-voltage trip point is internally set at approximately 4.3 V. It can be user-defined with an external resistor voltage divider:

$$UV_{TRIP} = \frac{1.5\ (R_5 + R_6)}{R_6} \qquad \text{(Equation 6)}$$

Thermal shutdown circuitry is included to protect the device from excessive junction temperature. It is only intended to protect the chip from catastrophic failures due to excessive junction temperature.

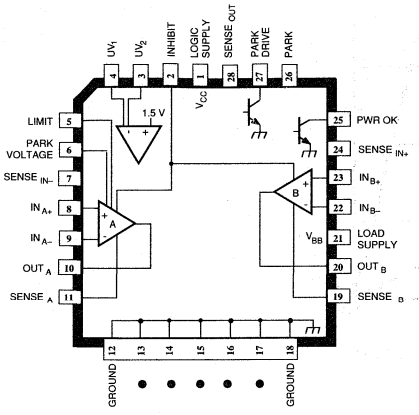
TEST CIRCUIT AND TYPICAL APPLICATION



Dwg. EP-041A

8958

VOICE COIL MOTOR DRIVER



Dwg. PP-038

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Supply Voltages, V_{BB} and V_{CC} ..... **16 V**
Output Current, I_{OUT} ..... **±1.0 A**
Park Drive Output Current, I_{PARK}
Continuous ..... **250 mA**
Peak ..... **1.0 A**
Amplifier Input Voltage Range,
V_{IN} ..... **-2.0 V to V_{CC}**
Sense Input Voltage Range,
$V_{SENSE\ IN}$ ..... **-0.3 V to V_{CC}**
Comparator and Digital Inputs,
V_{IN} ..... **-0.3 V to 10 V**
I_{IN} ..... **±10 mA**
Power OK Output, V_{CEX} ..... **20 V**
I_C ..... **30 mA**
Output Clamp Diode Current,
I_F (pulsed) ..... **1.0 A**
Package Power Dissipation, P_D ... **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Junction Temperature, T_J ..... **150°C***
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Providing control and drive of the voice coil motor used for head positioning in disk drive applications, the A8958SEA is a full-bridge driver which can be configured so that its output current is a direct function of an externally applied control voltage or current. This linear current control function is supplemented by additional circuitry to protect the heads and the data disk during system failure or normal system shutdown.

The two ±800 mA driver outputs provide very-low saturation voltage drops and precise current control utilizing a single current-sensing resistor connected in series with the load. Under-voltage lockout disables the system in a controlled sequence if a fault condition occurs.

When activated by the under-voltage comparator, or a park command, the output power drivers change from a controlled current to a user-determined constant park voltage. Other features include a power ok flag, a limit input to force the outputs to their maximum level in either polarity, an over-riding output disable to shut down both power amplifiers and reduce quiescent supply current, and internal thermal shutdown which disables the load (but still allowing the head to be parked) in the event of excessive junction temperatures. The load is re-enabled when the junction temperature returns to a safe level.

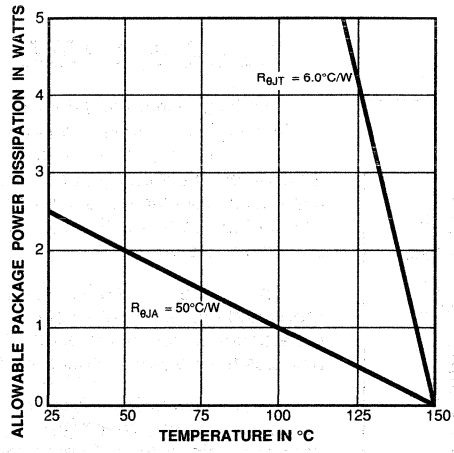
The A8958SEA is supplied in a 28-lead power PLCC for surface-mount applications. The copper half-batwing construction provides for maximum package power dissipation in a minimum package size. It is rated for continuous operation over the temperature range of -20°C to +85°C.

FEATURES

- Controlled-Velocity Head Parking
- 4 V to 15 V Operation
- Zero Deadband
- High Transconductance Bandwidth
- User-Adjustable Transconductance Gain
- ±800 mA Load Current
- Dual Under-Voltage Monitors with Flag and User-Selectable Trip Points
- Internal Thermal Shutdown Circuitry
- Replaces UC3175

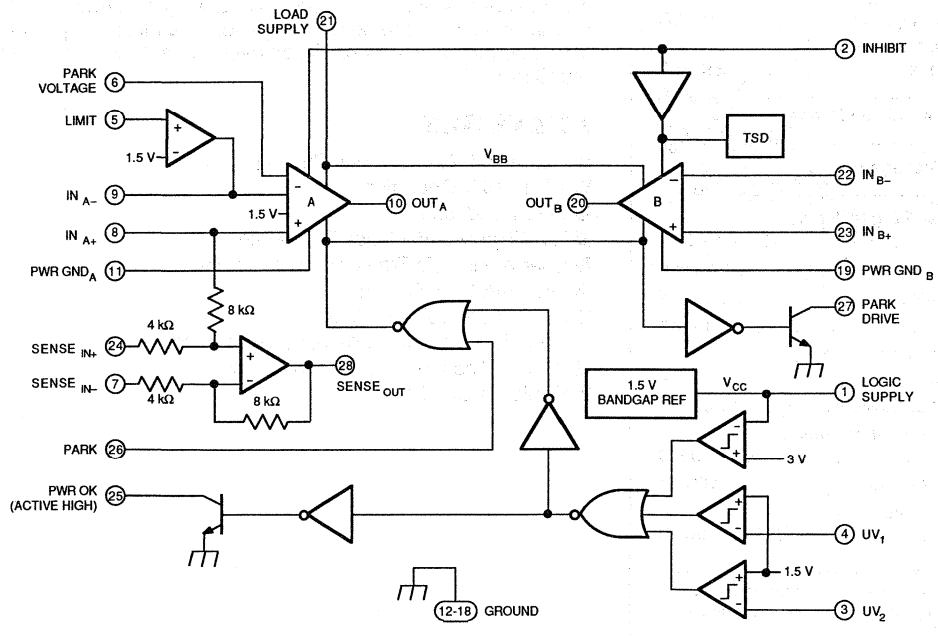
Always order by complete part number: **A8958SEA** .

PRELIMINARY



Dwg. GP-033

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-020A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{BB} = 12 V

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage Range	V_{CC}	Operating	3.0	12	16	V
Logic Supply UV Threshold	V_{CC}		—	2.8	3.0	V
Logic Supply UV Hysteresis	ΔV_{CC}		—	200	—	mV
Supply Current	I_{BB}	V_{OUT} = 6 V, no load	—	20	—	mA
	I_{CC}		—	1.0	—	mA
Inhibited Supply Current	—	$I_{BB} + I_{CC}$, $V_{INHIBIT} \geq 1.7$ V	—	3.0	6.0	mA
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	8.0	—	°C
Output Power Drivers						
Output Saturation Voltage	V_{SAT}	I_{OUT} = 250 mA	—	250	—	mV
		I_{OUT} = 800 mA	—	450	—	mV
		I_{OUT} = -250 mA	—	750	—	mV
		I_{OUT} = -800 mA	—	950	—	mV
Total Saturation Voltage (Source + Sink)	V_{SAT}	I_{LOAD} = 250 mA	—	1.0	1.2	V
		I_{LOAD} = 800 mA	—	1.4	1.6	V
Input Offset Voltage	V_{IO}	V_{CM} = 6 V	—	—	8.0	mV
Input Offset Drift *	ΔV_{IO}		—	—	25	µV/°C
Input Bias Current	I_{IN}	Except IN_{A+}, V_{CM} = 6 V	—	-150	-500	nA
		IN_{A+} to $SENSE_{IN+}$ = 12 kΩ, T_J = 25°C	69	84	105	µA/V
Input Offset Current	I_{IO}	IN_B only, V_{CM} = 6 V	—	—	200	nA
Large Signal Gain	A_{VS}	V_{OUT} = 1 V to 11 V, I_{OUT} = ±500 mA	1.5	5.0	—	V/mV
Slew Rate	SR		—	1.0	—	V/µs
Unity Gain Bandwidth	BW	Amplifier A	0.5	2.0	—	MHz
		Amplifier B	0.5	1.0	—	MHz
Common-Mode Rejection	k_{CMR}	V_{CM} = 1 V to 10 V	70	90	—	dB
Clamp Diode Forward Voltage	V_F	I_F = 800 mA; $V_{INHIBIT} \geq 1.7$ V	—	1.0	1.2	V
High-Side Current Limit	I_{OUT}	T_J = 25°C	—	1.0	1.2	A
Power Supply Rejection	k_{SVR}	V_{CC} = 4 V to 15 V, V_{CM} = 1.5 V	70	90	—	dB

Negative current is defined as coming out of (sourcing) the specified device terminal.

Continued next page...

Typical Data is for design information only.

* This parameter, although guaranteed, is not tested in production.

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Current Sense Amplifier						
Input Offset Voltage	V_{IO}	V_{CM} = 6 V	—	—	2.0	mV
Input Offset Drift	ΔV_{IO}	V_{CM} = 0 V to 12 V	—	—	1500	µV/V
		See *	—	—	8.0	µV/°C
Voltage Gain	A_{VS}	V_{ID} = -1 V to +1 V, V_{CM} = 6 V	1.95	2.00	2.05	—
Output Saturation Voltage	V_{SAT}	V_{OUT}, I_{OUT} = 1.5 mA	—	300	500	mV
		V_{CC} - V_{OUT}, I_{OUT} = -1.5 mA	—	400	700	mV
Park Function						
PARK DRIVE Leakage Current	I_{CEX}	V_{CEX} = 20 V	—	—	100	µA
PARK DRIVE Saturation Voltage	$V_{CE(SAT)}$	I_C = 200 mA	—	300	500	mV
PARK Input Threshold	V_{PARK}		0.7	1.1	1.7	V
PARK Input Current	I_{PARK}	V_{PARK} = 1.7 V	—	—	100	µA
PARK VOLTAGE Input Current	$I_{PARK\,V}$		—	-150	-500	nA
Under-Voltage Protection						
UV Threshold	V_{UV}	Low-to-High Trans., Other Input = 6 V	1.48	1.50	1.52	V
UV Threshold Hysteresis	ΔV_{UV}		15	25	40	mV
UV Input Current	I_{UV}	V_{UV} = 1 V	—	-0.5	-1.5	µA
PWR OK Saturation Voltage	$V_{CE(SAT)}$	I_C = 5 mA	—	—	450	mV
PWR OK Leakage Current	I_{CEX}	V_{CEX} = 20 V	—	—	5.0	µA
Auxiliary Functions						
LIMIT Input Voltage	$V_{LIMIT(L)}$	OUT_A forced Low	0.7	0.8	—	V
	$V_{LIMIT(H)}$	OUT_A forced High	—	2.2	2.3	V
	V_{LIMIT}	Limit inactive	1.2	—	1.8	V
		Open circuit	1.45	1.50	1.55	V
LIMIT Input Resistance	R_{LIMIT}	V_{LIMIT} = 1.2 V to 1.8 V	—	10	—	kΩ
INHIBIT Input Threshold	$V_{INHIBIT}$		0.7	1.1	1.7	V
INHIBIT Input Current	$I_{INHIBIT}$	$V_{INHIBIT}$ = 1.7 V	—	—	200	µA

Negative current is defined as coming out of (sourcing) the specified device terminal.

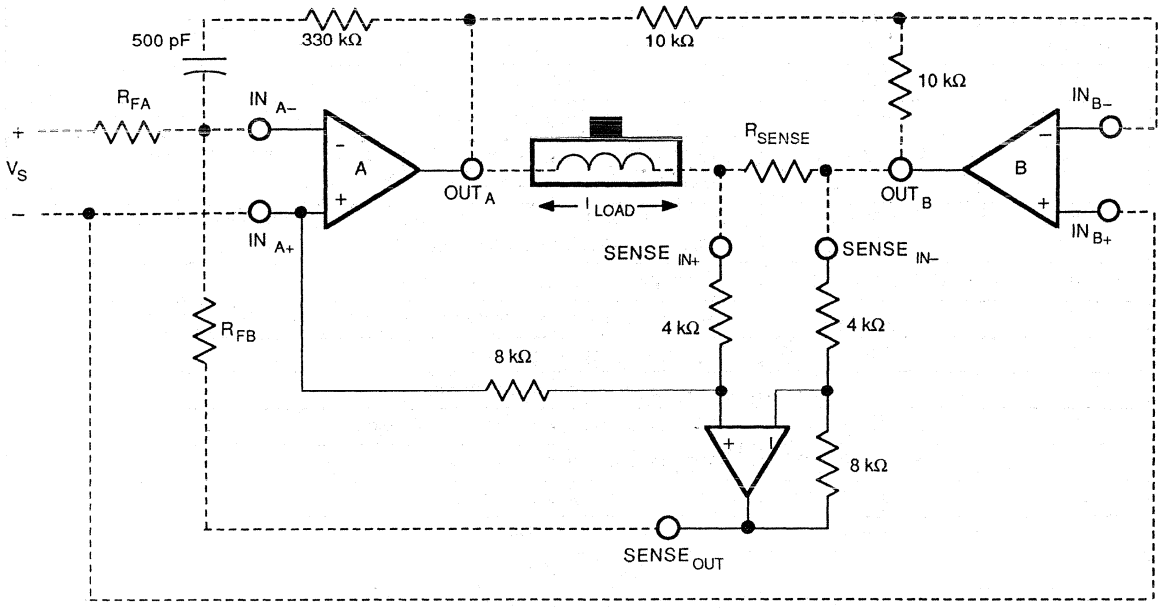
Typical Data is for design information only.

* This parameter, although guaranteed, is not tested in production.

TERMINAL FUNCTIONS

Terminal Number	Terminal Name	Function
1	LOGIC SUPPLY	V_{CC}; logic supply voltage in the range of +3 V to +16 V.
2	INHIBIT	An active-high logic input that inhibits the output stages without initiating a park.
3 and 4	UV_1 and UV_2	Under-voltage detection inputs. If not used, these terminals must be connected to the logic supply (V_{CC}).
5	LIMIT	A tri-state input that forces the output of amplifier A into saturation in either direction, or allows normal linear operation.
6	PARK VOLTAGE	Auxiliary inverting input to power amplifier A.
7	$SENSE_{IN-}$	Inverting input to current sense error amplifer.
8	IN_{A+}	Non-inverting input to power amplifier A.
9	IN_{A-}	Inverting input to power amplifier A.
10	OUT_A	Power amplifier A output to voice coil motor.
11	$PWR\ GND_A$	Power ground of amplifier A.
12-18	GROUND	Circuit reference and thermal heat sink.
19	$PWR\ GND_B$	Power ground of amplifier B.
20	OUT_B	Power amplifier B output to voice coil motor.
21	LOAD SUPPLY	V_{BB}; load supply voltage in the range of +3 V to +16 V.
22	IN_{B-}	Inverting input to power amplifier B.
23	IN_{B+}	Non-inverting input to power amplifier B.
24	$SENSE_{IN+}$	Non-inverting input to current sense error amplifer.
25	PWR OK	A logic low at this output indicates an under-voltage condition.
26	PARK	An active-high logic input that activates the park function.
27	PARK DRIVE	Power transistor for retract current control on power down or park command.
28	$SENSE_{OUT}$	Output of current sense error amplifier.

CURRENT SENSING

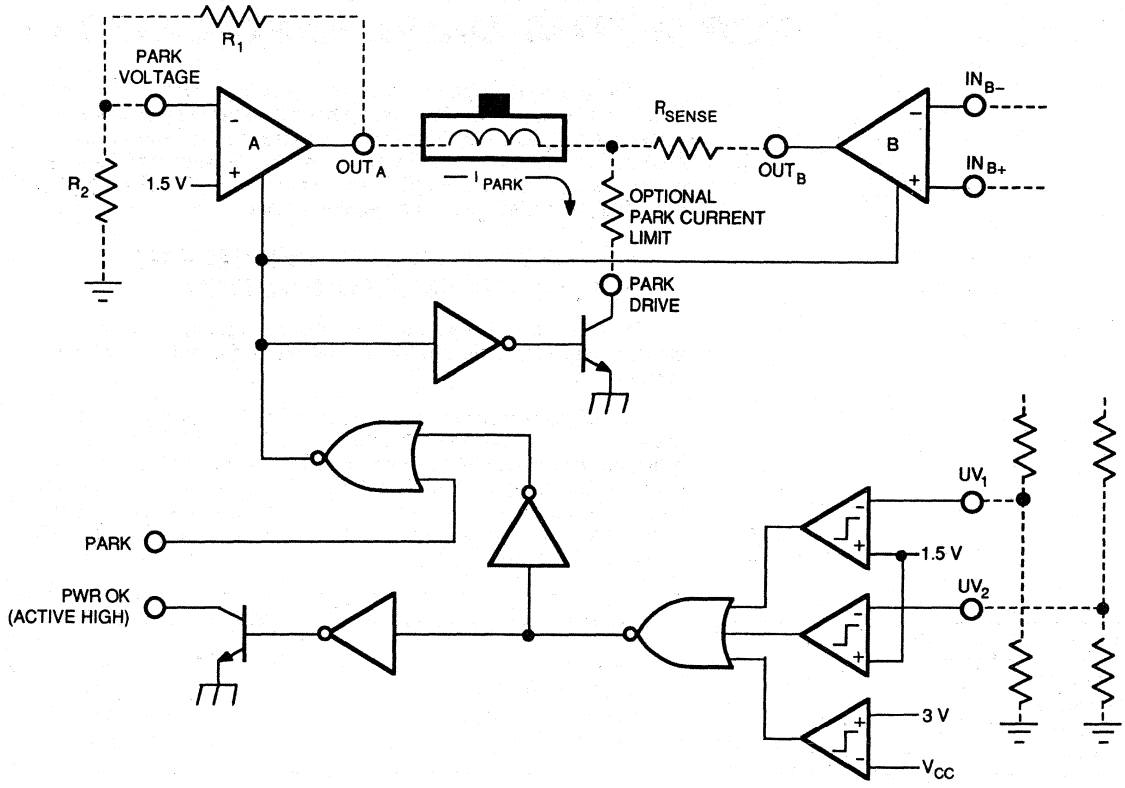


$$I_{LOAD} = g_m V_S = \frac{R_{FB} V_S}{R_{FA} A_{VS} R_{SENSE}}$$

Dwg. EP-034

where $A_{VS} = 2$

PARKING FUNCTION



$$V_{OUT\ A} = \frac{1.5\ (R_1 + R_2)}{R_2}$$

Dwg. EP-039

APPLICATIONS INFORMATION

POWER INTEGRATED CIRCUITS FOR MOTOR-DRIVE APPLICATIONS

Improved systems performance and reliability, lower component counts, and reduced cost are among benefits offered by space-saving power interface ICs. Many of the following devices are specifically designed for motor-drive applications. The development of these devices is especially significant in view of the increasing use of microprocessor-controlled servo and stepper motors.

UNIPOLAR STEPPER-MOTOR TRANSLATOR/DRIVER

The UCN5804B integrated circuit drives permanent magnet stepper motors rated to 1.25 A and 35 V with a minimum of external components.

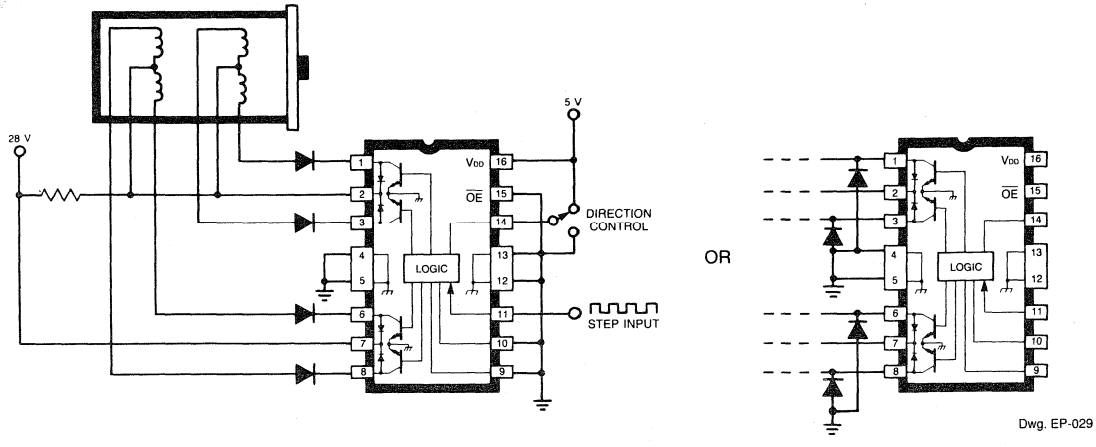
Internal step logic activates one or two of the four output sink drivers to step the load from one position to the next. The logic is activated when STEP INPUT (pin 11) is allowed to go HIGH. Single-phase (A-B-C-D), two-phase (DA-AB-BC-CD), or half-step (A-AB-B-BC-C-CD-D-DA) operation, and step-inhibit are selected by connections at pins 9 and 10. The sequence of states is determined by the DIRECTION CONTROL (pin 14).

Drive Format	Pin 9	Pin 10
Two-Phase	L	L
One-Phase	H	L
Half-Step	L	H
Step-Inhibit	H	H

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Output Voltage, V_{OUT}	**35 V**
Output Current, I_{OUT}	**1.25 A**
Logic Supply Voltage, V_{CC}	**4.5 V to 5.5 V**
Input Voltage, V_{IN}	**5.5 V**

L/R STEPPER-MOTOR DRIVE



Dwg. EP-029

FULL-BRIDGE MOTOR DRIVERS

The UDN2953B and UDN2954W are designed for bidirectional, chopped-mode current control of dc motors with peak start-up currents as high as 3.5 A. The output-current limit is determined by the user's selection of a sensing resistor. The pulse duration is set by an external RC timing network. The chopped mode of operation is characterized by low power-dissipation levels and maximum efficiency.

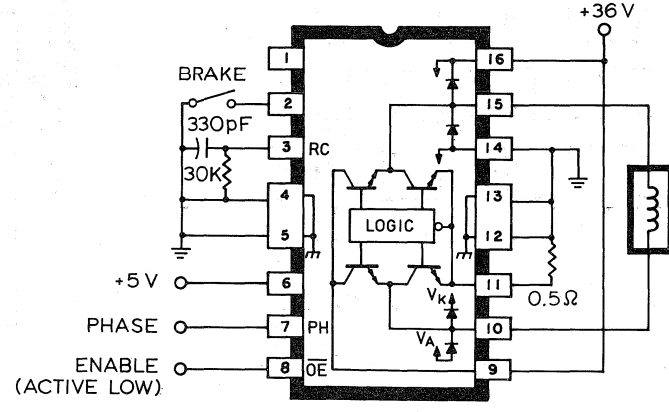
Internal circuit protection includes thermal shutdown with hysteresis, output transient-suppression diodes, and crossover current protection.

The UDN2953B is supplied in a 16-pin DIP with heat-sink contact tabs. The UDN2954W, with increased allowable package power dissipation, is supplied in a 12-lead single in-line power tab package. In both case styles, the heat sink is at ground potential and needs no insulation.

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Motor Supply Voltage, V_{BB}	**7.5 V to 50 V**
Continuous Output Current, I_{OUT}	**±2.0 A**
Peak Output Current, I_{OP}	**±3.5 A**
Logic Supply Voltage, V_{CC}	**4.5 V to 5.5 V**
Input Voltage, V_{IN}	**24 V**

UDN2953B



Dwg. No. A-12,649B

QUAD DARLINGTON SWITCHES

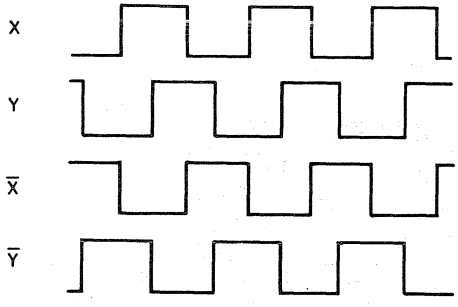
The UDN2878W and UDN2879W drive motor windings at up to 200 watts per channel. The integrated circuits include transient-suppression diodes and input logic that is compatible with most TTL, LS TTL, and 5 V CMOS. The 12-pin single in-line power-tab package allows maximum power-handling capability.

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Load Voltage, V_{CC} (UDN2878W)	**35 V**
(UDN2879W)	**50 V**
Continuous Output Current, I_C	**4 A**
Peak Output Current, I_{CP}	**5 A**
Logic Supply Voltage Range, V_S	**4.5 V to 7.0 V**
Input Voltage, V_{IN}	**V_S**

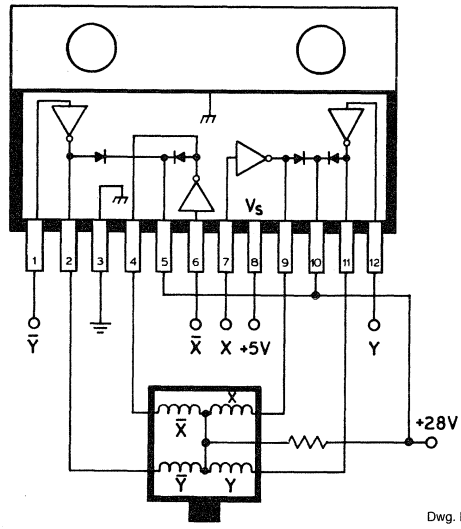
STEPPER-MOTOR DRIVE

2-PHASE, UNIPOLAR INPUT WAVEFORMS



Dwg. No. A-11,795

UDN2878W



Dwg. No. A-11,975

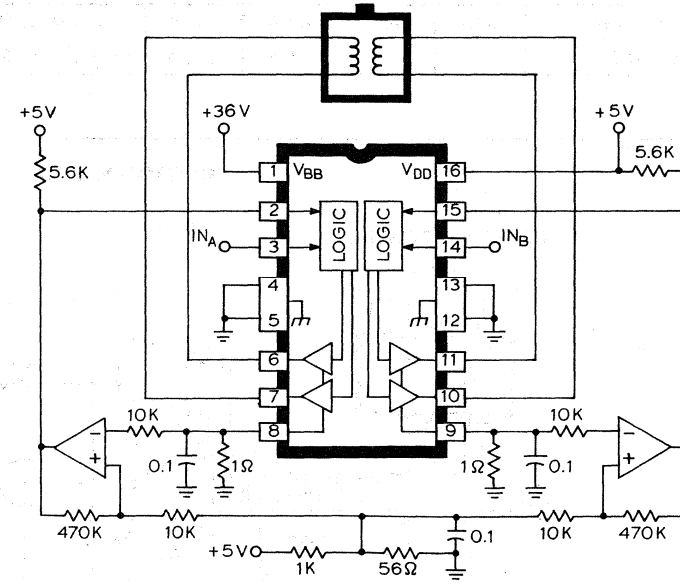
DUAL FULL-BRIDGE MOTOR DRIVER

The UDN2993B motor driver contains two independent full-bridges capable of operating with load currents of up to 600 mA. An internally generated deadtime prevents potentially destructive crossover currents when changing load phase. Internal transient-suppression diodes are included for use with inductive loads. Emitter outputs allow for current sensing in pulse-width modulated applications.

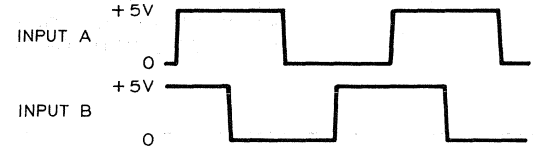
RECOMMENDED MAXIMUM OPERATING CONDITIONS

Load Voltage Range, V_{BB} . . . . . **10 V to 40 V**
Output Current, I_{OUT} . . . . . **±500 mA**
Logic Voltage Range, V_{DD} . . . . . **4.5 V to 5.5 V**

2-PHASE BIPOLAR STEPPER-MOTOR DRIVE
(Pulse-Width Modulated)



Dwg. No. A-12,453



Dwg. No. A-12,454

INTEGRATED CIRCUITS
FOR MOTOR-DRIVE APPLICATIONS

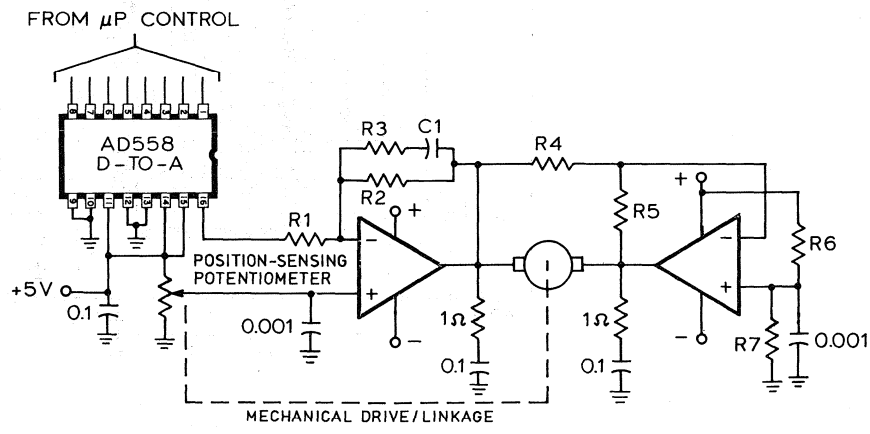
LINEAR MOTOR DRIVERS

Power operational amplifiers are useful in driving voice-coil motors, linear servo motors, and ac and dc motors in a linear mode where motor speed or position is a direct function of a linear input signal. The operational amplifiers listed here are standard "building block" circuits providing almost unlimited application. The high-gain, high-impedance operational amplifier configuration allows many specialized input, output, and feedback arrangements.

All devices feature high output voltage swings, high input common mode range, high PSRR and CMRR. The unity-gain stable versions need no external compensation. Internal thermal shutdown circuitry protects these devices against output overloads. The dual amplifiers include programmable output current-sensing capability.

PART NUMBER	TYPE	MAX. ΔV_S	CONT. I_{OUT}	PEAK I_{OP}	FEATURES	PACKAGE
ULN3751Z	Single	28 V	±2.5 A	3.5 A	Unity-Gain Stable Internal Compensation	5-Lead SIP
ULN3755W	Dual	40 V	±2.5 A	±3.5 A	Bootstrapped Output, Unity-Gain Stable,	12-Lead SIP
ULN3755B			±2.5 A	±3.5 A	Prog. Current Sense	16-Pin DIP

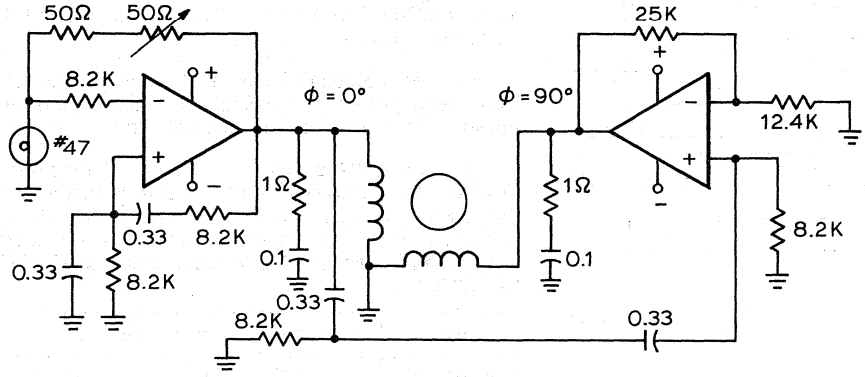
POSITION SERVO



R4 = R5 = R6 = R7
R1, R2 DEFINE D-C GAIN
R3, C1 SELECTED FOR LOOP COMP.

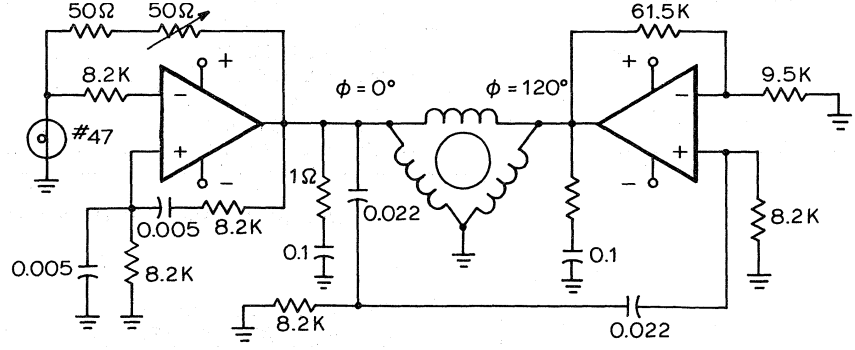
Dwg. No. A-12,652

TWO-PHASE, 60 Hz OSCILLATOR/MOTOR DRIVER



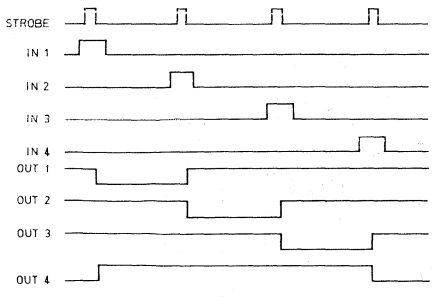
Dwg. No. A-12,651

THREE-PHASE, 400 Hz OSCILLATOR/MOTOR DRIVER



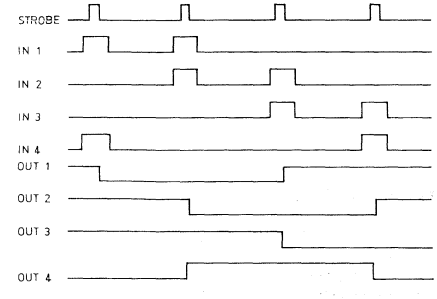
Dwg. No. A-12,650

UNIPOLAR WAVE DRIVE



Dwg. No. A-11,446

UNIPOLAR 2-PHASE DRIVE



Dwg. No. A-11,447

BiMOS UNIPOLAR MOTOR DRIVERS

Driving unipolar motors is one of many successful applications for the UCN5800A, UCN5801A, UCN5830B, andUCN5831B BiMOS II latched sink drivers.

All devices contain CMOS data latches, CMOS control circuitry, high-voltage, high-current bipolar Darlington outputs, and output transient protection diodes for use with inductive loads.

The UCN5800A is a direct replacement for the original UCN4401A. The UCN5801A replaces the UCN4801A. With a 5 V supply, BiMOS II devices typically operate at data input rates above 5 MHz; at 12 V, significantly higher speeds are obtainable. BiMOS III drivers, with output voltage ratings to 150 V, are available as UCN5900A and UCN5901A.

Device	Package	Drivers	Features
UCN5800A	14-pin DIP	4	Clear, Strobe, Output Enable
UCN5801A	22-pin DIP	8	Clear, Strobe, Output Enable
UCN5830B	16-pin DIP	4	Strobe and Output Enable
UCN5831B	16-pin DIP	4	Strobe, Output Enable, Saturated Outputs

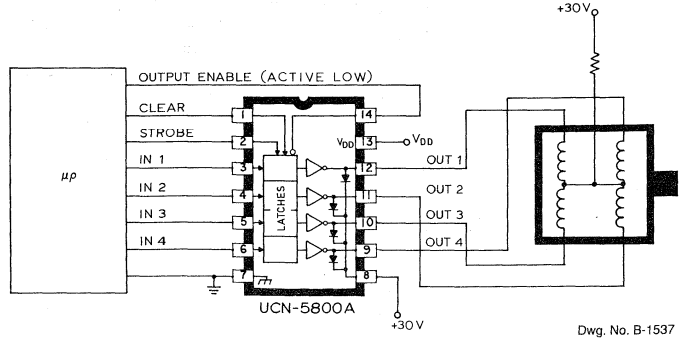
RECOMMENDED MAXIMUM OPERATING CONDITIONS

Output Voltage, V_{OUT}
- UCN5800A & UCN5801A . . . . . **35 V**
- UCN5830B & UCN5831B . . . . . **35 V**

Continuous Output Current, I_{OUT}
- UCN5800A & UCN5801A . . . . . **350 mA**
- UCN5830B & UCN5831B . . . . . **1.0 A**

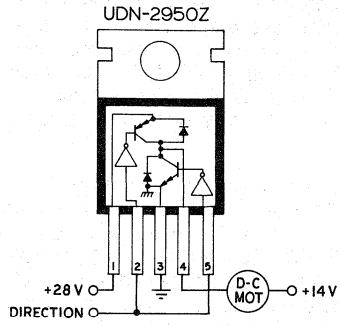
Logic Supply Voltage, V_{DD}
- UCN5800A & UCN5801A . . . . . **4.5 V to 12 V**
- UCN5830B & UCN5831B . . . . . **4.5 V to 5.5 V**

UNIPOLAR STEPPER-MOTOR DRIVE



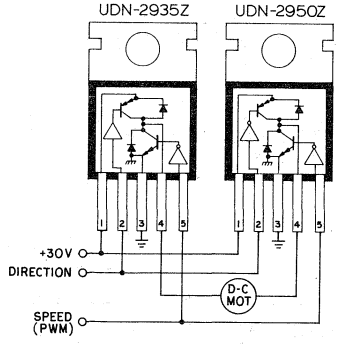
Dwg. No. B-1537

SINGLE-WINDING DC OR STEPPER-MOTOR DRIVE



Dwg. No. A-12,114

FULL-BRIDGE DC SERVO-MOTOR DRIVE



Dwg. No. A-12,115

HIGH-CURRENT BIPOLAR HALF-BRIDGE MOTOR DRIVERS

The UDN2935Z and UDN2950Z ICs are monolithic half-bridge motor drivers in power tab TO-220 style packages. The circuits combine sink and source drivers with diode protection, gain and level shifting systems, and a voltage regulator for single-supply operation. They are designed for servo-motor drive applications using pulse-width modulation.

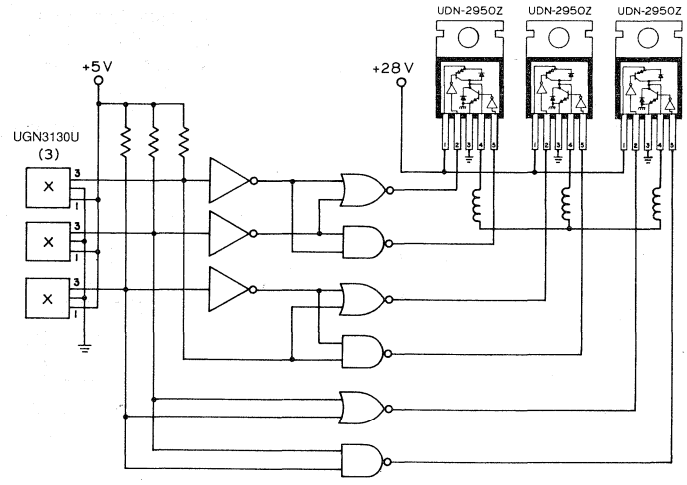
The PWM drive mode is characterized by minimal power dissipation requirements and allows the output to switch currents of 2 amperes. Output dc current accuracies of better than 10% at 100 kHz can be obtained.

The UDN2935Z and UDN2950Z may be used in pairs (full-bridge) to drive dc stepper motors or brushless dc motors.

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Supply Voltage, V_S	**8.0 V to 35 V**
Continuous Output Current, I_{OUT}	**±2.0 A**
Peak Output Current, I_{OP}	**±3.5 A**
Input Voltage, V_{IN}	**5.5 V**

3-PHASE BRUSHLESS DC MOTOR CONTROL

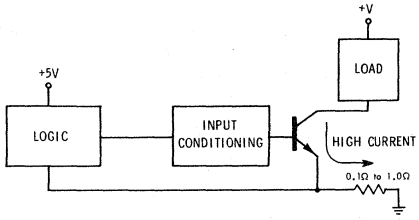


Dwg. No. A-12,653

APPLICATIONS INFORMATION

INTEGRATED CIRCUITS FOR CURRENT-SOURCING APPLICATIONS

FLOATING LOGIC GROUND LEVEL
(Sink Driver)



Dwg. No. A-11,532

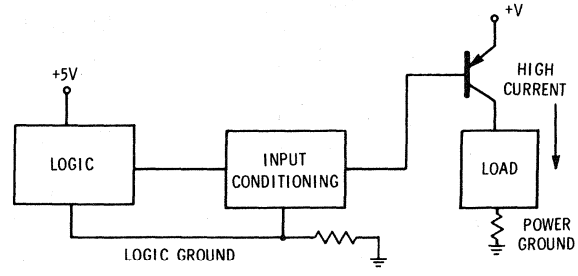
During recent years, the appearance of many new low-power monolithic devices (LSI and microprocessors) has created an increased need of peripheral power driver integrated circuits. Interface drivers are typically categorized in terms of their output-drive functions. When current flows out of the driver output terminal and into the load, the device is said to "source" current. Conversely, current flows from a load into a "sink" driver.

Integrated source drivers usually consist of high-voltage PNP devices and high-power NPN Darlington outputs (which provide PNP-type action), with input-level shifting. These power ICs are useful for interfacing low-level logic (TTL, CMOS, NMOS, PMOS) and high-current or high-voltage relays, solenoids, lamps (incandescent, LED, neon), motors, and displays (gas-discharge, LED, vacuum-fluorescent). They can also be used to provide multi-channel buffers for discrete power semiconductors .

The advantages of source drivers for display interface are quite evident. The X-Y addressing of most readouts requires both source and sink functions to minimize pin count, interconnections, and package count.

A more subtle advantage of source drivers is related to their use with inductive loads or incandescent lamps . Both types of load generate troublesome transients and noise currents on common logic /load ground lines. In addition, high ground currents can shift the ground rail, affecting logic input levels, thresholds, and noise immunity. The use of source drivers can minimize many of these concerns by separating the logic and power returns.

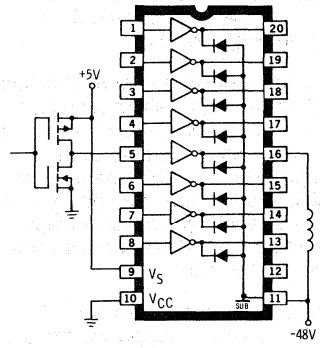
SEPARATE GROUND RETURNS
(Source Driver)



Dwg. No. A-11,531

RELAY-DRIVER APPLICATIONS

TELECOMMUNICATIONS RELAY DRIVER
(Positive logic)



Dwg. No. A-11,524

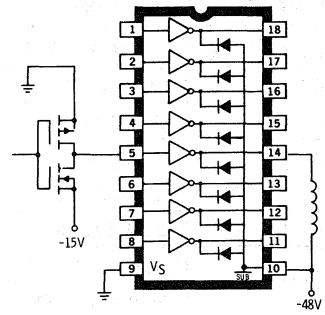
Series UDN2580A, eight-channel source drivers, and Type UDN2957A, five-channel source driver, provide current /voltage translation from TTL, positive CMOS, or negative CMOS logic to -48 V telecommunication relays requiring less than 350 mA. All devices have internal inductive-load transient-suppression diodes.

Type UDN2580A-1 is best driven from negative-reference CMOS or NMOS logic (-5 V or -12 V swing) in order to provide a -48 V swing at the output. The active-low input Type UDN2588A-1 can be driven from positive logic TTL (+5 V swing) or CMOS (+12 V swing) levels. The active-high input UDN2957A is similar to the UDN2588A-1, but it also has a chip-enable function that requires a minimum number of drive lines to control outputs from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

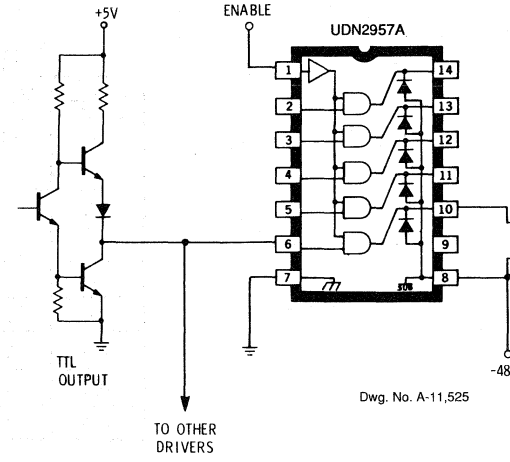
Supply Voltage, V_{EE} . . . . . **-50 V**
Continuous Output Current, I_{OUT} (per output) . . . . . **-350 mA**

TELECOMMUNICATIONS RELAY DRIVER
(Negative logic)



Dwg. No. A-11,538

MULTIPLEXED RELAY DRIVER



Dwg. No. A-11,525

VACUUM-FLUORESCENT/GAS-DISCHARGE DISPLAY APPLICATIONS

Series UDN6100A and UDN2580A source drivers provide solutions to problems encountered in driving higher-voltage vacuum-fluorescent and planar gas-discharge displays. Both series of parts provide TTL, CMOS, and NMOS input-logic compatibility. Series UDN6100A devices are active high (non-inverting) drivers. Series UDN2580A drivers are active low (inverting) devices.

At minimum cost, Series UDN6100A-2 devices offer 60 V output breakdowns for vacuum-fluorescent displays typically utilizing less than 32 characters. Featuring a minimum 80 V output breakdown voltage, standard Series UDN6100A drivers (no additional suffix) guarantee 25 mA per output. Suffix -1 devices provide for a 110 V breakdown, recommending them for 40 to 80-digit or dot-matrix V-F applications or gas-discharge anode-drive applications requiring the higher output voltage. All of these drivers include internal pull-down resistors and provide operation from single-ended positive supplies.

Operation from a split-supply allows the user to bias the V-F filament at ground potential or to utilize a system-supply voltage above ground (±40 V instead of +80 V). The UDN6138A source driver is recommended.

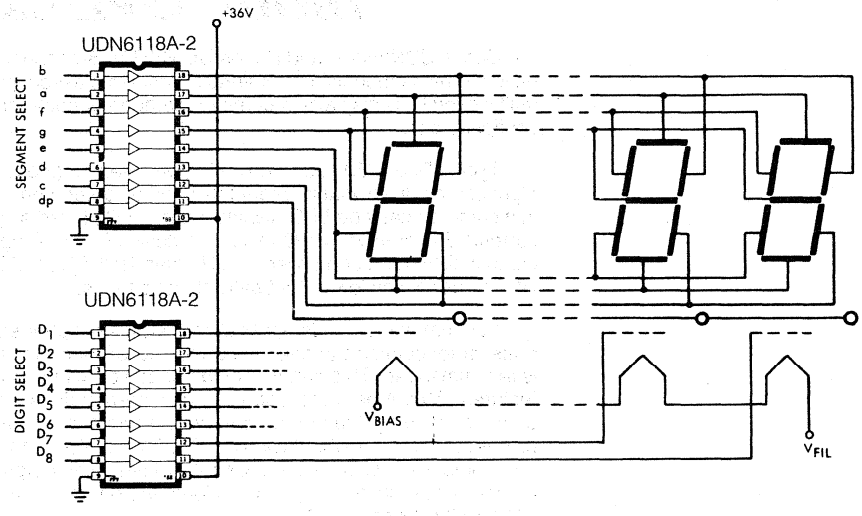
For vacuum-fluorescent display applications requiring a higher current capability (operating several displays with common drive circuitry), Type UDN2588A can be used with appropriate external output pull-down resistors to provide up to 350 mA per output.

MAXIMUM OPERATING VOLTAGES

V_S V_{BB}	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
+5	<14	>4.5	0	-45	UDN2588A
				-75	UDN2588A-1
+12	<8.4	>11.5	0	-45	UDN2588A
				-75	UDN2588A-1
+30	2.4	<0.4	NA	-30	UDN6138A-2
+40	2.4	<0.4	NA	-40	UDN6138A
+60	TTL or CMOS		NA	0	Series UDN6100A-2
+80	TTL or CMOS		NA	0	Series UDN6100A
+110	TTL or CMOS		NA	0	Series UDN6100A-1

CURRENT-SOURCING APPLICATIONS

MULTIPLEXED VACUUM- FLUORESCENT DISPLAY DRIVERS



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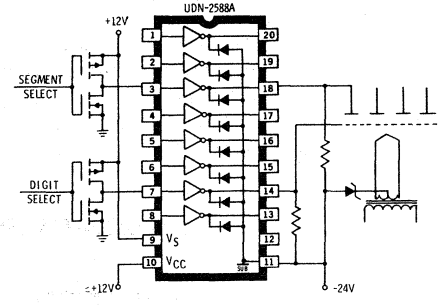


Dwg. No. A-11,526

LIGHT-EMITTING DIODE APPLICATIONS

Series UDN2580A and Series UDN2980A 8-channel source drivers provide monolithic solutions to problems associated with driving multiplexed LED displays in common-cathode or common-anode configurations.

Type UDN2585A is a non-Darlington inverting (input low = output high) source driver that is frequently used as a segment or dot driver in a common-cathode LED display where multiplexed segment or dot currents do not exceed 120 mA . This device features input logic-level compatibility with open-collector TTL, standard TTL, CMOS, and NMOS, as well as low output saturation voltages.

For common-cathode applications requiring higher segment currents, or for common-anode digit drive applications, Series UDN2980A is recommended. This non-inverting (input high = output high) series features 350 mA per output continuous current ratings with peak currents reaching 500 mA per output. Outputs may be paralleled for higher current capability. Type UDN2982A is logic-compatible with 2.4 V output levels of TTL and CMOS. Similar high output current ratings, for use in inverting applications, are offered by the Type UDN2580A driver.

Combining source drivers with multi-channel, high-current sink drivers (such as Type ULN2068B, UDN2595A, or ULN2814A) provides simple, compact, and economical solutions to driving high-current multiplexed LED displays.

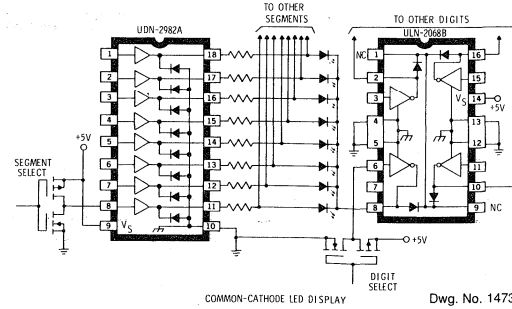
RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S
- UDN2585A . . . . . **15 V**
- UDN2982A . . . . . **45 V**

Continuous Output Current, I_{OUT} (per output)
- UDN2585A . . . . . **-120 mA**
- UDN2982A . . . . . **-350 mA**

Input Voltage, V_{IN} . . . . . **15 V**

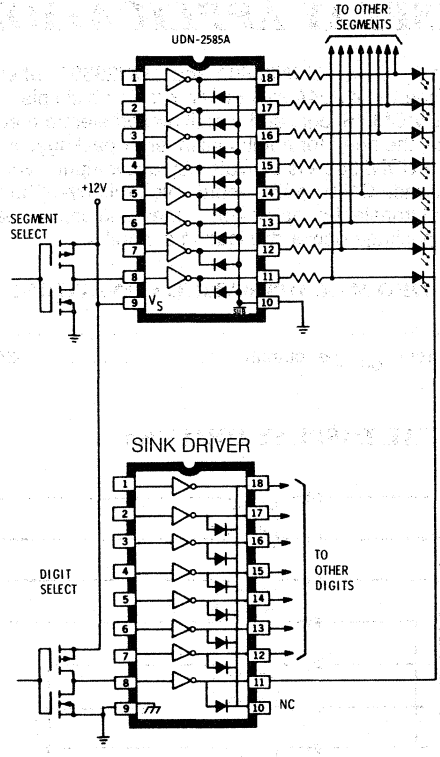
COMMON-CATHODE LED DISPLAY



Dwg. No. 1473A

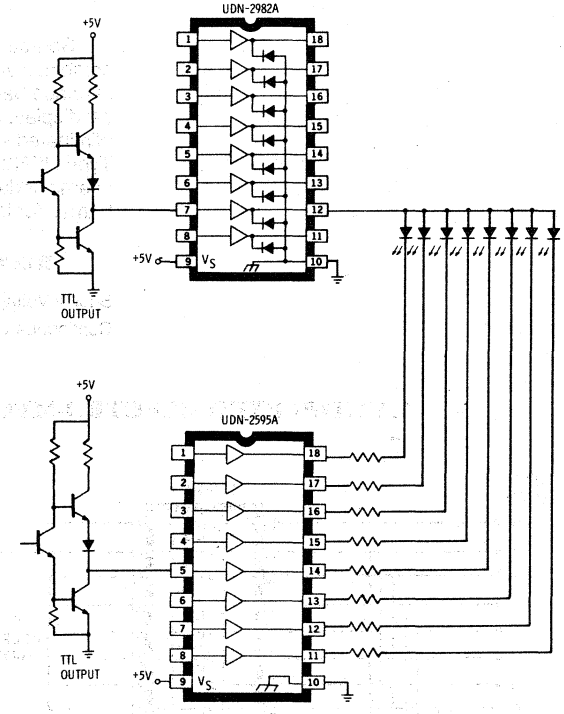
CURRENT-SOURCING APPLICATIONS

COMMON-CATHODE LED DISPLAY



Dwg. No. B-1481

COMMON-ANODE LED DISPLAY



Dwg. No. B-1480

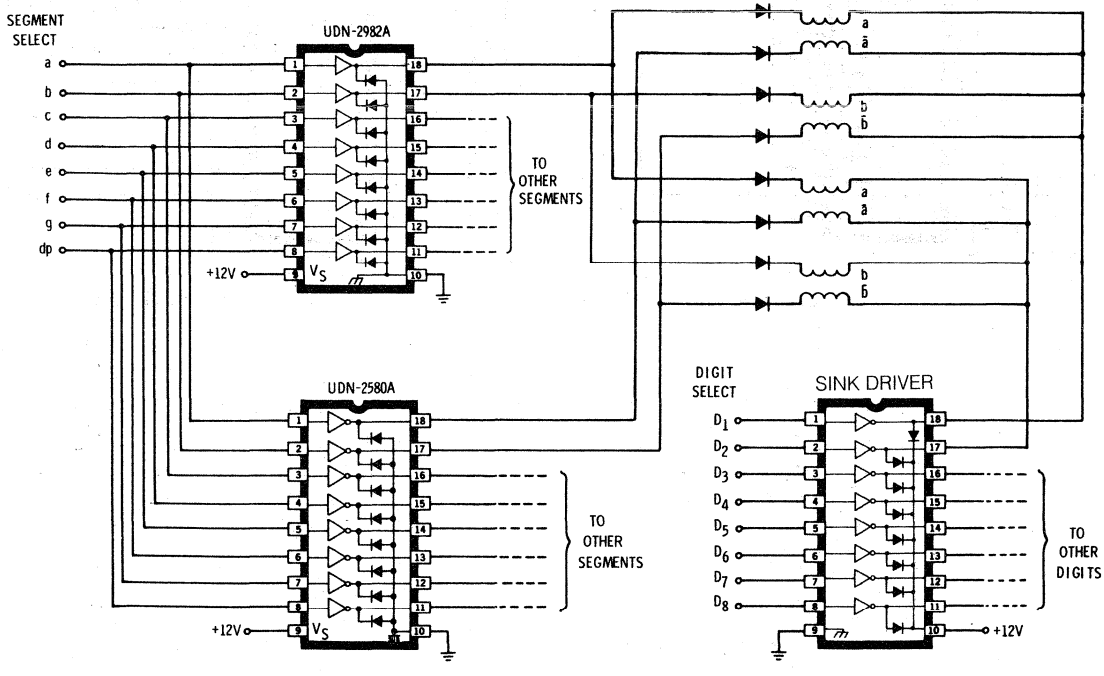
ELECTRO-MECHANICAL DISPLAY APPLICATIONS

Source drivers in the Series UDN2580A and UDN2980A, when combined with the Type ULN2804A sink driver, provide a simple interface between 12 V CMOS logic and a multiplexed electro-mechanical display. As shown, the need for additional inverter packages is eliminated since Type UDN2580A is activated by a low input level and Type UDN2982A is turned ON by a high input level. All drivers have internal inductive-load transient-suppression diodes and copper lead frames for improved package power dissipation capability.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S . . . . . **35 V**
Continuous Output Current, I_{OUT} (per output) . . . . . **-350 mA**

MULTIPLEXED ELECTRO-MECHANICAL DISPLAY DRIVERS



Dwg. No. B-1476

PRINTER APPLICATIONS

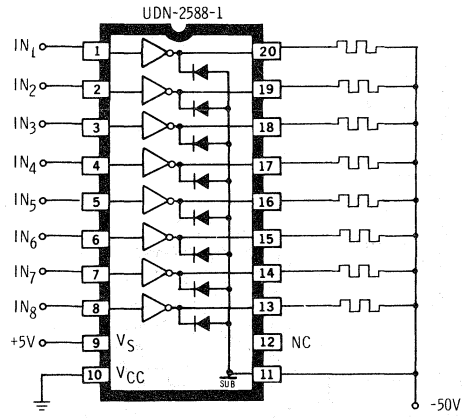
Source drivers have been used extensively in electrosensitive, thermal, and impact printer applications. Multi-channel devices in the Series UDN2580A and UDN2980A reduce parts count and provide up to 350 mA per output at voltages up to 75 V (resistive load). Copper lead frames make these devices capable of simultaneously delivering up to 125 mA continuously from all eight channels at an ambient temperature of +50°C.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_S
- UDN2588A-1 . . . . . **to 75 V**
- UDN2981A and UDN2982A . . . . . **5 V to 45 V**
- UDN2983A and UDN2984A . . . . . **35 V to 75 V**

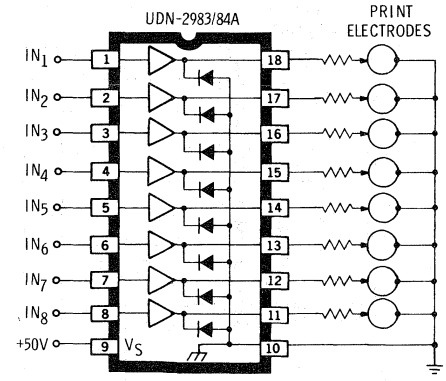
Logic Voltage, V_{IN} . . . . . **12 V**
Continuous Output Current, I_{OUT} (per output) . . . . . **-350 mA**
Peak Output Current, I_{OP} . . . . . **- 500 mA**

THERMAL PRINTER APPLICATION



Dwg. No. A-11,530

ELECTROSENSITIVE PRINTER APPLICATION



Dwg. No. A-11,529

INCANDESCENT LAMP DRIVER APPLICATIONS

Driving multiplexed incandescent lamps at voltages up to 75 V with peak currents approaching 500 mA per segment, Series UDN2980A eight-channel source drivers, when combined with Type ULN2069B sink drivers, provide for a very cost-effective approach. Multiplexed lamps must typically be operated at a voltage $\sqrt{N}$ (N = the number of digits) times the nominal d-c voltage, to obtain sufficient brightness. For example, a four-digit, 28 V display requires 56 V to operate satisfactorily. In addition, care must be taken to select a proper driver to withstand the substantial inrush currents created by cold filaments. Peak currents of up to ten times the nominal operating currents have been observed. Multiplexed lamps must also incorporate diodes to prevent series /parallel paths to unaddressed elements.

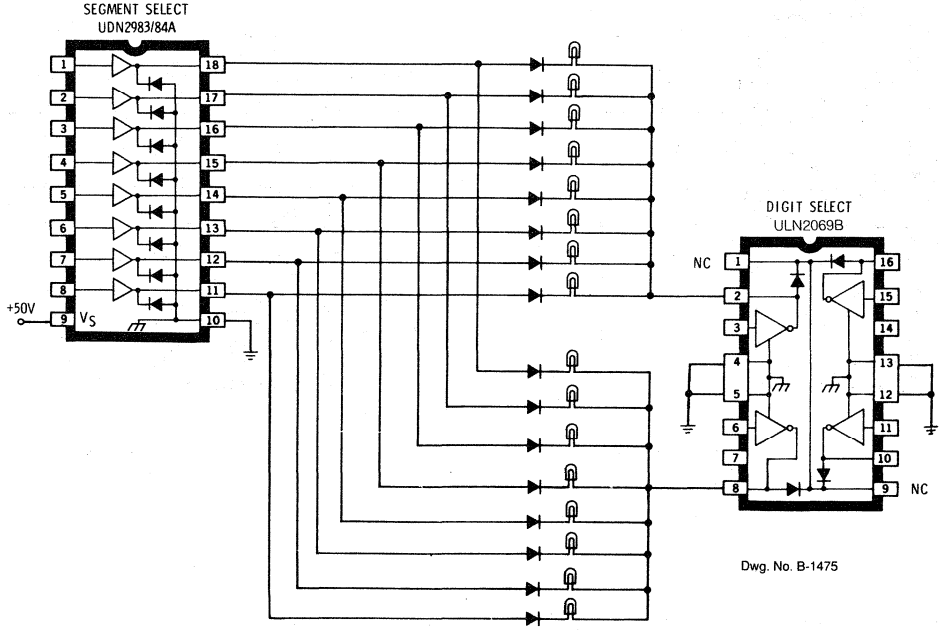
RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_S
- UDN2981A and UDN2982A . . . . . 5 V to 45 V
- UDN2983A and UDN2984A . . . . . 35 V to 75 V

Continuous Output Current, I_{OUT} (per output) . . . . . -350 mA

Peak Output Current, I_{OP} . . . . . -500 mA

MULTIPLEXED LAMP DRIVER, TTL- OR MOS-COMPATIBLE

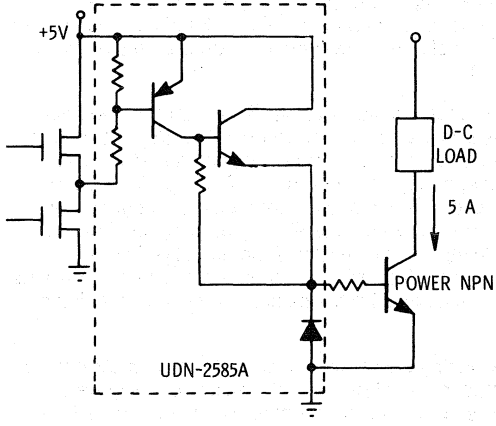


MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

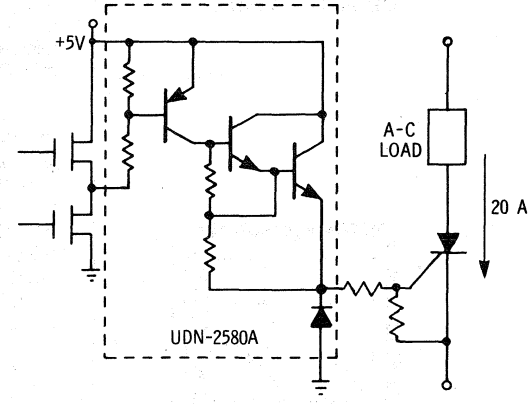
Source drivers can be employed as multi-channel pre-drivers for discrete high-current or high-voltage semiconductors, thus reducing the need for many discrete components. For instance, a UDN2580A 8-channel source driver can provide up to 350 mA of pre-drive current into the base of power NPN devices, making 5 A load currents readily available. Higher load currents can be obtained by using power NPN Darlington devices.

For a-c loads, it is possible to use a source driver to provide gate current (with appropriate current-limiting) to a power SCR or triac. This scheme can provide an economical solution to many applications such as driving incandescent lamps or a-c motors at up to 20 A.

DRIVER FOR HIGH-POWER DISCRETE DEVICES



Dwg. No. A-11,533



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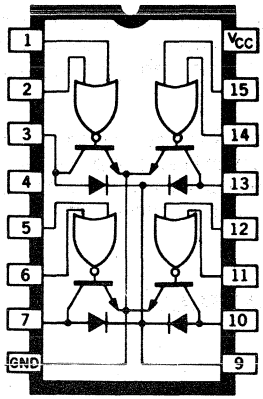
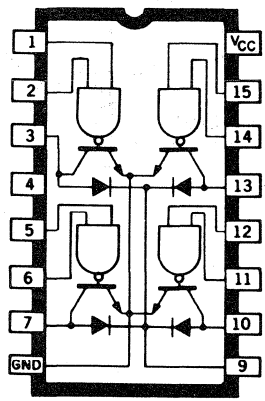
APPLICATIONS INFORMATION

EXPANDING THE FRONTIERS OF IC INTERFACE FOR ELECTRONIC DISPLAYS



Dwg. No. A-9869



Dwg. No. A-9866

FIGURE 1

INTRODUCTION

The original monolithic high-voltage/high-current power drivers (Series UHP500) were capable of sustaining 100 V and sinking load currents of 250 mA on each of four outputs. That 1970 peripheral driver capability has since been expanded and improved on to solve many of the most difficult display interfaces. Newer devices are rated for operation to 130 V, sourcing or sinking to 1.5 A, and as many as eight drivers per package (not all together) with inputs for TTL, Schottky TTL, DTL, CMOS, and PMOS.

LAMP (INCANDESCENT) INTERFACE

Utilizing marketing inputs that related to existing hybrid interface circuits, a group designed and manufactured monolithic ICs which initially were largely used for aircraft indicator lamp interface. Although not widely known, these quad driver units were developed quite independently (and simultaneously) to the ubiquitous TI 75451 series of high-speed, low-voltage peripheral drivers. A concentration upon circuit design factors, improvements in DIP packaging (copper alloy lead frames), and tighter, tougher control of diffusion-related parameters has allowed the manufacture of quad power drivers rather than the dual mini-DIPs offered by TI.

An increased awareness for improvements in reliability and space and power reductions provided a rather successful military market for lamp and relay interface; early success was evident in military aircraft indicator lamp interface, a tough application for TTL type ICs due to severe inrush currents resulting in secondary breakdown during "turn on". The increased current sinking capability of the peripheral power driver ICs offers a solution to lamp interface that usually obviates the need for "warming" resistors (across the output) which slightly warm the lamp filament and thus minimize problems associated with cold lamp filaments.

The high current-sinking capability of these ICs allow such loads as the #327 or #387 lamps to be driven without difficulty of secondary breakdown. The device beta will usually not allow sinking of the 10 to 13 times (nominal value) inrush current of cold lamps; but the lamp rapidly reaches a current level within the device output limitations (Figure 2 shows current as a function of time for a single #327 lamp). Sustaining this instantaneous inrush current and its peak power has been a key element in the success of many lamp interface circuits.

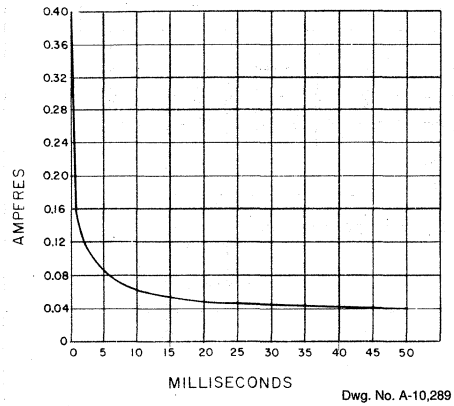
GAS DISCHARGE DISPLAY ICs

Early in 1972, the first high-voltage IC designed for gas discharge displays—a five channel, 130 V unit for cathode (segment) interface was produced. Subsequently, other circuits, both cathode and anode drivers, were produced; most of which were used in calculator applications with the Burroughs Panaplex® II.

Through a collaborative effort begun late in 1973 with Burroughs Corp. a newer, more efficient interface scheme evolved. Featured in

IC INTERFACE FOR ELECTRONIC DISPLAYS

"Electronic Displays '75," this series of monolithic IC interface devices for the high-voltage gas discharge panels has been one of the trailblazers in the world of display interface ICs. Intended for use in multiplexed display systems, these ICs present one of the easiest and least expensive solutions to a difficult interface problem. A combination of high-voltage bipolar techniques with thin-film resistor technology (circuit resistors sputtered over the IC dielectric) has provided both digit (anode) and segment (cathode) interface.



Dwg. No. A-10,289

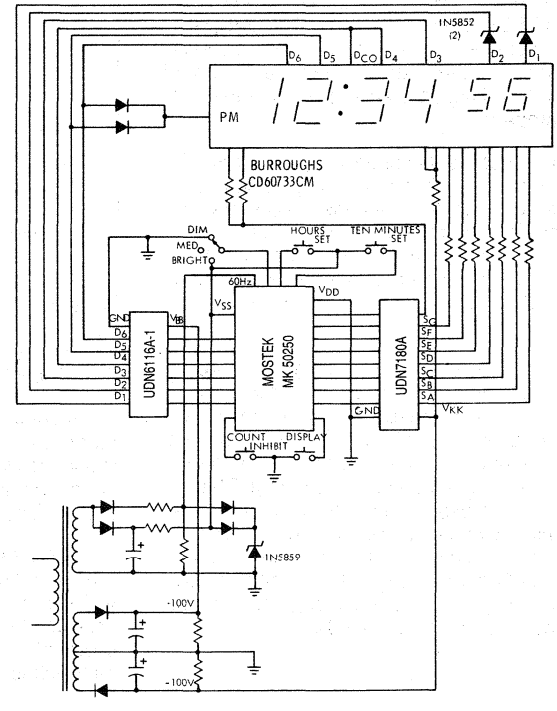
FIGURE 2

To facilitate a minimum component interface, a split supply (±100 V) is employed to allow dc level-shifting (rather than capacitors or >200 V transistors) and both digit and segment drivers incorporate all pull-up, pull-down, current limiting, off-bias reference, etc. which were formerly required in discrete and/or hybrid systems. With the combination of the digit and segment drivers (each capable of withstanding 120 V), the split power supply approach affords PN diode IC technology suitable for driving a display usually requiring a 180 V minimum ionization voltage (equivalent to ±90 V in the split system).

The use of the Series UDN6100/7100A gas discharge display drivers shows the need for only two monolithic ICs for displays of up to eight digits and eight segments as shown in Figure 3. Systems requiring digit or segment counts greater than eight employ additional driver ICs. The UDN7180A device, for reasons of package power dissipation and/or dissimilar segment currents (certain 14 or 16 segment alphanumeric panels) uses external, discrete current-limiting resistors.

Higher current applications are difficult for both programmable current and switching type display drivers. Segment currents beyond 2.5 or 3 mA present package power dissipation limitations to most dual in-line packages. By using external resistors, the UDN7180A driver allows segment currents of up to 14 mA.

The transistor switch with current-limiting resistor scheme used in these gas discharge display drivers also minimizes problems associated with gas panel arcing which can destroy programmable current circuits. Some of the gas display manufacturers recommend the use of series resistors in each segment line to prevent destruction to the semiconductor interface circuit should such a panel arc occur. Without these series resistors (internal thin-film resistors in these devices) the IC can be destroyed by the high voltage and resulting high current should the panel voltage drop to a very-low level during an arc.



Dwg. No. A-9751B

FIGURE 3

LED INTERFACE

With the obvious abundance and variety of LED interface integrated circuits it would seem unlikely that there are still systems in search of an IC hardware solution to further minimize cost, component count, space, etc.; but this is definitely the case. The deficiencies are chiefly related to the limited number of current-sourcing circuits and/or high-current drivers.

The efficiency of LED displays has improved, but with the larger digits (up to 1" presently) most of the IC drivers are unable to switch the higher currents required in multiplexed systems. The rule-of-thumb generally applied uses the suggested dc current—multiplied by the number of digits in the display. For example, a multiplexed display of 160 mA peak current will give approximately the same light intensity output as a steady 20 mA in each of eight digits. Of particular difficulty is the switching of currents associated with the lower efficiency yellow and green LEDs. Completely monolithic integrated circuit solutions are available for applications requiring segment currents (source drivers) of 350 mA and digit currents (sink drivers) of up to 4 amperes!

Many of the ICs used in high-current LED applications were originally designed for use with electro-mechanical loads (relays, solenoids, motors, etc.) although the high-voltage ratings of the drivers are obviously not a concern. A combination of high-current, high-voltage Darlington drivers is shown in Figure 4.

The ULN2074B source driver is utilized as a modified emitter-follower. Through the use of discrete diodes in the common collector line, allowing the base to be switched to a potential higher than the collector, it is then possible to obtain a saturated output. This prevents the usual emitter-follower problems associated with gain, the MOS output impedance, and power. It is also possible to now better define the voltage at the emitter output and to then provide suitable segment current-limiting resistors for the LEDs.

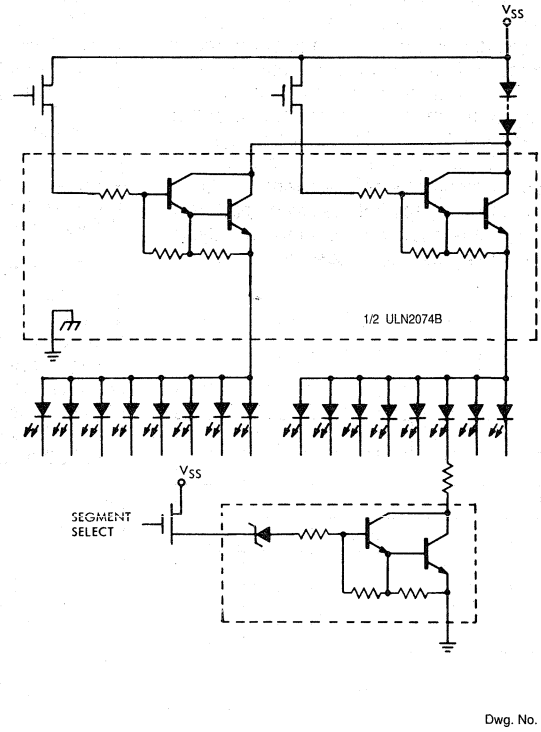


FIGURE 4

An eight-channel source driver is shown as a digit switch for common anode LEDs in Figure 5. The Series UDN2980A drivers will handle output currents to a maximum of 500 mA. Two basic versions of the driver will allow interface from TTL, Schottky TTL, DTL, PMOS, and CMOS levels.

A common-cathode LED configuration is shown in Figure 6 for currents of up to 1.5 A per digit. A Series UDN2980A source driver is used to switch the segment side, the ULN2064B or ULN2074B to switch the digit side. As has been shown with Figure 4, the IC package power dissipation must be considered with high-current applications.

The three examples that have been shown for LED interface represent only a very-small portion of the total applications area. The high-current capabilities and high gain of the drivers represent potential solutions to many difficult LED display systems—alphanumeric, seven-segment, or matrix; common-cathode or common-anode; continuous or multiplexed.

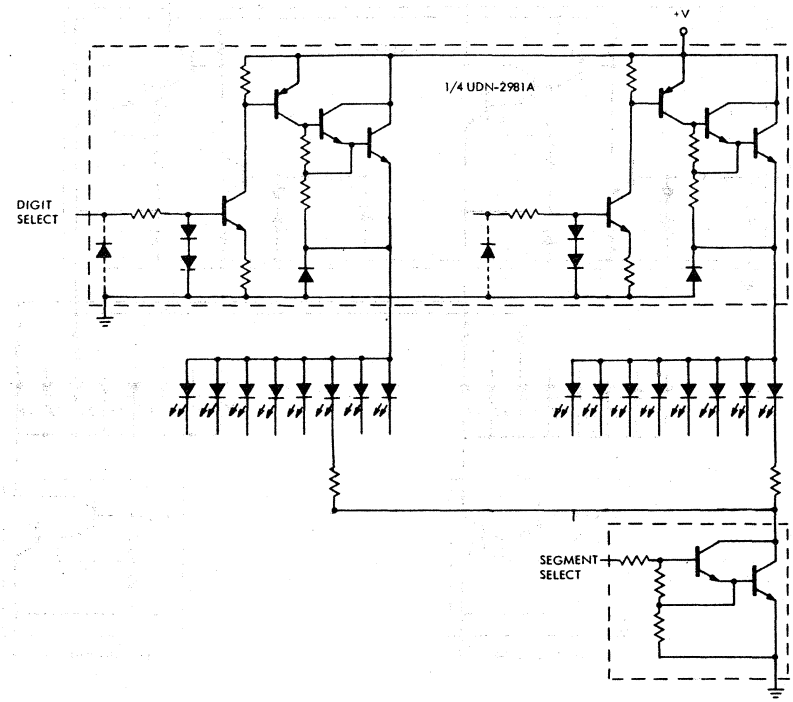


FIGURE 5

AC PLASMA DISPLAY INTERFACE

Plasma displays, such as those manufactured by National Electronics/NCR (USA) and NEC or Fujitsu (Japan), all have one common element with their gas discharge cousin—both types use a neon gas mixture. The plasma panels emit an orange glow when switched at rather high frequencies, and light output intensity is a function of frequency. The ac term for the plasma display is something of a misnomer since these panels actually operate from a toggled dc supply (usually in the area of 20 kHz).

The panel is basically a neon-filled capacitor, and has plates (electrodes) which are covered with the dielectric—between which is the neon mixture. Switching this capacitive load presents a problem with high peak currents in addition to the older problem of the high voltages which are associated with gas displays. Drive circuits use supply voltages of 150 to 260 V (depending on unipolar or bipolar drive), and the semiconductors used must switch instantaneous currents in the order of several hundred milliamperes for the larger displays.

Several high-voltage, high-current arrays can provide an answer to one side of the ac plasma display interface. The ULN7003A Darlington power driver is rated at 150 V. It is able to handle the application shown in Figure 7 (a basic dc, non-multiplexed clock interface rather than a more complex multiplexed system).

The high-current diodes that are internal to the arrays are utilized in the unipolar drive scheme connected to a suitable OFF reference. In one POS application, a set of 14 ULN7003A Darlington drivers replace more than 400 discrete components. The cost and space savings in such a machine are considerable, and a very complex printed wiring board was greatly simplified.

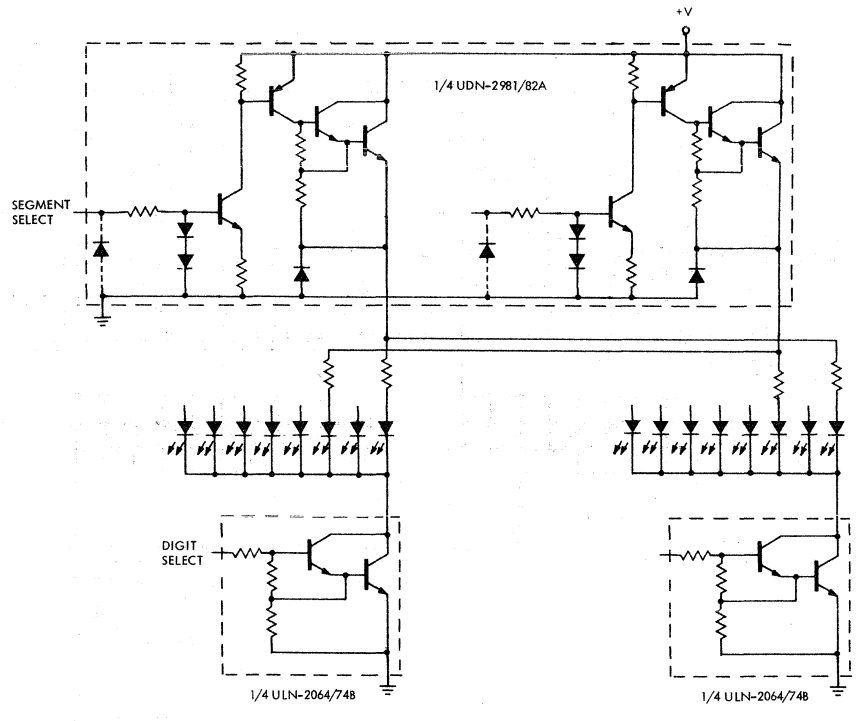


FIGURE 6

Further improvements in interface and plasma displays will no doubt evolve, and thus benefit all concerned— display and interface vendor along with the end user. Plasma displays are well-suited to custom panels (particularly those with various sizes of characters) and with improvements in IC breakdown voltages some further simplification of interface should evolve.

FLUORESCENT DISPLAY INTERFACE

Although the vast majority of fluorescent displays are directly driven from MOS logic (handheld and low-cost desk calculators), there is an emerging need for interface integrated circuits for use with the larger characters (higher currents) and the higher voltages coming into use. These blue-green display panels originated in Japan, and the manufacturers are quite aggressively pursuing markets such as POS systems, clocks, cash registers, appliances, automotive displays, etc. Larger and/or more complex styles are being made, including displays with alphanumeric capability (a starburst 14 or 16-segment pattern).

Modest voltage capability (60 or 70 volts) is all that is required of a semiconductor device to drive these panels, and the currents are in 20 to 30 mA region. These electrical requirements are well within the capability of many gas discharge digit drivers.

The UDN6118A device is designed specifically for use with fluorescent displays and includes internal pull-down resistors so that up to eight segments and eight digits will require only two packages and a greatly simplified power supply (Figure 8). The UDN6118A driver is compatible with TTL, Schottky TTL, DTL, and 5 volt CMOS.

The future of fluorescent displays look rather strong, particularly if competition further reduces prices. For the moment at least, these displays will not seriously tax the capability of IC interface.

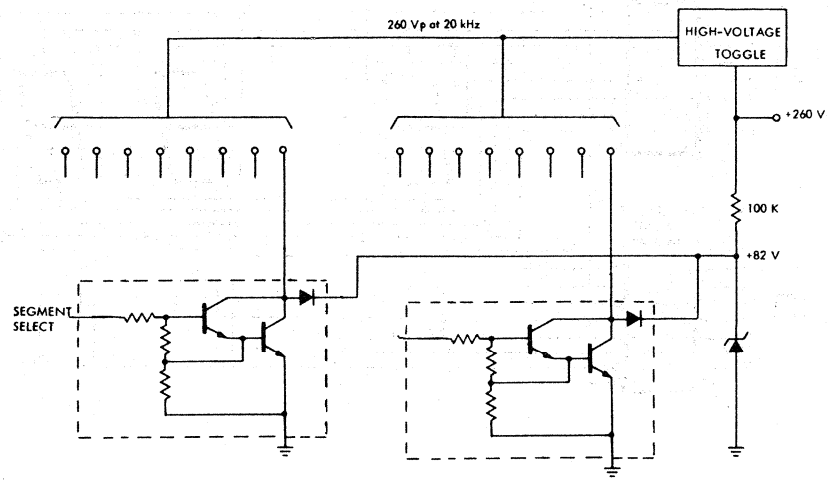


FIGURE 7

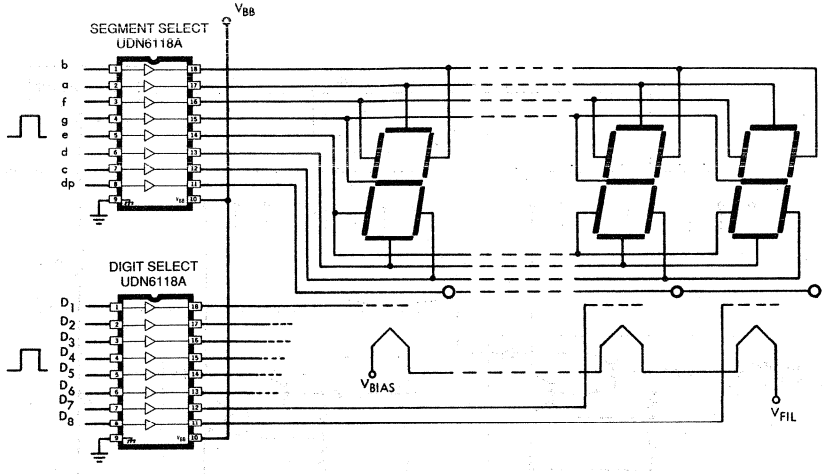
HOT WIRE READOUTS

Although hot wire readouts could easily be placed in the incandescent category, their application in multidigit, multiplexed display systems more closely resembles LED circuit operation. Since hot wire displays will conduct current in either direction, isolation diodes are required to prevent sneak paths from partially turning ON unaddressed segments. Compare the typical hot wire display of Figure 9 with the LED display of Figure 5. The availability of a suitable, inexpensive diode array would be of considerable asset in multiplexed hot wire systems.

The hot wire readouts are available in both seven-segment and alphanumeric (16-segment) versions and are quite well-suited to high ambient light applications. They do not wash out in sunlight, although their reliability diminishes with the higher currents required in brightly lighted applications. As described, multiplexed schemes can be cumbersome because of the great number of discrete diodes required. One avionics system using a 16-character, 16-segment alphanumeric panel required 256 discrete diodes.

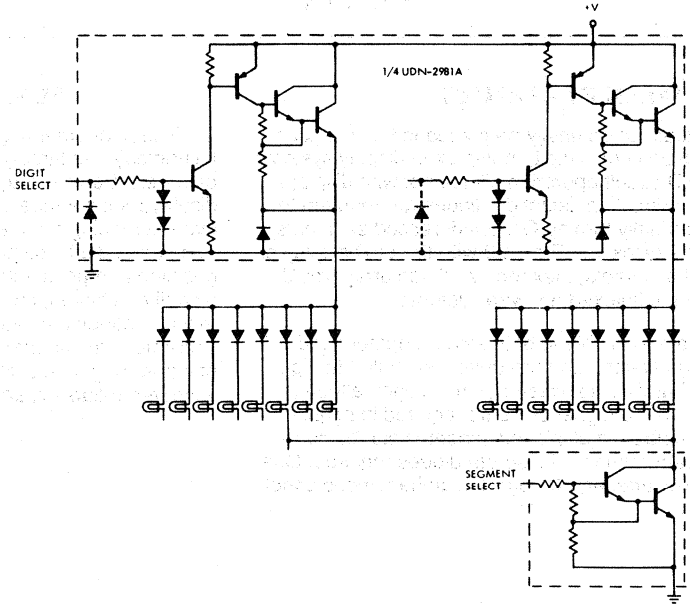
SUMMARY

The phenomenal growth in display technology has largely come as a result of the electronic calculator, and electronic displays will pervade all our lives in an ever-increasing number of products. The use of digital displays in appliances, gasoline pumps, electronic games (even pinball machines), etc., etc., will also require that a continuing evolution on interface integrated circuits meet the challenges of higher brightness, increased currents, improved reliability, and lower system costs.



Dwg. No. A-10,261B

FIGURE 8



Dwg. No. B-1362

FIGURE 9

APPLICATIONS INFORMATION

TRENDS IN IC INTERFACE FOR ELECTRONIC DISPLAYS

Display technology was truly set into high gear by the explosion of the electronic calculator business. Expansion at a phenomenal pace continues, encompassing a multitude of products, particularly high-volume consumer products (calculators, clocks, games, and watches). Recently, further stimulated by the "microprocessor revolution," with its far-reaching effects, and the resulting changeover to solid state design from electromechanical, mechanical, fluidic, or electrical systems, the vistas for displays have expanded well beyond the horizon. Products have been and are being developed, using microprocessors and displays, that never previously existed.

To augment this microprocessor revolution, semiconductor manufacturers are developing many new interface circuits useful with displays, although some of these will not be exclusively for display systems. To accomplish this, the present boundaries of device design, process, packaging, and electrical parameters will require continual extension and expansion.

DISPLAY BUFFERS

A continuing evolution of standard interface ICs is needed to buffer low-level logic from high-voltage and/or high-current loads. Some of this buffer development will serve display systems. Since there already is a broad assortment of buffers (particularly for low-to medium-current LED applications), the ongoing development in simple or low-order interface will mainly concentrate upon further reduction in discrete component count, package improvement (particularly for high-current/high-power devices), improvements in device current, voltage, switching speed, and greater reliability.

Figures 1, 2, and 3 show some interface ICs that represent buffer circuits; other vendors supply similar, or identical, high-current or high-voltage buffers to allow operation of displays from low-level logic. Two basic changes have occurred relatively recently:

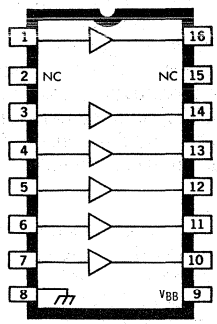
1. Greater use of 18-pin DIPs for eight driver channels (Source Driver, Figure 2).

2. Creation of sourcing functions (Figures 2 and 3; useful for LED, gas-discharge, vacuum fluorescent, incandescent, and electromagnetic displays, depending upon device ratings). While further buffer designs are needed (particularly in high-current (>2 A) and high-voltage (>100 V) circuits), the main emphasis will be toward the incorporation of logic and control circuitry with output buffers.

COMPLEX INTERFACE

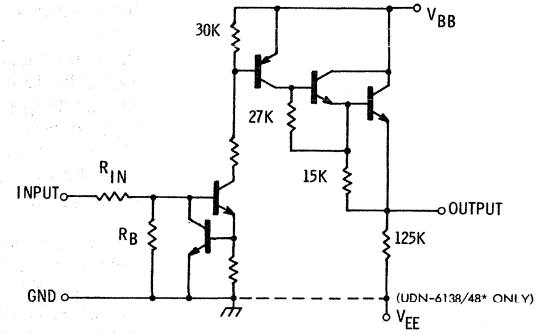
Paralleling (though lagging) the microprocessor LSI revolution is the area of greatest future for IC display circuits: The need for complex, smart or high-order interface. This will be MSI to LSI logic (with perhaps some linear functions) combined with suitable output buffers.

UDN6116A-1
GAS-DISCHARGE DRIVER



Dwg. No. A-9643A

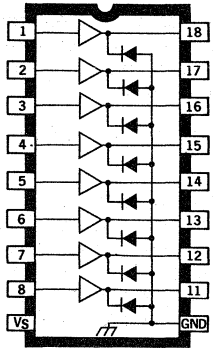
FIGURE 1A



Dwg. No. A-10,592C

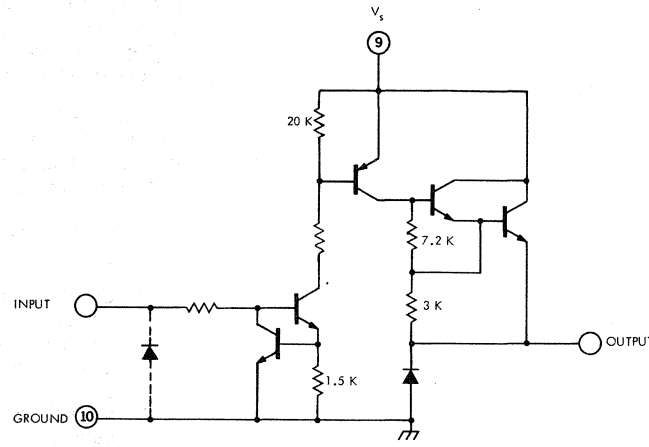
FIGURE 1B

SERIES UDN2980A
SOURCE DRIVER



Dwg. No. A-10,243

FIGURE 2A



Dwg. No. A-10,242A

FIGURE 2B

8-DIGIT/8-SEGMENT HIGH-CURRENT LED INTERFACE

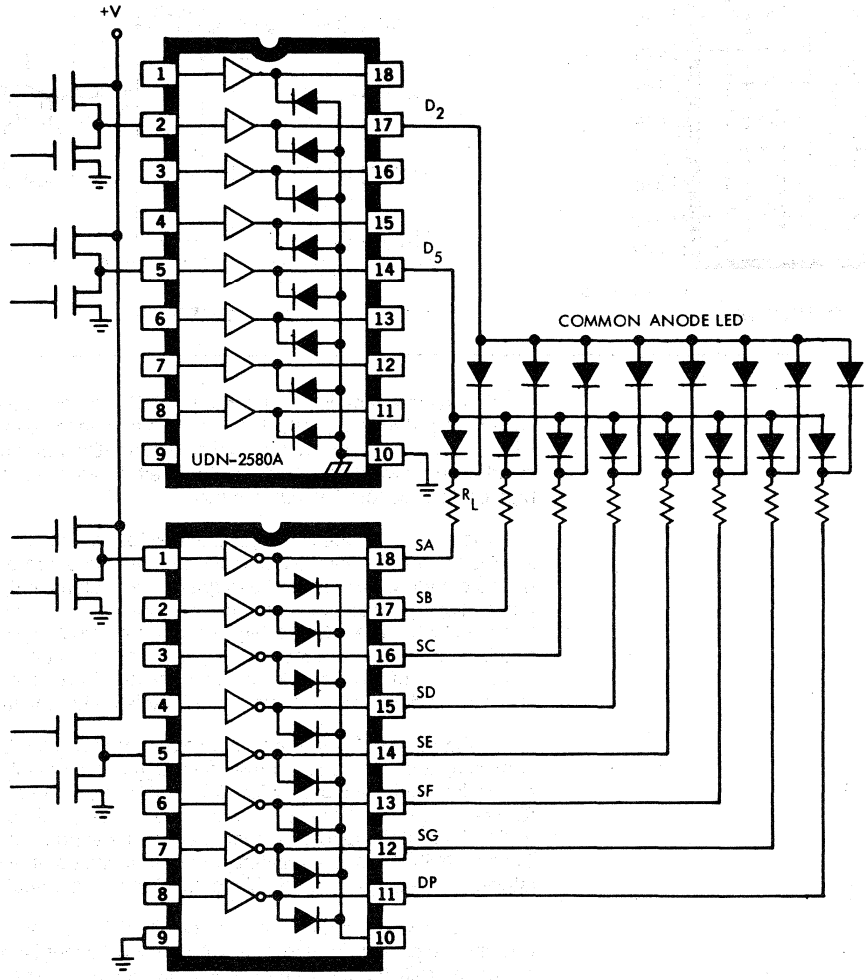
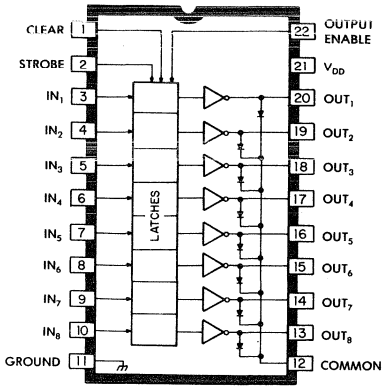


FIGURE 3

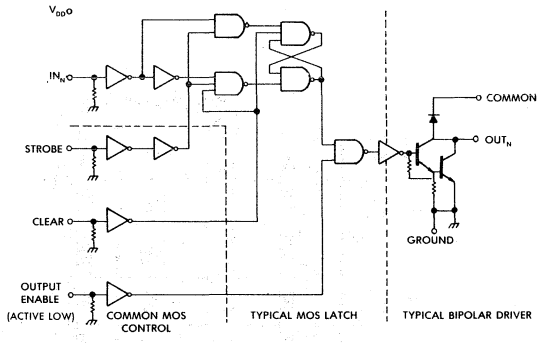


Dwg. No. A-10,498A

FIGURE 4A

UCN5801A

BiMOS LATCH/DRIVER



Dwg. No. A-10,495A

FIGURE 4B

Display interface ICs (similar to the MOS I/O control chips), both custom and standard product, are becoming available in this category. High-volume applications may justify custom ICs, but the more general trend will be toward standard, off-the-shelf designs— chiefly due to the high costs of developing custom ICs.

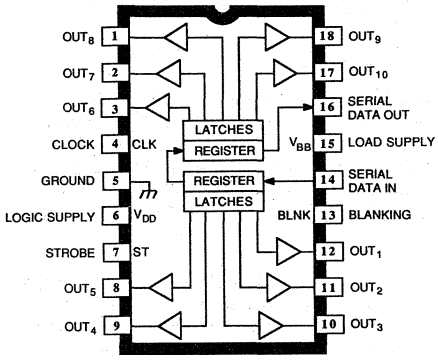
The higher voltage displays (gas-discharge, vacuum fluorescent, ac plasma, and dc electroluminescent) may share some circuits (if appropriately planned and designed), particularly in the area of matrix displays. It is difficult to imagine, however, much commonality between high-current LEDs, high-voltage gas-discharge or ac plasma, and low-power LCDs, although they should share considerably the development of cellular CAD circuit designs. Basic shift registers, latches and decoders do have considerable commonality.

In Figure 4 is a pinout and logic diagram of a BiMOS device combining logic and output drive. Although not expressly intended for display applications, this BiMOS (CMOS logic and bipolar outputs) IC has a great deal of utility to engineers working with lower voltages and high currents (LEDs, incandescent and electromagnetic displays). Type UCN5801A is a parallel-in/parallel-out unit composed of eight 'D' latches and eight 350 mA/50 V bipolar Darlington outputs.

More recently, serial-in/parallel-out BiMOS interface ICs have been designed expressly for use with vacuum fluorescent displays. Figure 5 shows the UCN5810A 10-bit serial-in/parallel-out interface for use with VF displays; the use of serial data allows 10 output lines, data in and data out in a standard 18-lead DIP. It makes possible both fewer IC packages and simpler PC board wiring, although it is slower than a parallel data approach. It uses only a single pin of the I/O ports.

A slightly more recent design for vacuum fluorescent displays is the UCN5815A. This is a 22-lead, 8-bit parallel-in/parallel-out BiMOS unit. The unit may have data inputs and a strobe bus (see Figure 6). The chip enable/blanking pin provides control of VF buffers. A power-on-clear is internally incorporated.

UCN5810A



Dwg. PP-029

FIGURE 5A

UCN5815A
PARALLEL 8-BIT VF INTERFACE

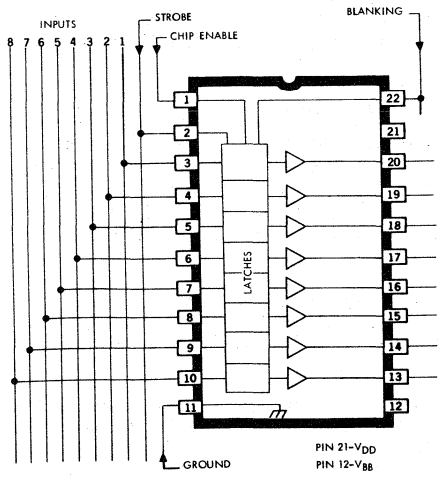


FIGURE 6

VF DRIVER BLOCK DIAGRAM

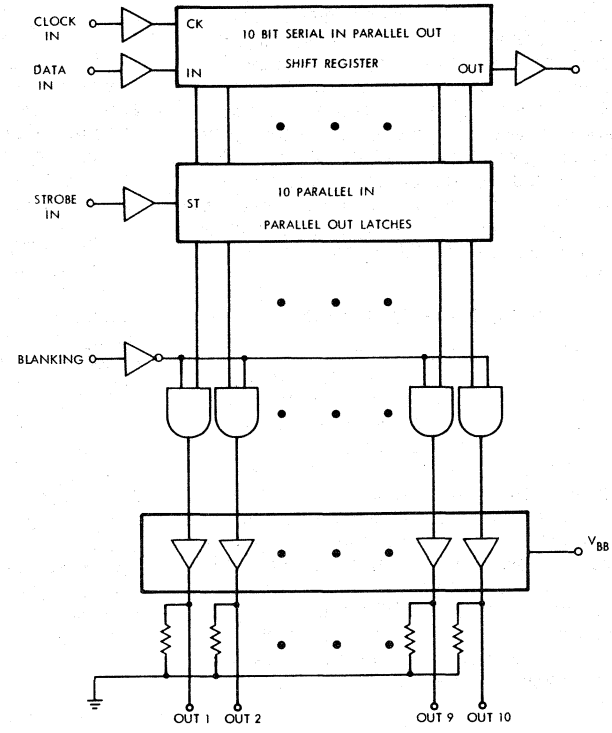


FIGURE 5B

TRENDS IN IC INTERFACE
FOR ELECTRONIC DISPLAY

DEVICE TECHNOLOGIES

With the exception of LCD displays (which at least until recently have been largely, if not entirely, driven by MOS) the display and interface technologies in high-volume use are mainly associated with bipolar semiconductors. Early display interface ICs (particularly devices such as the 7447 and 7448) were aimed at LED technology and represent MSI with modest output capability. The increasing use of higher voltage displays, multiplexed high-current applications, and the need for greater circuit complexity and low pin count will dictate other technologies, such as I^2L, BiMOS, CMOS/DMOS, and possibly DMOS.

STANDARD BIPOLAR

Standard bipolar technology, long associated with TTL or linears (early op amps), appears very limited in scope for the future. Circuit density and supply power requirements will dictate other processes for functions beyond the simple MSI level. The advantages of standard bipolar ICs appear to be in the areas of simple high-current, high-power, or high-voltage interface. In particular, applications requiring the combination of high voltages (≥100 V) or multiple high-current outputs (≥2 A) will restrict the logic/control circuitry to a low level. Cost, chip size, and package power dissipation will restrict this circuitry largely to versatile, simple buffers.

I^2L

Anticipated to increase significantly is the use of I^2L for systems of low-to-modest voltages (LEDs through VF). The present limits of I^2L appear to be limited to applications below the 50- to 60-volt level. I^2L, with its combination of circuit density, low power and reasonable switching speeds should make a fine match for LEDs or other low-voltage display applications. For higher voltages (>25 or 30 V), prospects the penalty of reduced circuit density may diminish its cost effectiveness. Some increase in standoff voltage may be afforded by the uses of cascaded output transistors or process improvements, thus reducing the need to sacrifice logic density. Without a standard I^2L logic family, the main market penetration would appear to be custom designs although there is a definite opportunity for standard interface for lower voltage applications, particularly LEDs and vacuum fluorescent.

BiMOS

BiMOS, a combination of CMOS and bipolar for interface ICs, seems to fit a technology niche of higher breakdown voltages than I^2L, especially where logic power and supply voltage range (5 to 15 V) is important. Other BiMOS or BiFET ICs which are presently on the market, are largely related to operational amplifiers, although other uses, such as the Series UCN5800 application of BiMOS to interface, are emerging.

Currently, it is feasible to design and manufacture BiMOS interface with breakdown voltages in the 80 to 100 V range. With additional time and greater concentration on increasing breakdown voltage, it appears that higher voltages (≥150 V) for output buffers could be obtained. By obtaining breakdowns in the 120 V to 160 V range, BiMOS then becomes a viable IC technology for interface for the higher voltage displays: dc gas-discharge with ±100 to ±130 V and glow transfer or dc electroluminescent (DCEL) opportunities with a range of 120-150 volts.

Switching speeds and output configurations (active pull-down or resistive) are critical to matrix displays with large numbers of drive lines. Adding active pull-down or pull-up will tend to increase chip size (and cost), thus adding to the potential overall difficulty of BiMOS with its greater process complexity and slightly longer manufacturing cycle. This does appear to be a very key technology for the near future. Its product niche will include applications requiring 60 to 100 V (or more) breakdowns, low-power logic, wide supply range, modest speeds, and MSI to small LSI.

CMOS/DMOS

CMOS/DMOS display interface appears to be intended for much of the same display market as BiMOS. Product information now available indicates 60 to 100 V breakdown (DMOS outputs), CMOS logic, low-to-modest output currents (≤25 mA), and logic speeds to 4 MHz. Designs now being promoted are targeted toward ac plasma and vacuum fluorescent panels.

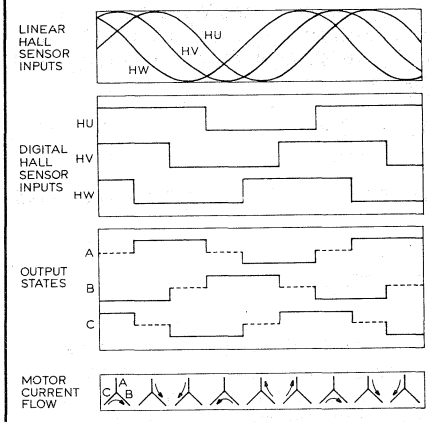
Two apparent disadvantages now appear to exist:

1. Logic operates from 12 V ±10% (may be done to provide maximum speed).
2. Output drive current is insufficient for high-current displays (without 100 mA, or more, the larger matrix panels will use discretes or another technology).

These shortcomings may be modified with time, although it is doubtful if 500 mA to 1A DMOS ouputs are practical.

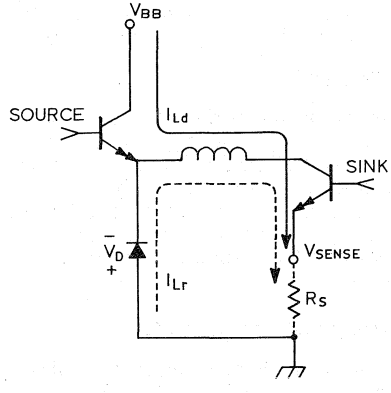
APPLICATIONS INFORMATION

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER



Dwg. No. A-14,146

FIGURE 1



Dwg. No. A-14,147

FIGURE 2

Three-phase brushless dc motors are especially useful because they have no brushes to make noise, dust, or wear out. The brushes of a conventional motor have been replaced by position sensors, usually Hall effect or optical devices. These sensors detect the rotor position with respect to the stator windings. This information is used to drive the windings in a sequence synchronized with the rotor position, called commutation. To use a three-phase brushless motor usually requires custom ICs to perform the commutation, and discretes for drivers. Then, to control the motor current, and with it speed and torque, requires pulse width modulation circuitry. All this adds up to many components and an expensive solution.

Now, due to progress in integrated power technology, all of the functions needed to drive three phase brushless motors can be performed by one chip. The UDN2936W incorporates Hall effect sensor decoding logic, power outputs capable of driving 2 A continuous at 45 V, PWM current limiting, direction control, dynamic braking, and integrated protection features. This device can be used to provide a simple, inexpensive, and reliable solution to the problem of driving brushless dc motors.

OVERALL CHIP STRUCTURE

The UDN2936W is made up of five sections, namely the commutation logic, output drivers, current limiting, direction and braking, and thermal shutdown. All logic and power functions utilize only bipolar processing, which allows for high power with an efficient use of die area.

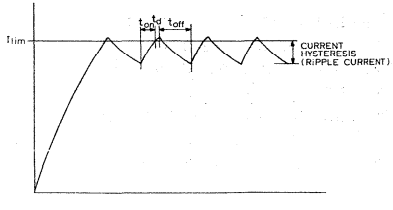
MOTOR COMMUTATION

In a three-phase motor, winding current must be synchronized to rotor position to run the motor efficiently, i.e., with unidirectional torque. Hall effect sensors detect rotor position, which must be decoded to drive the coils in the proper sequence. Hall effect sensors produce low level differential analog outputs. Today's Hall effect ICs amplify this signal to make it easier to use. These Hall effect ICs produce either large signal ac linear waveforms, or open collector digital signals. The UDN2936W is compatible with both types of Hall effect ICs.

Position of the Hall effect sensors determines the decoding sequence to produce the correct driving waveforms for each motor. The decoding sequence programmed into this device is based on Hall effect cells 60 electrical degrees apart. This 60 degree sequence is one of the most common used in the industry. The truth table and timing waveforms found in Figure 1 illustrate how the Hall cell inputs, driving output waveforms, and motor currents states are interrelated. Motors with other commutation sequences can typically be accommodated by inverting one of the position inputs.

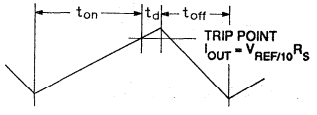
CHOPPING CURRENT CONTROL

The current limit technique chops the source drivers to control the load current level. The maximum current and percentage ripple, or hysteresis, can be programmed by the user or left to internal default values. Source chopping produces a continuous sense voltage (see Figure 2), so this voltage is an accurate representation of load current, even during recirculation. Also, chopping only the sources produces a fast current charge-up and a slower current decay. This occurs because of the different voltages across the coil in both states, and results in a controllable current waveform. The chopping method functions as follows: When the current reaches I_{TRIP}, the source is disabled and the current recirculates through a sink driver and a clamp diode. The motor current decays a fixed percentage, the source is enabled again, and the cycle repeats. The internal sense voltage comparator has a limited bandwidth that essentially filters out noise on the sense pin to prevent erroneous chopping.



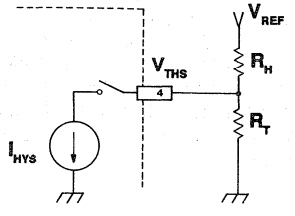
Dwg. No. A-14,148

FIGURE 3A



Dwg. No. A-14,149

FIGURE 3B



Dwg. No. A-14,150

FIGURE 4

The limiting current level and hysteresis are determined by the user or left to internal defaults. Figure 3 illustrates these values in a typical output current waveform. A voltage divider on the V_{REF} pin sets the external V_{REF}. If set above 3 V, the internal V_{REF} is used. Whether V_{REF} is set internally or externally, $V_{REF}/10$ is the trip threshold on V_{SENSE}. The default trip can be programmed by:

$$I_{TRIP} = \frac{0.3\ V}{R_S}$$

Default hysteresis is set at 7.5%. For a V_{REF}<3 V, the trip threshold is the following:

$$I_{TRIP} = \frac{V_{REF}}{10\ R_S}$$

In this case, hysteresis is created by drawing 200 µA from the resistor divider when the sources are chopped, lowering the trip theshold a certain percentage. The sources turn back when the sense voltage decays to the new lower threshold. Hystersis is given by this expression:

$$\%hys = \frac{100\ (200\ \mu A \cdot R_H)}{V_P}$$

The graphs in Figure 5 aid in selecting values for R_H and R_T.

The internal and external current limit settings can be used together to start a motor with a high regulated current, and run it at a lower regulated current. To do this, V_{REF} must be tied above 3 V when the motor starts, and the V_{REF} divider switched in after start-up (see Figure 6).

OUTPUTS

The output section consists of three half-bridges capable of sourcing or sinking 2 A continuously at a saturation voltage of less than 2 V per driver. They are built to sustain at least 45 V. Source and sink clamp diodes are included to provide a current path during commuation and chopping. These are high-performance substrate isolated diodes that virtually eliminate the wasteful parasitic substrate currents of conventional diodes. The drivers, both source and sink, are bipolar double level metal Darlingtons.

DIRECTION AND BRAKING

The direction control allows the motor to be reversed even while running. When direction changes polarity, the state of the outputs is reversed, i.e., if the source was ON, the sink will turn ON, and vice versa. Because the turn off times are longer than the turn on times, the drivers turning ON must be delayed by a precise amount to prevent

potentially destructive crossover currents. This delay is generated internally.

The brake function uses the back EMF of the motor to brake it dynamically. The windings are effectively 'shorted' together through sink drivers and clamp diodes.

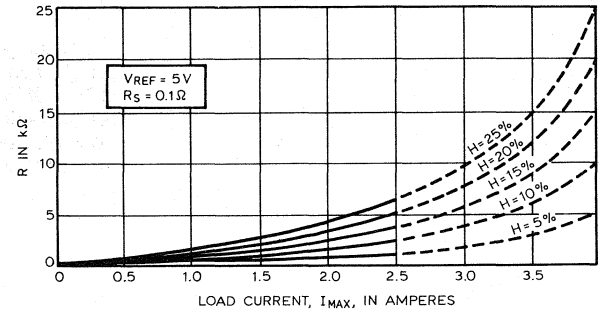
THERMAL SHUTDOWN AND POWER DISSIPATION

The thermal shutdown feature protects the IC from overheating. This circuit turns OFF all drivers at about 165°C, and allows the device to cool down approximately 25° before turning ON again.

The device is packaged in a 12-pin power SIP that has a large copper tab for excellent heat dissipation. The design of the tab, and the fact that it is at ground, make the package easy to use with a heat sink. The maximum allowable power dissipation in 25°C ambient air without a heat sink is 5.2 W. With minimal heat sinking, dissipation greater than 10 W can be accomplished.

APPLICATION

The application shown in Figure 7 is a simple one illustrating the use of the UDN2936W in an open-loop situation with bilevel current limiting. The motor uses digital open-collector Hall cells such as the UGN3113U or linear Hall effect ICs such as the UGN3503U. These Hall effect sensors have a quiescent output voltage of 2.5 V, and emitter follower outputs. The UDN2936W has a regulated internal 2.5 V reference designed to make the inputs compatible with those linear Hall effect sensors. The 5 V supply is also used as a reference in the current limiting for the V_{REF} resistor divider. Choosing R_S = 0.15 ohms results in internal default trip current of 2 A, and 7.5% ripple. This internal limiting is active when Q1 is OFF. R1 and R2 form a resistor divider, when Q1 is ON, to apply 1 V to the V_{REF} input, producing 0.67 A of regulated running current and 5% ripple. Typically, Q1 would be OFF during start-up, giving 2 A of regulated start-up current, and then turned ON to provide 0.67 A of running current. The values of R_1, R_2, and V_{SENSE} can be calculated using the circuit and equations of Figure 5, or the tables of Figure 6.



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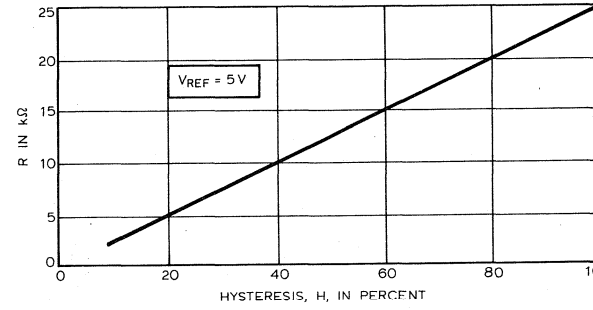
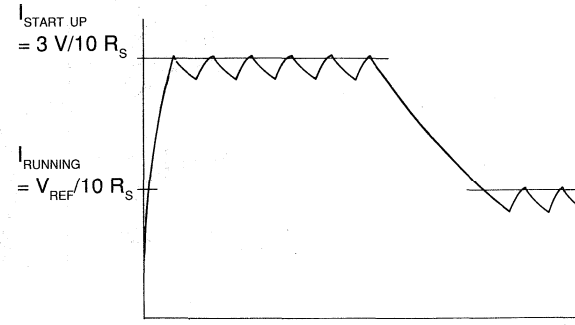


Dwg. No.. A-14,152

FIGURE 5



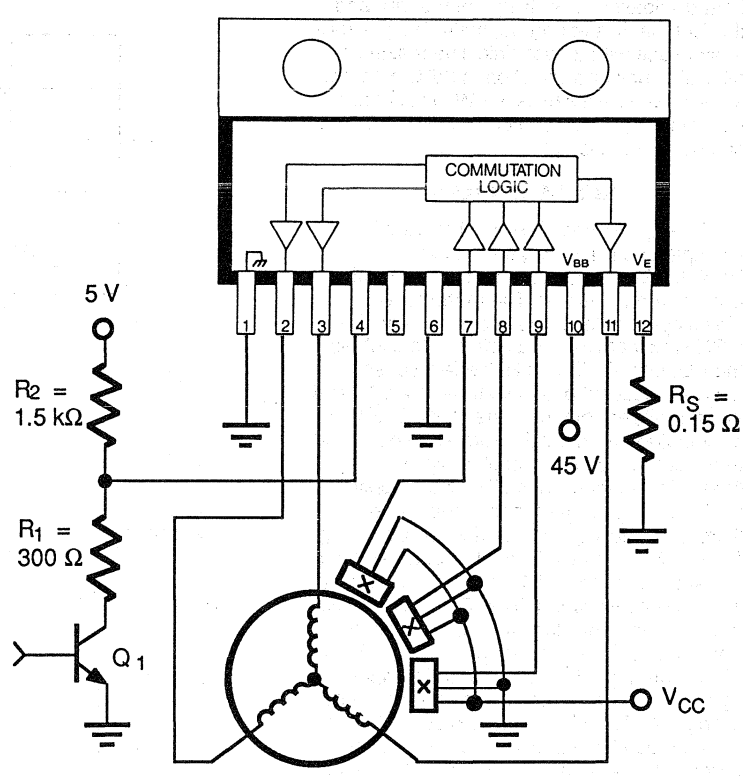
Dwg. No. A-14,153

FIGURE 6

The motor speed is controlled by the current limiting. For a given load, speed is proportional to torque, and torque is proportional to motor current. Subsequently, the motor speed can be controlled through V_{REF}.

CONCLUSION

Smart power integrated circuits have come a long way in the past few years in solving numerous motor driving problems. The UDN2936W is one example of how integrated monolithic devices can replace a drive circuit of many components with one reliable component. Also evident is the fact that bipolar transistors continue to provide economic solutions in the high current application.



Dwg. EP-033

FIGURE 7

APPLICATIONS INFORMATION

POWER OP AMP APPLICATIONS

INTRODUCTION

Monolithic power operational amplifiers meet many high-current design challenges. The Series ULN3750 high-gain, high-current operational amplifiers are used in power-driver applications such as servo-positioning systems (e.g., voice-coil motors for disk drives), dc motors, single-phase and multi-phase motor-drive circuits, linear regulators, and in many other applications that, in the past, have required power buffers driven by conventional operational amplifiers.

Linear motor drivers will inherently produce lower electrical noise levels than their fast-switching digital counterparts. Linear position servos usually achieve substantially higher resolution and are capable of faster response than digitally controlled stepper motors. Series ULN3750 offers increased output-voltage swing and high output-current drive, high gain as well as unity-gain stability and the capability to sense load currents without need of the usual level-shifting or sense circuitry.

The operational amplifiers in this family of ICs provide peak push-pull output currents as high as ±3.5 A, making them suitable for applications in which both current sourcing and current sinking are needed. Illustrated in the examples that follow, some of the op amps allow a very high output swing. They also provide overload and thermal protection under a variety of fault conditions.

Attention to thermal design in IC layout has minimized temperature-induced degradation of parameters while maximizing output-power capability. Single power op amp drivers are furnished in power-tab TO-220 packages (ULN3751Z). Dual units are supplied in 12-pin single in-line packages (ULN3755W) and in low-cost standard DIPs with heat-sink tabs (ULN3755B).

BRUTE FORCE AND SMALL SIGNALS

Both classical small-signal op amps and brute-force boosters must possess two attributes: they must have true differential (inverting and noninverting) inputs. Second, to minimize errors and drifts in closed-loop configurations, they must have high open-loop gain. Frosting-on-the-cake includes low offset voltage and drift, unity-gain stability, high output swing, large common-mode input range, high common-mode rejection, short-circuit protection, and a thermal-shutdown feature.

The Series ULN3750 offers all these features, and more. Consider the input section. The circuit is a classic op amp input stage found, for example, in many operational amplifiers with little power-handling capacity. The use of PNP input transistors allows the application of input voltages ranging from about 0.5 V below ground to approximately three base-emitter drops below the positive supply voltage. The ability to use ground-level input voltages is an important consideration. It allows the op amp to be easily operated from a single supply, where the input source is often referenced to ground.

The two capacitors shown in the input-circuit schematic provide compensation with adequate phase-gain margins to allow operation for closed-loop gains as low as 1. Note the graph of the amplifier's gain and phase characteristics as functions of frequency (noninverting test circuit, A_V = 1000). It exhibits a smooth, 6 dB per octave rolloff to frequencies as high as 1 MHz, and an approximate 20° phase margin at unity gain.

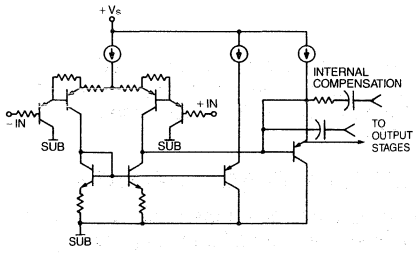
In the amplifier's output stage, the output transistors are completely protected from inductive kickback voltages by clamping diodes built into the chip. The clamp diodes are capable of handling currents equal to the rated capacity of the output sink/source transistors. The output transistors are connected in a quasi-complementary configuration. The

SERIES ULN3750 POWER OP AMPS

Device	Type	Peak Current Output	Short-Circuit Protection	Thermal Protect	Boost Voltage	Compensation	Functional Supply Span	Package
ULN3751Z	Single	3.5 A	—	Yes	—	Internal	6 V to 30 V	5-Pin TO-220 Power-Tab SIP
ULN3755W	Dual	3.5 A	Yes	Yes	Yes	Internal	6 V to 40 V	12-Pin Power-Tab SIP
ULN3755B	Dual	3.5 A	Yes	Yes	Yes	Internal	6 V to 30 V	16-Pin Batwing DIP

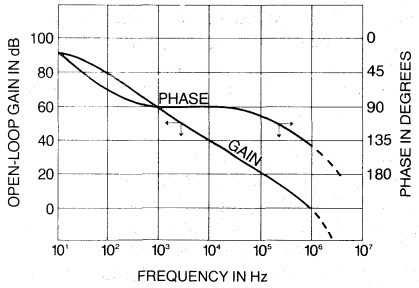
Some of the material appearing in this application note, is taken from an article that appeared in the August 22, 1985 issue of EDN magazine

INPUT STAGE



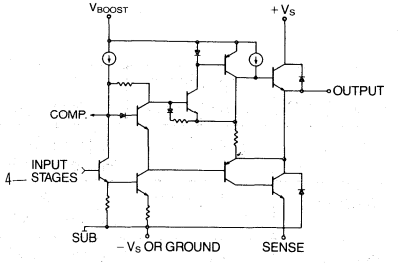
Dwg. No. W-115

GAIN AND PHASE CHARACTERISTICS



Dwg. No. W-116

OUTPUT STAGE



Dwg. No. W-117

lower sink transistor can provide output voltages as low as ground plus one saturation drop. The current-sense terminals can be used to impart a transconductance characteristic to the amplifier, or simply to provide a separate power output ground and minimize output-to-input feedback through a common ground resistance.

BOOST TO BOOTSTRAP

The boost terminal is a unique feature of the ULN3755B and ULN3755W. It increases the amplifier's available output-voltage swing by 1 V to 2 V, depending on output current, by allowing the upper source transistor to saturate (an impossibility with the usual emitter-follower lacking the boost feature). To take advantage of the boost capability, use a boost-terminal voltage that is about 3 V higher than the positive load supply voltage. The boost function allows the amplifier to be bootstrapped in ac applications by its own output or by another ac output.

The specifications shown for the ULN3755W apply to operation with ±6 V supplies, at an ambient temperature of +25°C. Not shown are the amplifier's absolute maximum ratings: 40 V supply span, ±3.5 A peak repetitive current, and 20 W allowable package power dissipation (with 3°C/W heat sink and +25°C ambient).

The Series ULN3750 currently is comprised of three types. Considering allowable package power dissipation ratings, continuous output currents to ±1 A are recommended for the 16-pin batwing DIPs (suffix "B"). Applications with ratings to ±2.5 A require the TO-220 or 12-pin single in-line power tab packages (suffix "Z" and "W" respectively). All devices provide thermal shutdown at high junction temperatures. All are unity-gain stable. Pin count essentially dictates the features available with the various units.

CAREFUL THERMAL DESIGN WRINGS WATTS FROM ICs

Power ICs are now capable of delivering tens of watts of power. It is easy to obtain such power from an IC when the device is mounted in a metal can with low thermal resistance. Moreover, it is easy to provide heat sinking for such a package. Metal packages, however, are expensive. The challenge is to develop inexpensive plastic packaging that also provides a way to keep junction temperatures at a safe level.

What's a safe level? At the moment, the prevailing industry standard for maximum junction temperature is +150°C. However, using any temperature as a reference, an IC's expected lifetime roughly doubles for every 10°C reduction in junction temperature. Note, too, that such circuit parameters as leakage current suffer significant degradation at high temperatures.

The most widely accepted IC package is the dual in-line package (DIP). Without special enhancements, though, the standard DIP is woefully inefficient for thermal transfer. The package itself provides a junction- to-ambient thermal resistance as high as 125°C/W. This figure assumes the use of a Kovar lead frame and, since the lead frame is the main carrier of heat from the IC to the outside world, changing the material to copper reduces the thermal resistance to about 60°C/W. All power operational amplifiers have copper lead frames and heat sinks.

POWER OP AMP APPLICATIONS

ULN3755W DUAL POWER OP AMP TYPICAL ELECTRICAL CHARACTERISTICS, T_A = +25°C, $T_J \leq$ +150°C, + V_S = V_{BOOST} = +6 V, - V_S = -6 V (unless otherwise specified).

Characteristic		Test Conditions*	Typical Value
Quiescent Current	$+I_S$	No Load	70 mA
	I_{BOOST}	V_{BOOST} = 9 V, No Load	7.0 mA
Input Offset Voltage		V_{OUT} = 0 V, No Load	2.0 mV
Input Bias Current		V_{OUT} = 0 V	80 nA
Input Offset Current		V_{OUT} = 0 V, No Load	10 nA
Open-Loop DC Gain		f = 0 Hz	100 dB
Slew Rate		V_{IN} = 0.2 V Step	1.0 V/µs
Output Swing		V_{BOOST} = 6 V, I_{OUT} = ±1 A	9.5 Vpp
		V_{BOOST} = 9 V, I_{OUT} = ±1 A	10.5 Vpp
Power-Supply Rejection		Either Supply	80 dB
Common-Mode Rejection			85 dB

Limiting the junction temperature to +150°C, the 60°C/W figure allows a worst-case (still air) package power dissipation of 1.33 W at +70°C. Unfortunately, this power figure is still inadequate for many modern power applications.

HIGH-POWER SIPs

For high-power applications, power ICs use single in-line packages similar to the TO-220, universally used for power transistors. The 5-pin ULN3751Z uses such a package. Its maximum junction-to-tab thermal resistance is 4.0°C/W. The ULN3755W dual power op amp is housed in a similar, but wider, package. Exhibiting 3°C/W maximum junction-to-tab thermal resistance, the IC can dissipate as much as 26 W at a tab temperature of +70°C.

ISOTHERMAL DESIGN CUTS GRADIENTS

Chip temperatures inevitably rise in high-power applications. Even with ideal packaging, the thermal resistance of the silicon chip itself will result in a temperature gradient across the chip. In linear circuits such as these op amps, the worst effects can arise from unequal heating on the chip's surface.

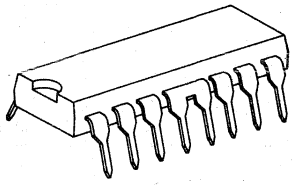
It is important to position input transistors as far as possible from the heat-generating output devices. What is less obvious is the need to arrange the high-gain input stages so as to minimize the effects of any temperature differences between them. For example, unequal junction temperatures in the amplifier's input transistors can cause large offset-voltage and offset-current shifts.

As shown in the chip drawing and schematic, cross-coupling of the input stages cancels differences in the low-level transistors' junction temperatures. It is also necessary to lay out the stage's associated resistors to minimize temperature gradients. In this case, all input-stage resistors are arranged in the same epitaxial tub (and in the same direction) to ensure that all resistors are equally affected by the unavoidable heating.

A CASE STUDY

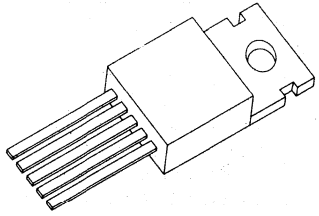
Note the isothermal lines shown in the chip drawing. Q_{25} and Q_{26} are at equal temperatures; these two current-mirror transistors must have the same base-emitter voltages. It's a different story, however, for Q_{21} and Q_{22}. They lie farther away from the power section, and layout considerations have made it impossible to keep them at equal temperatures. The same problem also exists for Q_{20} and Q_{23}. For the purposes of illustration, assume that a dissipation-induced temperature rise causes the base-emitter voltage of Q_{25} and Q_{26} to drop by 3 mV. Transistor Q_{22} is slightly cooler and suffers a V_{BE} decrease of 2 mV while the comparable Q_{21} drop is only 1.5 mV. Finally, Q_{20} and Q_{23} exhibit V_{BE} changes of 1 mV and 0.5 mV, respectively. As a result of thermal cross-coupling, the V_{BE} reductions from either input can be matched at 2.5 mV. The base-emitter voltage variations as a function of temperature thus cancel out. Without this cross-coupling, the total change in base-emitter voltage would be 3 mV for the left input stage and 2 mV for the right input stage.

16-PIN BATWING 'B' PACKAGE



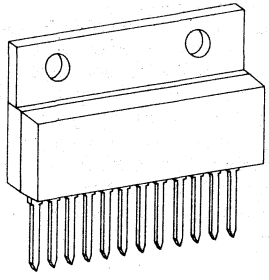
Dwg. No. W-167

5-PIN TO-220 'Z' PACKAGE



Dwg. No. W-113

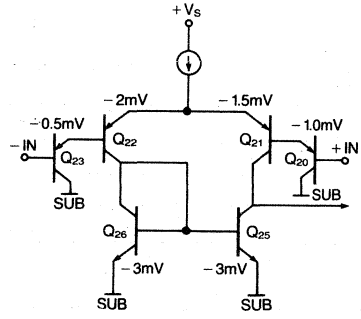
12-PIN SINGLE IN-LINE 'W' PACKAGE



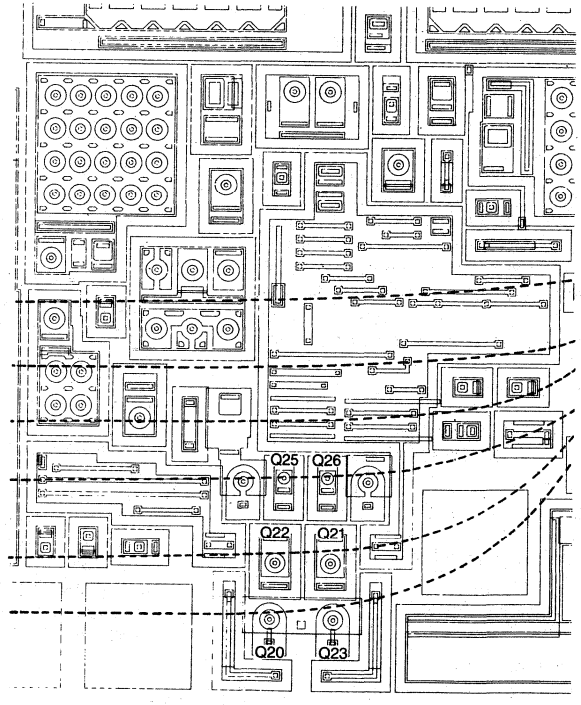
Dwg. No. W-114

ISOTHERMAL DESIGN

CHANGES IN V_{BE} WITH TEMPERATURE



Dwg. No. W-118



Dwg. No. W-168

POWER OP AMP APPLICATIONS

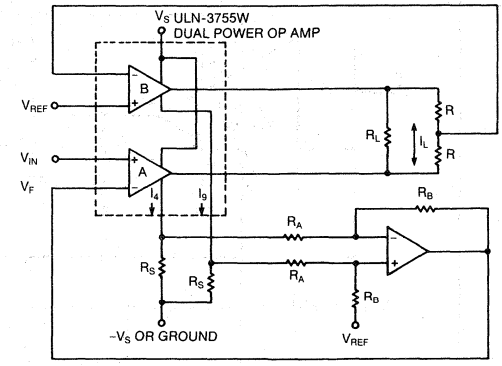
CURRENT-SENSE TRANSCONDUCTANCE

The op amps' current-sense terminals can be used to derive a transconductance function. This function is commonly used in motor control applications such as voice-coil servo or microstepping positioning systems found in many computer disk drives. The drawing at right shows the ULN3755W dual amplifier connected as a transconductance amplifier. In this example, amplifier B is used as a slave to amplifier A. Feedback from the pair of current-sensing resistors, R_S, in the emitters of the output's current-sinking transistors is applied to the summing network and scaled to the inverting input of amplifier A, where it is compared to the input voltage.

The voltage developed across the sensing resistors is directly proportional to the output current. Using this voltage as a feedback source defines the gain of the circuit as output current in amperes as a function of the input voltage in volts. The gain thus assumes the dimensions of a transconductance function (output current divided by input voltage), expressed in siemens (formerly mhos).

Conventional monolithic power op amps can be made to operate in similar configurations where the current-sensing resistor(s) are inserted in the ground (or negative supply) return. However, that configuration is not recommended, since both the amplifier's signal and bias currents now flow through the output current sensing resistor(s), causing the high-gain signal ground to float. Operating in this mode can cause problems with stability and common-mode rejection, as well as reducing the input common-mode range. The dual power op amps in the Series ULN3750, however, provide open-emitter outputs that can be used to sense current without degradation of the input characteristics of the high-gain stages.

TRANSCONDUCTANCE AMPLIFIER



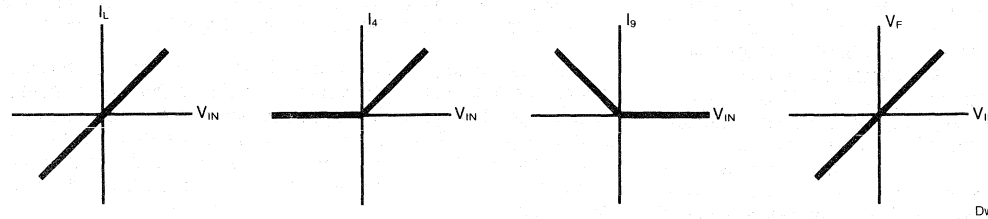
Dwg. No. W-119

The graphs below illustrate the bidirectional nature of output load current (and the same current divided between the two output sink returns).

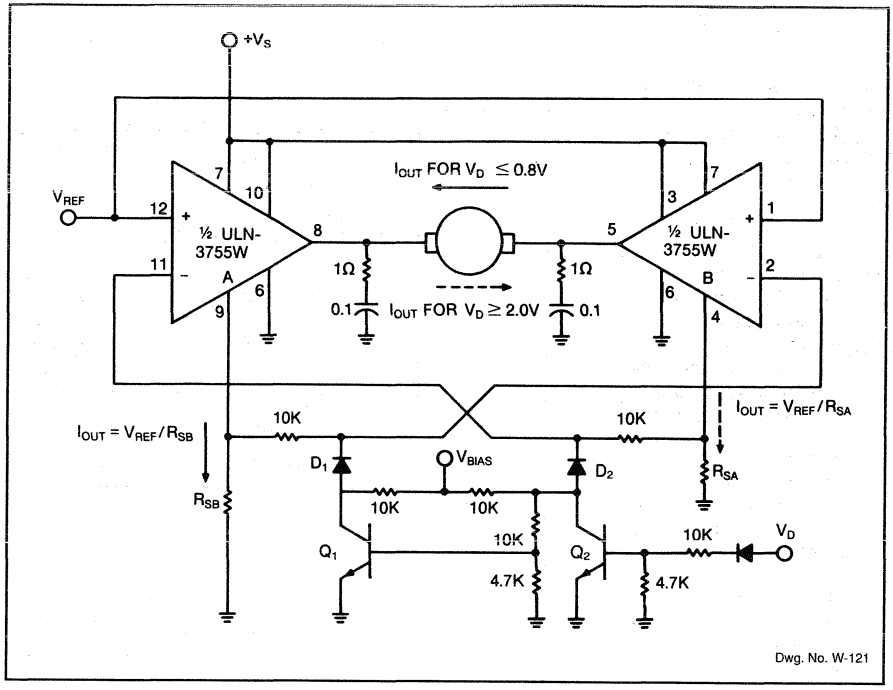
$I_4 - I_9 = I_L$. The external network sums and amplifies (scales) the voltages developed across the current-sensing resistors. The resulting feedback voltage (V_F) is a scaled, level-shifted version of the load current. It is possible, in certain applications, to combine this network with the input-feedback network and eliminate the small-signal operational amplifier. The negative feedback forces the amplifier to adjust the output current to attain a value such that the feedback voltage equals the applied input voltage. The transfer function of the transconductance amplifier is approximately:

$$I_L/(V_{IN} - V_{REF}) = R_A/(R_B R_S)$$

Resistors R_A, R_B, and R_S define the transconductance gain. To avoid limiting the transconductance amplifier's output compliance (swing capability), low-value current-sensing resistors (R_S) should be used. The product of peak output current and sensing resistance should be kept to as low a value as possible.



Dwg. No. W-120



BIDIRECTIONAL CURRENT CONTROLLER

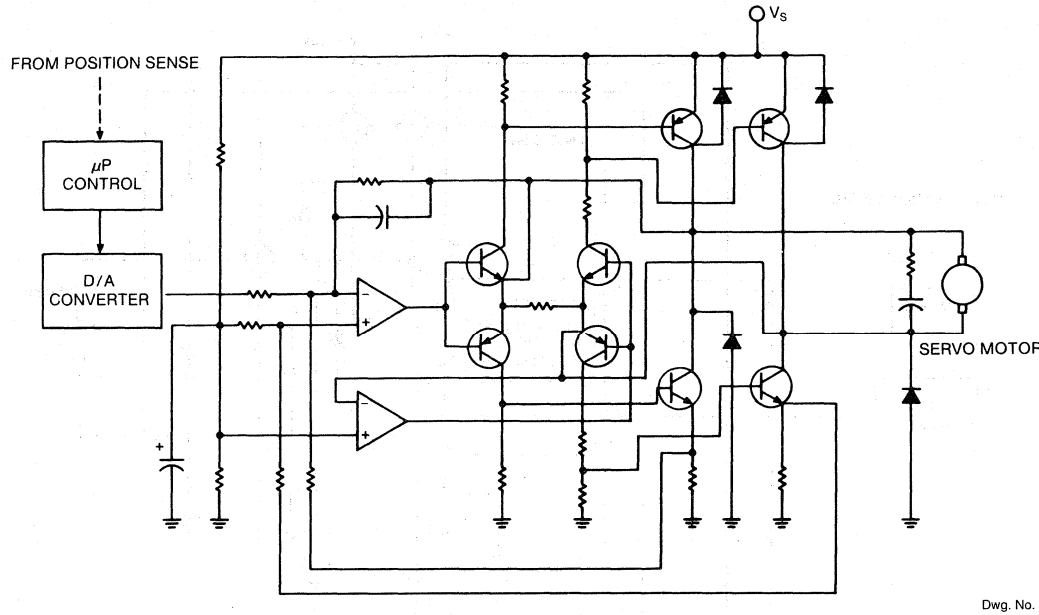
There are many applications requiring constant current sources that can be controlled both in magnitude and direction. Examples of this requirement are found in some brushless dc motor drives as well as in numerous industrial process control systems. Both open-loop and closed-loop feedback systems are used depending on the specific requirements to be met. In any case, there exists a voltage directly proportional to the desired output current and a control signal or switch whose state determines direction.

The circuit above is a bidirectional transconductance amplifier. A voltage, proportional to the desired current, is applied to both non-inverting inputs of a ULN3755W, which is connected in a bridge configuration. Current feedback is obtained from current-sense resistors (R_{SA} and R_{SB}). The voltage developed across the current-sense resistor is directly proportional to the load current. This sense voltage is applied to the inverting inputs of the amplifiers, as shown, to provide negative feedback. The output will adjust until the feedback voltage is equal to the programmed input voltage. This can be expanded to a switched selector network or the output of a servo-control loop.

The direction of the load current is controlled by a positive bias voltage applied to either of the inverting inputs. V_D represents the digital direction-control voltage. When V_D is low, Q_2 is OFF, allowing D_2 to conduct, driving pin 11 high. This causes the output of amplifier A to be driven low. Q_1 meanwhile, is ON, clamping the anode of D_1 to ground (or to the saturation voltage of Q_1). This results in D_1 being held OFF and allowing active feedback to pin 2 of amplifier B. Amplifier B will then source current into the load with amplifier A acting as a current sink. By raising V_D to a high level, the output of amplifier B will go low, with amplifier A acting as the controlled current source. Resistor values are non-critical except to ensure that the inverting input of the switched amplifier is held above the programming voltage (V_{REF}) applied to its non-inverting input. As shown, control voltage V_D is TTL compatible.

If V_D is the output of a pulse generator, this application will produce a time-dependent current reversal. This meets the requirements found, for example, in a typical industrial process control application where a current is passed through a pair of electrodes immersed in a conducting fluid. Alternatively, Q_2 and its drive can be replaced by a latching Hall Effect switch for use in brushless dc motor applications where current is controlled by R_S.

DISCRETE CIRCUIT IMPLEMENTATION



DIGITALLY CONTROLLED POSITION SERVO

In a position-control application, a microprocessor is often used to control a servomotor's shaft angle or to control position, as in a computer disk drive. Shown is a typical discrete semiconductor circuit implementation of that concept. The basic configuration is a classic one, using two low-power operational amplifiers, many discrete passive components, and four PNP and NPN power transistors connected in a push-pull, H-bridge configuration.

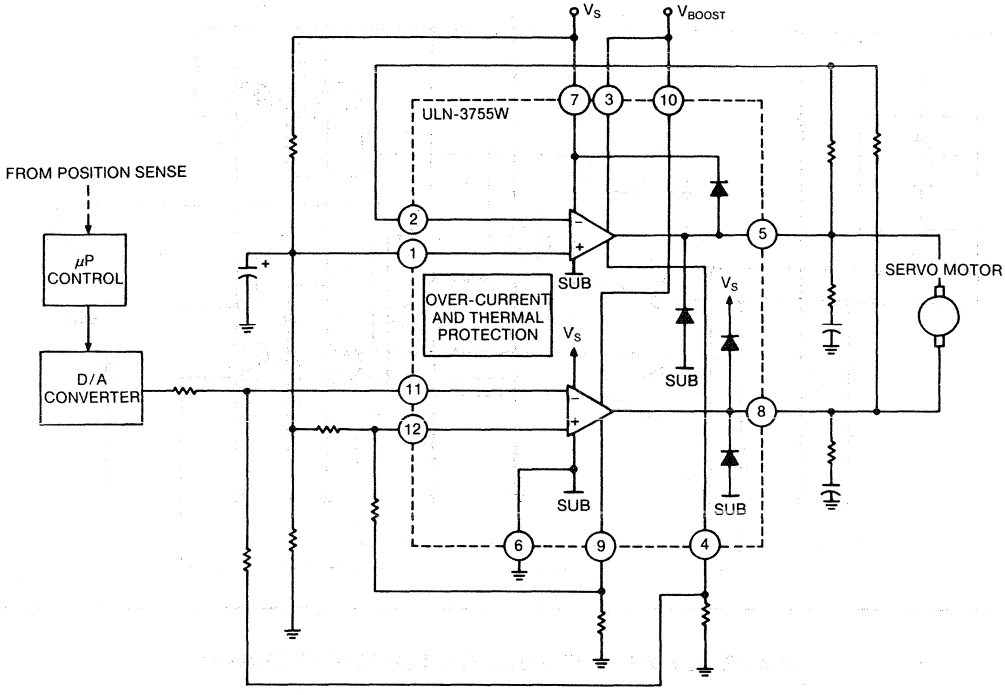
The circuit consists of small-signal input operational amplifiers and power output stages. The circuit derives its input from the D/A converter, whose output is determined by a code from the controlling microprocessor and related digital-control circuitry.

The analog equivalent of this servo-control circuit might use a multi-turn potentiometer to produce a voltage proportional to the servomotor's position. In any event, the sensed position signal normally undergoes processing and comparison with the desired position, through a digitally-based microprocessor system (or its analog equivalent) that produces an error signal to control the servo amplifier's output.

A circuit that uses far fewer components to accomplish the same position-control function is constructed around the ULN3755W integrated circuit. In addition to the original functions, the circuit now includes thermal and short-circuit protection, as well as component matching and thermal tracking inherent to monolithic construction. The ULN3755W dual power operational amplifier has its two independent outputs connected in a push-pull, H-bridge configuration. An 8-bit D/A converter yields a resolution of 256 shaft positions in discrete steps of 1.41°. A higher resolution converter would, of course, provide finer control. Because of its push-pull arrangement, the circuit provides bidirectional servo control.

The overall resolution of the system is a function of the position-sensing element, whether a digitally encoded disk or an analog potentiometer, and the digital control circuitry, including the microprocessor and the A/D converter. The ULN3755W dual operational amplifier combines the small-signal summing amplifiers, predrivers, and the output H-bridge. The IC's outputs also include clamping diodes with current-handling capacity equal to that of the output drivers.

DIGITALLY CONTROLLED POSITION SERVO— INTEGRATED CIRCUIT IMPLEMENTATION



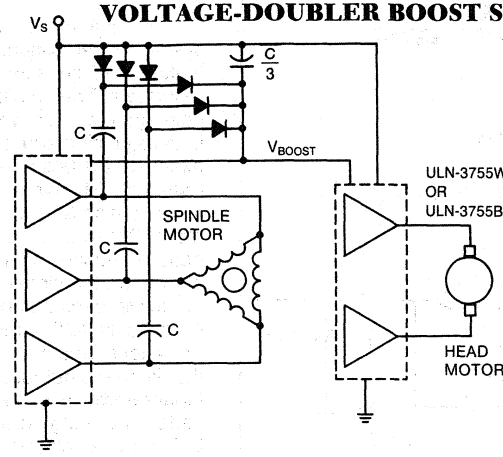
The current-sense pins (4 and 9) provide access to the emitters of the H-bridge current sinks, thereby providing convenient output-current sensing to ground (or to the negative rail), while allowing separate low-current signal ground returns. This feature helps to prevent undesirable feedback to the input stage, a common problem with conventional approaches to output-current sense.

If a voltage higher than the supply is applied to the ULN3755W boost pins, the positive output swing is limited only by the saturation resistance of the output transistors (typically less than 0.5 Ω). For example, with a 12 V supply, the circuit typically supplies a 10.5 Vpp output swing at 1 A output current. This figure is at least 1 V higher than can be expected from ICs lacking the boost capability. Note that the externally supplied boost voltage should be at least 3 V higher than the load supply voltage. This criterion satisfied, the boost voltage can be any value within the IC's 40 V absolute-maximum rating. The circuit shown will deliver continuous output currents of up to ±2.5 A and peak output currents as high as ±3.5 A.

The user must be aware that although the voltage or current limits shown are well within the IC's capabilities, the resultant power dissipation must be kept within the constraints of the overall (chip + package + heatsink) thermal rating. This rating is principally dependent on the package chosen and the amount of heat sinking provided by the user.

The boost feature provides important additional output voltage swing at the amplifier's full rated current. However, the IC's boost input requires only a low, unregulated current of 25 mA, maximum. Thanks to this modest current requirement, the boost voltage can be obtained from such compact sources as inexpensive, modular dc to dc converters. Or, in a head-positioning application in a disk drive, for example, a simple overwinding in the spindle motor (or a voltage doubler using the motor's driven phases) can easily generate such a voltage.

VOLTAGE-DOUBLER BOOST SUPPLY



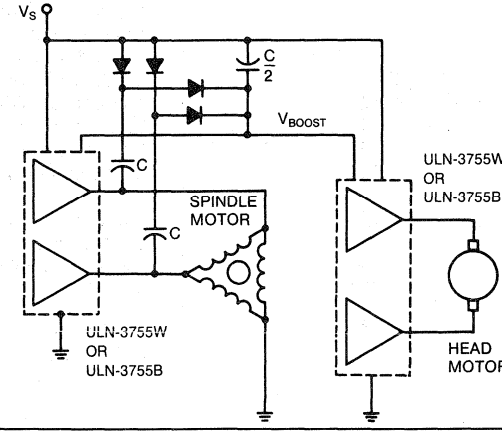
Dwg. No. W-125

SIMPLE VOLTAGE DOUBLERS FOR OP AMP BOOST

An example of a simple-to-implement voltage-doubler boost supply is shown above. This circuit affects the doubling by connecting a series diodecapacitor network between the main supply and each of the spindle motor's driven phases. A three-diode bridge then charges the voltage-doubling capacitor to nearly twice the main supply voltage. Note that connecting the capacitor to the main supply (instead of to ground) effectively reduces rms ripple in the main supply by injecting its charge current into the supply mains concurrently with the spindle's opposing drive currents. Although, in theory, only one motor phase is needed to generate the boost, the three-phase connection is recommended to prevent unbalancing the spindle.

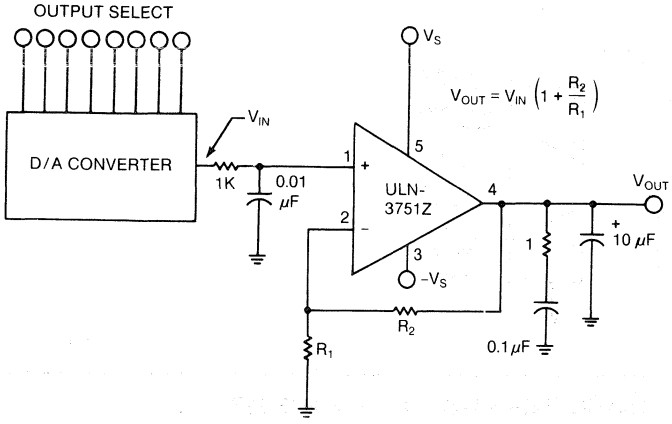
Below is a similar circuit using a ULN3755W to provide linear drive to a delta-connected spindle motor. The use of linear drive instead of pulse-width-modulation results in much lower noise with only a slight reduction in efficiency. Because fast PWM transitions in the circuit above result in motor losses, the efficiency compromise of the linear configuration is not as significant as might be expected.

VOLTAGE-DOUBLER BOOST SUPPLY WITH LINEAR DRIVE



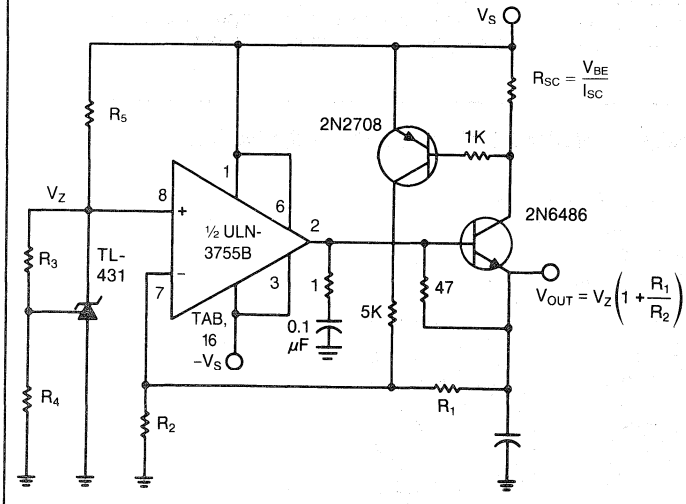
Dwg. No. W-124

POSITIVE-OUTPUT PROGRAMMABLE REGULATOR



Dwg. No. W-126

POSITIVE-OUTPUT REGULATOR WITH SHORT-CIRCUIT LIMITING



Dwg. No. W-127

HIGH-CURRENT REGULATORS

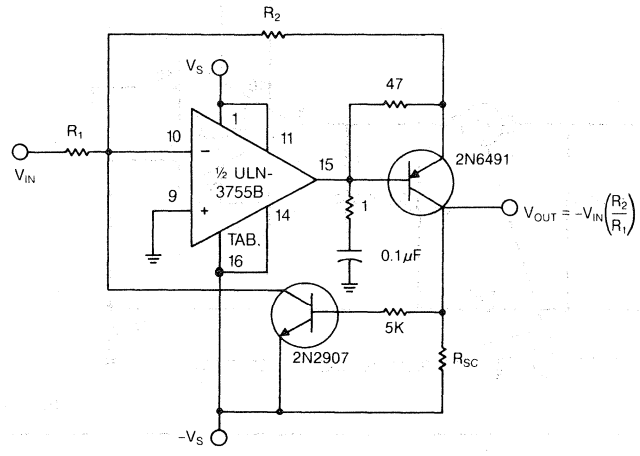
The high current-output capability of the operational amplifiers in Series ULN3750 makes them suitable for use in linear voltage regulators. The amplifiers' high open-loop gain and low offset voltage ensure high load regulation and accuracy. Consider, for example, the positive-output, programmable regulator . The circuit provides output currents as high as ±3.5 A peak. Unlike most monolithic regulators, the ULN3751Z is equally effective as a sink or a source. Therefore, the circuit maintains regulation for active loads that present reversing load currents. Note that the circuit easily handles transitions from high to low output voltages, thanks to the output's sinking capability. The input reference is the output of a D/A converter, providing programmability. An 8-bit D/A, for example, provides for 256 steps of output resolution.

For higher output currents (but without the sink capability) the addition of an external power transistor provides outputs as high as the NPN power transistor's safe operating area allows. This circuit is shown using a voltage reference such as the popular three-terminal TL431. The voltage V_Z is determined by the ratio of resistors R_3 and R_4, while R_5 provides bias current. The circuit can, of course, be programmed by substituting the D/A reference above. The amplifier's output voltage is a function of the ratios of R_1 and R_2. The PNP transistor provides short-circuit (I_{SC}) current limiting according to the expression shown.

To configure a high-current, dual-output supply, a mirror-image circuit can be used. Simply connect this stage's input to the D/A converter or voltage reference output. The combination of this circuit and the positive output regulator provides an accurately tracking pair of positive and negative supplies from a common reference, whether a programmable D/A converter or the simple resistor-programmed TL431. Both circuits use the ULN3755B with external high-current pass transistors. The external devices are unnecessary if output-current loading is less than 2.5 A.

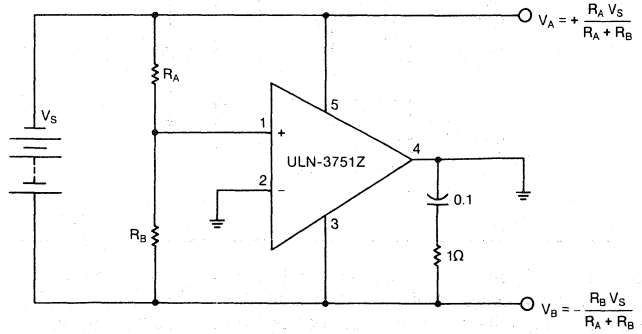
The previously described boost capability can be used to good advantage in these regulator circuits. Applying a low-current boost voltage at least 3 V higher than the

HIGH-CURRENT NEGATIVE OUTPUT REGULATOR



Dwg. No. W-128

ARTIFICIAL GROUND/SPLIT SUPPLY



Dwg. No. W-129

load supply voltage results in a regulator with less than 1 V input-output differential, (dependent on output current) yielding high efficiency from the main supply. The 0.1 Ω/0.1 μF network at the amplifier's output provides local compensation for the output stage.

A simple split supply can also be developed using a single ULN3751Z power op amp to generate an artificial ground, as shown below. By taking advantage of the device's four-quadrant sink/source drive capability, the outputs will ratio (rather than track) over a wide range of supply voltages and unequal load currents. *Total* load current is unrestricted, provided the *difference* in load currents is less than the maximum rated current of the power op amp. In addition, the allowable package power dissipation rating must be greater than the product of the amplifier's sourcing current ($I_A < I_B$) and the source driver voltage (V_A) or sinking current ($I_A > I_B$) and the sink driver voltage (V_B). This circuit is also very useful in tracking supplies to enhance common-mode supply rejection.

ICs CONTROL MOTOR SPEED

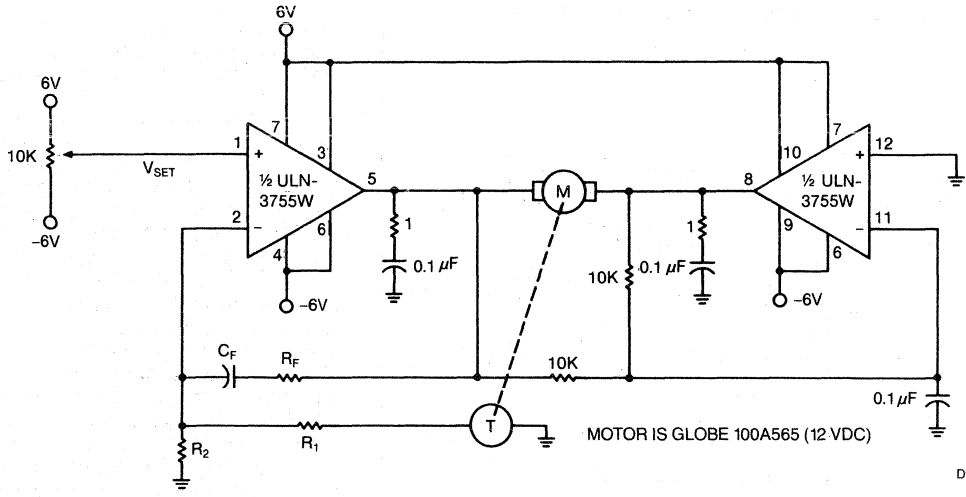
Power op amps can be used to provide accurate speed control for dc motors. The drawing shows a closed-loop system for controlling the speed of a 12 V dc motor. The circuit provides bidirectional speed control. The amplifiers' push-pull configuration ensures a full rail-to-rail voltage swing (minus the output stages' saturation drops) across the motor in either direction.

The circuit uses a mechanically-coupled tachometer to provide speed-stabilizing feedback to the first amplifier section. The motor's speed and direction of rotation is set by adjusting the 10 kΩ potentiometer at the amplifier's noninverting input. The motor speed, in rpm, is:

$$S = V_{SET}(R_1 + R_2)/0.0027\ R_2$$

The R_FC_F feedback network prevents oscillation by compensating for the inherent dynamic mechanical lag of the motor. Select the R_FC_F time constant to match the particular motor's characteristics. By consulting with individual motor data sheets, the R_F and C_F values can be chosen to match the motor response or dynamic time constant. This should yield a good starting point for stabilizing the system. Optimal response is achieved by varying the compensating capacitor.

DC MOTOR SPEED CONTROL



Dwg. No. W-130

N-PHASE MOTOR DRIVE

Its high amplification factor and its built-in power-output stage make the integrated power operational amplifier a convenient driver for single-phase or multiphase ac motors. The high gain allows one op amp to be configured as an oscillator to generate the required ac signal. The power-output stage, of course, supplies the high-current drive to the motor.

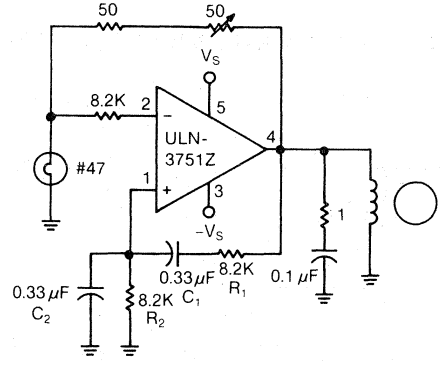
Consider, for example, the three motor-drive circuits shown here. The first circuit is a single-phase driver that uses the ULN3751Z single power op amp. The other circuits use the ULN3755W dual amplifier to drive two-phase and three-phase motors. Note that in all three circuits, the controlling op amp is configured as a Wein-bridge power oscillator. The R_1C_1 and R_2C_2 feedback networks determine the oscillation frequency according to the expression:

$$f_O = 1/(2\pi\sqrt{R_1R_2C_1C_2})$$

By varying either R_1, or R_2, the oscillator frequency can be adjusted over a narrow range.

In the single-phase and two-phase examples, the oscillation frequency is 60 Hz. In the three-phase example, the frequency is

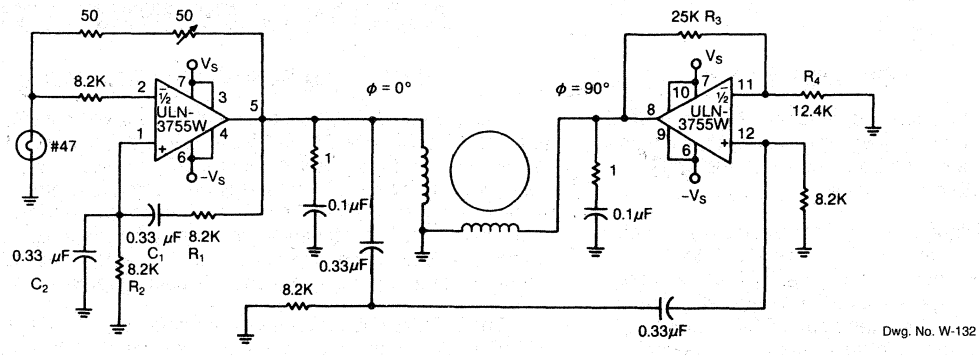
SINGLE-PHASE AC MOTOR DRIVER



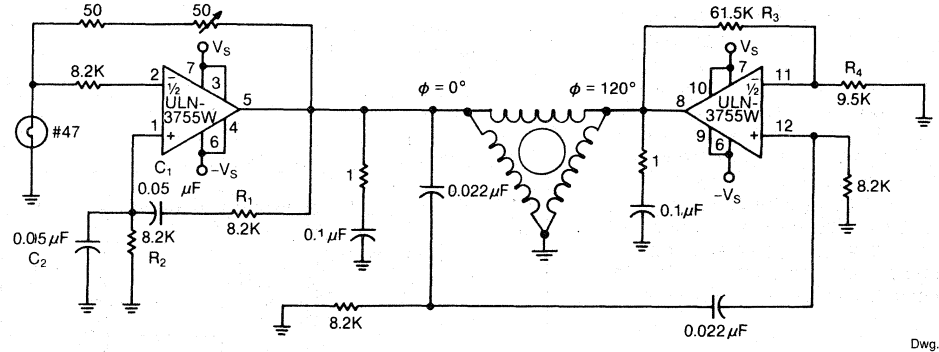
Dwg. No. W-131

400 Hz. The Type 47 incandescent light bulb in the oscillator circuits serve to stabilize the amplifier's output amplitude. The bulb owes its stabilization qualities to its intrinsic positive temperature coefficient. If the amplifier's output level attempts to increase, the corresponding increase in lamp current causes a temperature rise in the filament. The heating, in turn, results in an increase in filament resistance, producing increased negative feedback and a reduction in amplifier gain. A PTC (positive temperature coefficient) resistor could be used instead of the lamp. To set the output amplitude, adjust the 50 Ω potentiometer in the feedback network.

TWO-PHASE AC MOTOR DRIVER



THREE-PHASE AC MOTOR DRIVER



To drive multiphase motors, it's a relatively simple matter to add another stage to the single-phase circuit. In the 60 Hz, two-phase drive, the 8.2 kΩ/0.33 μF networks provide both the 60 Hz oscillator frequency and the 90° phase shift needed by the right-hand amplifier. The 8.2 kΩ/0.005 μF networks in the three-phase drive set the 400 Hz oscillator frequency, while the 8.2 kΩ/0.022 μF networks provide the required 120° of phase shift. The motor shown is a three-phase delta-connected motor with one input grounded and the remaining inputs driven from the 0° and 120° phase-shifted amplifier outputs. The result is a balanced three-phase ac drive.

In both the two-phase and three-phase circuits, the R_3/R_4 ratio sets the second amplifier's gain to compensate for signal attenuation occurring in the phase shifters. Again, pins 3 and 10 can be returned to a boost supply to obtain additional output-swing capability.

The three circuits can all be driven from an external source, such as a pulse or square wave output of a digital source, setting the gain of the left-hand amplifier to a level less than that required for oscillation. The RC feedback networks then function as active filters, causing the outputs to be sinusoidal.

UNIVERSAL BUILDING BLOCKS

Power operational amplifiers provide a fundamental set of universal building blocks incorporating the merged equivalent of small-signal operational amplifiers, pre-drivers, output amplifiers and various protective features such as output clamp diodes, thermal shutdown, and output-current limiting. An output-boost capability can provide for high output-voltage swing, while an output-current-sensing scheme prevents unwanted interaction between the outputs and inputs. Many applications that previously required individual low-level and high-level components can now be implemented with a single integrated circuit and few external components.

APPLICATIONS INFORMATION

SERIES 5800
BiMOS II POWER DRIVERS

INTRODUCTION

The second generation of merged CMOS/bipolar integrated circuits extends the lead in innovative interface forged by the original BiMOS power drivers.

Higher-density CMOS logic gives BiMOS II integrated circuits improved switching speeds at reduced costs. With a 5 V supply, second generation BiMOS typically operates at data input rates above 5 MHz; at 12 V, significantly higher speeds are obtainable. The BiMOS II series also offers new and improved functions.

Reliable, single-chip BiMOS II solutions are available for a wide variety of peripheral and power interface problems. Two or more devices are no longer required to interface low-level (TTL, CMOS, NMOS, PMOS) LSI or microprocessor functions with power loads such as LEDs, gas-discharge or vacuum-fluorescent displays, relays, solenoids, thermal printers, motors, impact printer hammers, and incandescent lamps. Since all BiMOS devices include logic and control in addition to power functions, they also free the microprocessor from many housekeeping tasks.

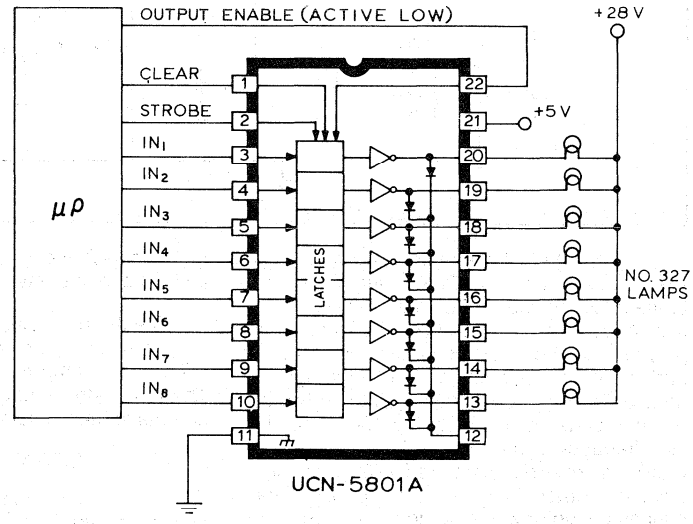
INCANDESCENT LAMP DRIVERS

Each of the UCN5800A or UCN5801A open-collector Darlington outputs will sink up to 500 mA and will sustain at least 50 V in the OFF state. The high peak current rating of these devices allows their use with the high inrush (10 x) currents normally associated with incandescent lamps. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximun current: Either a reduction in output current or a suitable combination of duty cycle and number of active outputs is usually required.

The UCN5800A is supplied in a standard 14-lead DIP. The UCN5801A is furnished in a 22-lead DIP with 0.400" row spacing.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	**45 V**
Logic Supply Voltage Range	**5.0 V to 12 V**
Continuous Output Current	**350 mA**



Dwg. No. A-12,550

PLANAR GAS-DISCHARGE DISPLAY DRIVERS

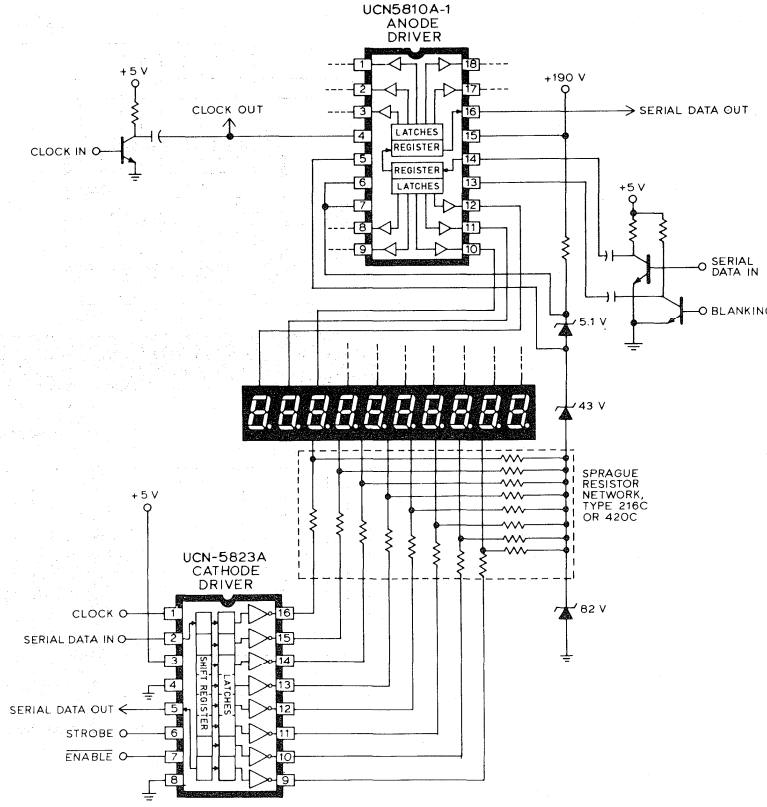
Combining the high-voltage UCN5810A-1, UCN5812A-1 or UCN5818A-1 serial-input, latched source driver with the UCN5823A serial-input, latched sink driver provides a simple way to drive multiplexed high-voltage planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN5810A-1, UCN5812A-1, UCN5818A-1 . . . . . **75 V**
- UCN5823A . . . . . **95 V**

Logic Supply Voltage Range . . . . . **5.0 V to 12 V**

Continuous Output Current
- UCN5810A-1, UCN5812A-1, UCN5818A-1 . . . . . **-25 mA**
- UCN5823A . . . . . **350 mA**



Dwg. No. C-1275

VACUUM-FLUORESCENT DISPLAY DRIVERS

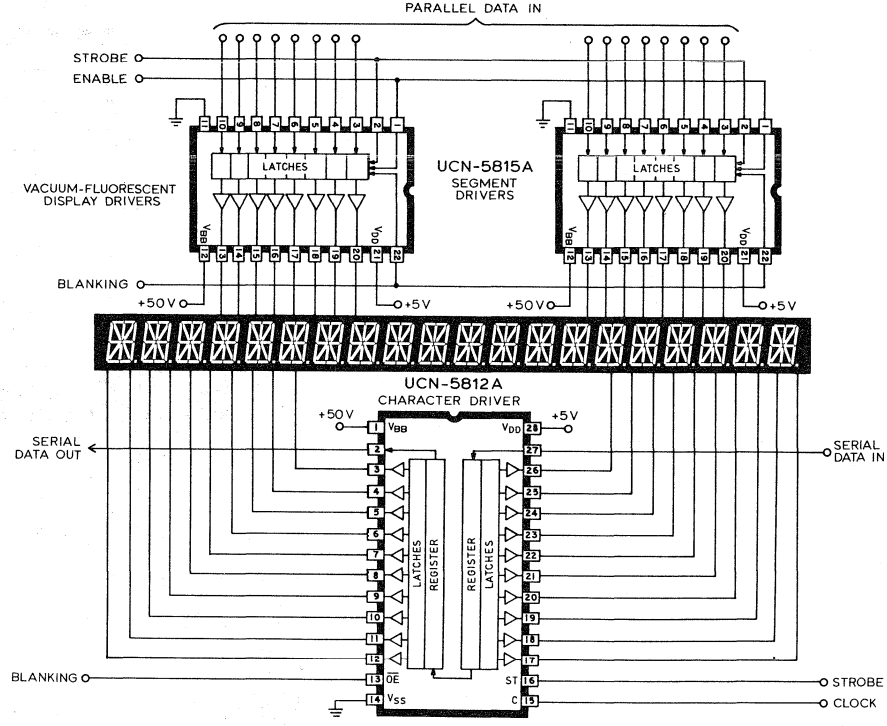
The UCN5815A 8-bit, latched, source driver provides a practical means of driving the segments, dots (matrix panel), or bars of multiplexed high-voltage vacuum-fluorescent displays. The UCN5810A (10-bit), UCN5812A (20-bit), or UCN5818A (32-bit) serial-input latched source drivers are well-suited for use as character or digit drivers. The high-voltage versions (suffix-1) can also be used to drive the anodes of planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN5810A, UCN5812A, UCN5818A ..... **55 V**
- UCN5810A-1, UCN5812A-1, UCN5818A-1 ..... **75 V**

Logic Supply Voltage Range ..... **5.0 V to 12 V**

Continuous Output Current ..... **-25 mA**



Dwg. No. D-1112

MULTIPLEXED INCANDESCENT LAMP DRIVERS

In order to obtain brightness equivalent to normal dc operation, multiplexed incandescent displays must be operated at a voltage:

$$E_{MPX} = E_{DC}\sqrt{N}$$

where E_{MPX} = the recommended operating supply voltage,

E_{DC} = the rated dc lamp voltage, and

N = the number of digits being multiplexed.

Multiplexed lamps also require isolation diodes to prevent sneak series/parallel paths to unaddressed elements.

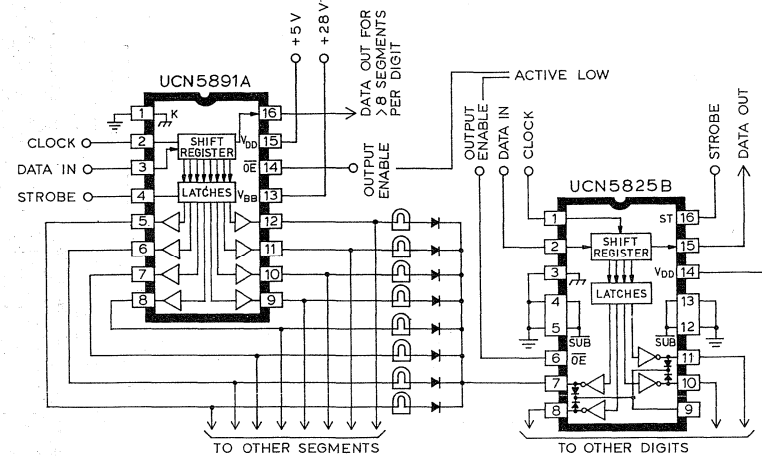
Serial-input, latched source drivers provide simple, compact, and economical segment drivers for mutiplexed incandescent lamp applications. The UCN5890A and UCN5891A feature high-voltage, high-current (500 mA, peak) Darlington outputs. The UCN5895A has saturated outputs for minimum voltage drop and will source up to 250 mA per driver. The drivers are supplied in an economical 16-pin "A" package. The UCN5890, UCN5891, and UCN5895 are pin-compatible except for output ratings.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN5890A . . . . . **75 V**
- UCN5891A . . . . . **45 V**
- UCN5895A . . . . . **45 V**

Logic Supply Voltage Range . . . . . **5.0 V to 12 V**

Continuous Output Current
- UCN5890A . . . . . **-350 mA**
- UCN5891A . . . . . **-350 mA**
- UCN5895A . . . . . **-120 mA**



Dwg. No. EP-024

MULTIPLEXED LED DRIVERS

Latched source drivers are simple, compact, and economical segment drivers for multiplexed LED and incandescent and lamp applications. The UCN5895A features saturated outputs for minimum voltage drop. It sources a minimum of 120 mA per driver. The source driver is supplied in an economical 16-pin 'A' package.

A typical common-cathode LED display driver application is shown below. The high-current UCN5821A, a latched sink driver, is used to drive the digits. Common-anode LED displays would require the use of the UCN5891A source driver and UCN5821A sink driver.

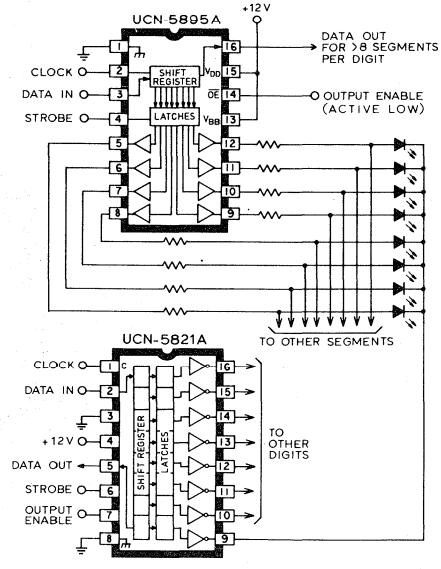
In order to obtain sufficient brightness, multplexed LED displays must typically be operated at greatly increased current. Appropriate current limiting is required.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN5821A . . . . . **45 V**
- UCN5890A . . . . . **75 V**
- UCN5891A . . . . . **45 V**
- UCN5895A . . . . . **45 V**

Logic Supply Voltage Range . . . . . **5.0 V to 12 V**

Continuous Output Current
- UCN5821A . . . . . **350 mA**
- UCN5890A . . . . . **-350 mA**
- UCN5891A . . . . . **-350 mA**
- UCN5895A . . . . . **-120 mA**



Dwg. No. B-1541

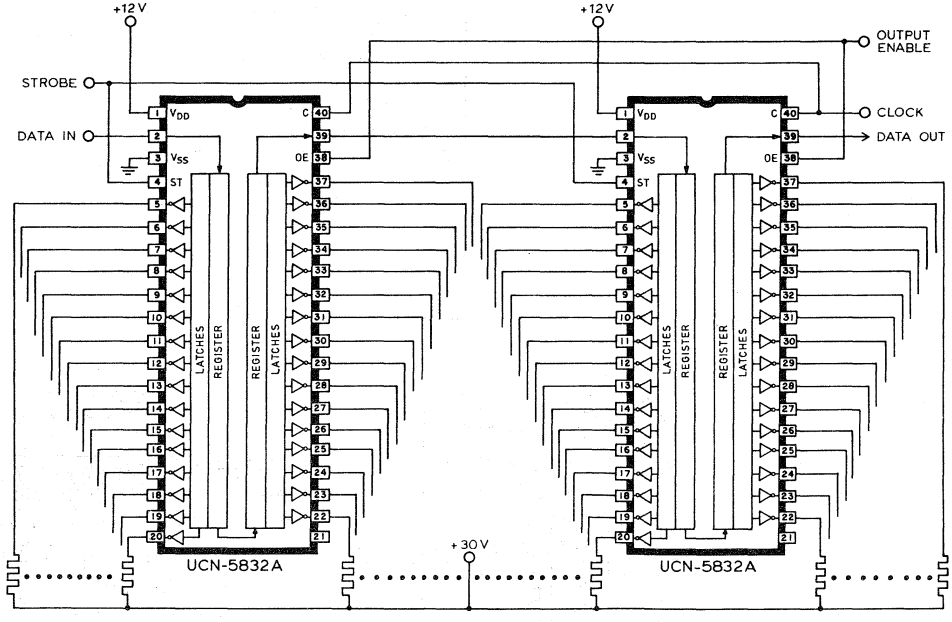
THERMAL PRINTHEAD DRIVER

Designed primarily for use with thermal printheads, the UCN5832A is optimized for low output-saturation voltage and high-speed operation. Each device has 32 bipolar, open-collector saturated outputs, a CMOS data latch for each driver, a 32-bit CMOS shift register, and CMOS control circuitry. A CMOS serial data output allows these devices to be cascaded in applications requiring more than 32 bits.

The UCN5832A is supplied in a 40-pin DIP with 0.600" row spacing. Under normal conditions, all outputs will sustain 100 mA continuously without derating. They can also be supplied in unpackaged chip form or in a leaded chip carrier.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	**40 V**
Logic Supply Voltage Range	**5.0 V to 12 V**
Continuous Output Current	**100 mA**



Dwg. No. D-1113

RELAY AND SOLENOID DRIVERS

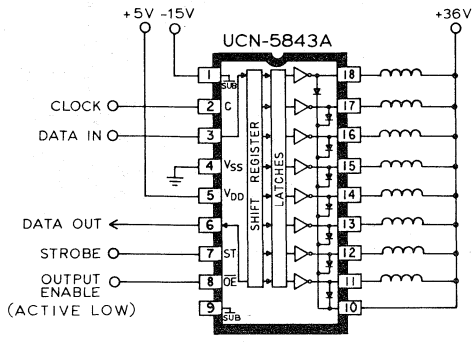
BiMOS II drivers provide an interface flexibility beyond the reach of standard logic buffers and power-driver arrays. Drivers with internal, transient-suppression diodes are ideal for use with relay and solenoid loads.

Series UCN5840A sink drivers feature isolated logic and power grounds that allow split-supply operation or isolated grounds for reduction of transients and noise currents on common logic/load ground lines. The UCN5890A source driver requires load supply voltages of at least 20 V. For lower-voltage operation, the UCN5891A is recommended.

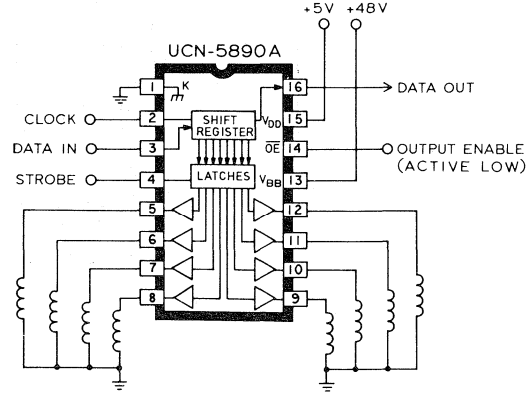
The serial DATA OUTPUT allows cascading for interface applications requiring additional drive lines. The OUTPUT ENABLE can also provide a CHIP ENABLE function that uses a minimum number of drive lines to control output from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltages (Inductive Load)	
UCN5841A	**35 V**
UCN5842A	**50 V**
UCN5843A	**60 V**
UCN5890A	**50 V**
UCN5891A	**35 V**
Logic Supply Voltage Range	**5.0 V to 12 V**
Continuous Output Current	**350 mA**



Dwg. No. A-12,547

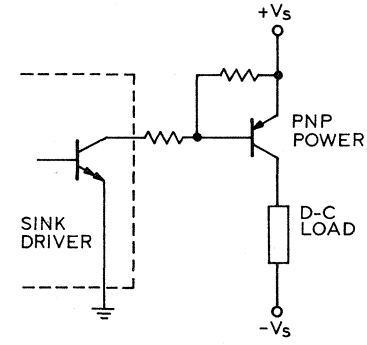


Dwg. No. A-12,548

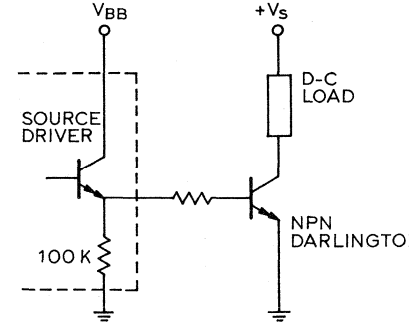
MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

BiMOS II power drivers can also be used as multi-channel pre-drivers for discrete high-current semiconductors, reducing the need for many discrete components. BiMOS II sink drivers provide enough switching current to the bases of discrete PNP power transistors for load currents of up to 20 A. Higher load currents can be obtained by using power Darlington devices. BiMOS II source drivers may require discrete Darlington power drivers for significant load currents, but have the advantage of allowing rather wide load-voltage swings.

For ac loads, source drivers can be used to provide gate current (with appropriate current limiting) to a power SCR or triac. This scheme can provide an economical approach to many applications such as driving incandescent lamps or ac motors with current levels of up to 20 A.



Dwg. No. A-11,744A



Dwg. No. A-11,745A

GENERAL INFORMATION & PRODUCT INDEX 1

PRODUCT SELECTION GUIDES 2

PERIPHERAL POWER & DISPLAY DRIVER ICs 3

HALL-EFFECT & OPTOELECTRONIC SENSOR ICs 4

INTEGRATED CIRCUITS to MIL-STD-883 5

AUTOMOTIVE, SIGNAL-PROCESSING, & CONSUMER ICs 6

DISCRETE TRANSISTORS, DIODES, & ARRAYS 7

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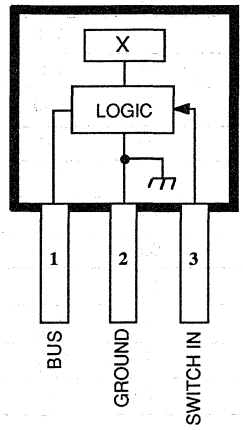
PACKAGE INFORMATION 9

SECTION 4. TECHNICAL DATA & APPLICATION NOTES for Hall-Effect and Optoelectronic Sensor ICs

in Numerical Order ..... Beginning at 4-1
Applications Information:
Hall Effect Applications Guide 4-64
The Hall Effect Sensor 4-98
Light Sensing Using Optical Integrated Circuits 4-103

3055

MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR ICs



Dwg. PH-005

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{BUS} . . . . . **24 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Operating Temperature Range, T_A
UGN3055U . . . . . **-20°C to +80°C**
UGS3055U . . . . . **-40°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**
Package Power Dissipation,
P_D . . . . . **750 mW**

The UGN3055U and UGS3055U Hall effect sensors are digital magnetic sensing ICs capable of communicating over a two-wire power/signal bus. Using a sequential addressing scheme, the device responds to a signal on the bus and returns the diagnostic status of the IC, as well as the status of each monitored external magnetic field. As many as 30 sensors can function on the same two-wire bus. This IC is ideal for multiple sensor applications where minimizing the wiring harness size is desirable or essential.

The device consists of high-resolution bipolar Hall effect switching circuitry, the output of which drives high-density CMOS logic stages. These logic stages decode the address pulse and enable a response at the appropriate address. The combination of magnetic-field or switch-status sensing, low-noise amplification of the Hall transducer output, and high-density decoding and control logic is made possible by the development of a new sensor BiMOS fabrication technology.

This unique magnetic sensing IC is available in two temperature ranges; the UGN3055U operates within specifications between -20°C and +85°C, while the UGS3055U is rated for operation between -40°C and +125°C. Alternate magnetic and temperature specifications are available upon request. Both versions are supplied in a 60 mil (1.54 mm) thick, three-pin plastic SIP. Each package is clearly marked with a two-digit decimal device address (xx).

FEATURES

- Complete Multiplexed Hall-Effect IC with Simple Sequential Addressing Protocol
- Allows Power and Communication Over a Two-Wire Bus (Supply/Signal and Ground)
- Up to 30 Hall-Effect Sensors Can Share a Bus
- Sensor Diagnostic Capabilities
- Magnetic-Field or Switch-Status Sensing
- Low Power of BiMOS Technology Favors Battery-Powered and Mobile Applications
- Ideal for Automotive, Consumer, and Industrial Applications

Always order by complete part number:

Part Number	Operating Temperature Range
UGN3055U	-20°C to +80°C
UGS3055U	-40°C to +125°C

3055
MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR IC

OPERATIONAL CHARACTERISTIC over operating temperature range.

Electrical Characteristics		Symbol	Limits			Units
			Min.	Typ.	Max.	
Power Supply Voltage		V_{BUS}	—	—	15	V
Signal Current		I_S	12	15	20	mA
Quiescent Current	V_{BUS} = 6 V	I_{QH}	—	—	2.5	mA
	V_{BUS} = 9 V	I_{QL}	—	—	2.5	mA
	I_{QH}–I_{QL}	I_Q	—	—	300	µA
Address Range		Addr	1	—	30	—
Clock Thresholds	LOW to HIGH	V_{CLH}	—	—	8.5	V
	HIGH to LOW	V_{CHL}	6.5	—	—	V
	Hysteresis	V_{CHYS}	—	0.8	—	V
Clock Period		T_{CLK}	0.1	1.0	—	ms
Address LOW Voltage		V_L	V_{RST}	6	V_{CHL}	V
Address HIGH Voltage		V_H	V_{CLH}	9	V_{BUS}	V
Power-On Reset Voltage		V_{RST}	2.5	3.5	5.5	V
Settling Time	V_{BUS} = 9 V	t_h	100	—	—	µs
	V_{BUS} = 6 V	t_l	100	—	—	µs
Propagation Delay	LOW to HIGH	t_{plh}	10	—	—	µs
	HIGH to LOW	t_{phl}	—	—	10	µs
Pin 3 Input Resistance	No Magnetic Field (V_{OUT} = HIGH)	R_{OUTH}	40	—	75	kΩ
	Mag. Field Present (V_{OUT} = LOW)	R_{OUTL}	—	—	50	Ω

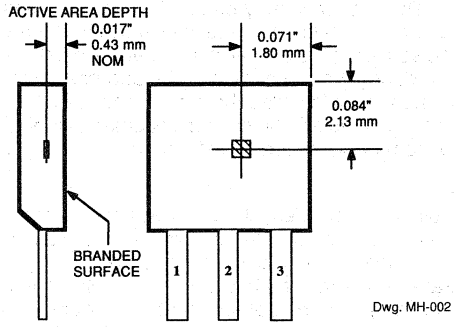
Magnetic Characteristics

Magnetic Thresholds	*Turn-On	B_{OP}	50	150	300	G
	Turn-Off	B_{RP}	-25	100	300	G
Hysteresis (B_{OP}–B_{RP})		B_{HYS}	0	50	75	G

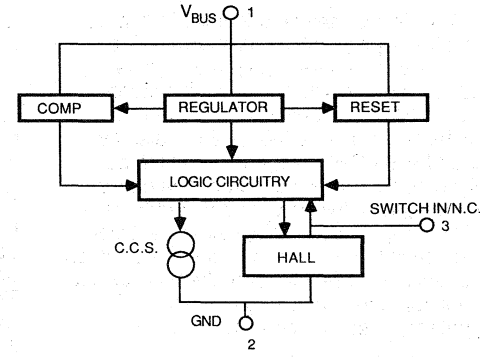
*Alternate magnetic switch point specifications are available on request. Please contact the factory.

3055
MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR IC

SENSOR LOCATION



FUNCTIONAL BLOCK DIAGRAM



DEFINITION OF TERMS

Sensor Address

Each bus sensor has a factory-specified predefined address. At present, allowable sensor addresses are integers from 1 to 30.

LOW-to-HIGH Clock Threshold (V_{CLH})

Minimum voltage required during the positive-going transition to increment the bus address and trigger a diagnostic response from the bus sensors. This is also the maximum threshold of the on-chip comparator which monitors the supply voltage, V_{BUS}.

HIGH-to-LOW Threshold (V_{HL})

Maximum voltage required during the negative-going transition to trigger a *signal* current response from the bus sensors. This is also the maximum threshold of the on-chip comparator which monitors the supply voltage, V_{BUS}.

Bus HIGH Voltage (V_H)

Bus HIGH voltage required for addressing. Voltage should be greater than V_{CLH}.

Address LOW Voltage (V_L)

Bus LOW Voltage required for addressing. Voltage should be greater than V_{RST} and less than V_{CHL}.

Bus Reset Voltage (V_{RST})

Voltage level required to reset individual sensors.

Sensor Quiescent Current Drain (I_Q)

The current drain of bus sensors when active but not addressed. I_{QH} is the maximum quiescent current drain when the sensor is not addressed and is at V_H. I_{QL} is the maximum quiescent current drain when the sensor is not addressed and is at V_L.

Diagnostic Phase

Period on the bus when the address voltage is at V_H. During this period, a correctly addressed sensor responds by increasing its current drain on the bus. This response from the sensor is called the **diagnostic response** and the bus current *increase* is called the **diagnostic current.**

Signal Phase

Period on the bus when the address voltage is at V_L. During this period, a correctly addressed sensor that detects a magnetic field greater than magnetic Operate Point B_{OP} responds by maintaining a current drain of I_S on the bus. This response from the sensor is called the **signal response** and the bus current *increase* is called the **signal current.**

Sensor Address Response Current (I_S)

Current returned by the bus sensors during the *diagnostic* and the *signal* responses of the bus sensors. This is accomplished by enabling the constant current source (CCS).

Magnetic Operate Point (B_{OP})

Minimum magnetic field required to switch ON the Hall amplifier and switching circuitry of the addressed sensor. This circuitry is only active when the sensor is addressed.

Magnetic Release Point (B_{RP})

Magnetic field required to switch OFF the Hall amplifier and switching circuitry after the output has switched ON. This is due to magnetic memory in the switching circuitry. However, when a device is deactivated by changing the current bus address, all magnetic memory is lost.

Magnetic Hysteresis (B_{HYS})

Difference between the B_{OP} and B_{RP} magnetic field thresholds.

ADDRESSING PROTOCOL

The device may be addressed by modulating the supply voltage as shown in Figure 1. A preferred addressing protocol is as follows: the bus supply voltage is brought down to 0 V so that all devices on the bus may be reset. The voltage is then raised to the address LOW voltage (V_L) and the bus quiescent current is measured. The bus is then toggled between V_L and V_H (address HIGH voltage), with each positive transition representing an increment in the bus address. After each voltage transition, the bus current is monitored to check for diagnostic and signal responses from sensor IC's.

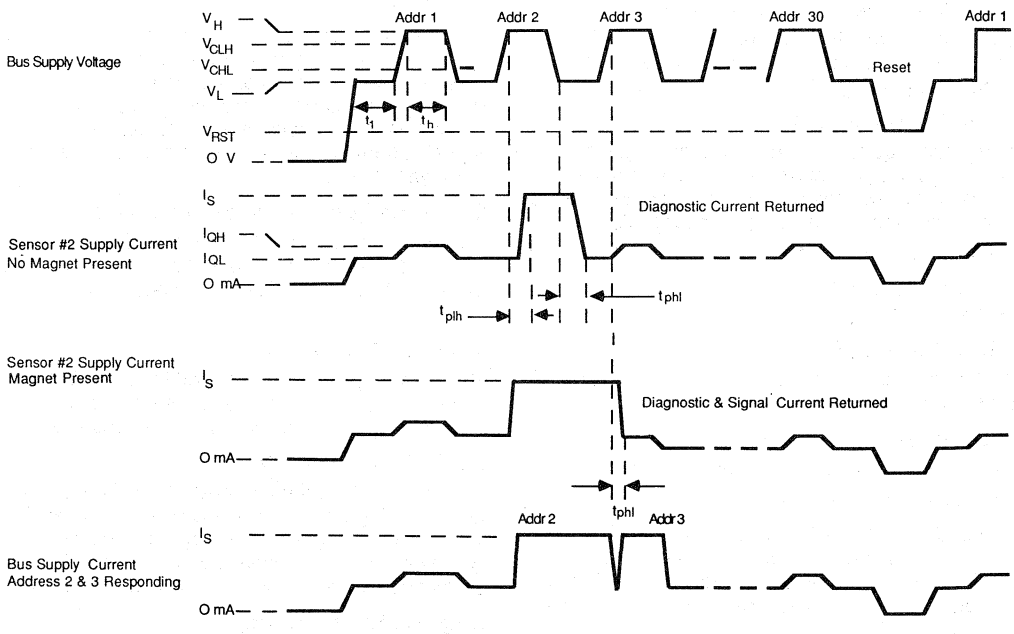
Sensor Addressing

When a sensor detects a bus address equal to its factory programmed address, it responds with an increase in its supply current drain (called I_S during the HIGH portion of the address cycle). This response may be used as an indication that the sensor is alive and well on the bus and is also called the *diagnostic* response. If the sensor detects an ambient magnetic field, it also responds with I_S during the low portion of the address cycle. This response from the sensor is called the *signal* response. When the next positive transition is detected, the sensor becomes disabled, and its contribution to the bus signal current returns to I_Q.

Bus Current

Figure 1 displays the above described addressing protocol. The top trace represents the bus voltage transitions as controlled by the bus driver (see applications note for an optimal bus driver schematic). The second trace represents the bus current contribution of sensor (address 2). The *diagnostic* response from the sensor indicates that it detected its address on the bus; however, no *signal* response current is returned which indicates that sufficient magnetic field is not detected at the chip surface. The third trace represents the current drain of sensor 2 when a magnetic field is detected. Note both the *diagnostic* and *signal* response from the sensor. The last trace represents the overall bus current drain when sensors 2 and 3 are present; note that

FIGURE 1
BUS TIMING DI



NOTE: Diagnostic current is returned when the preset device address is detected.
Signal current is returned when the correct address and magnetic field are both detected.

APPLICATIONS NOTES

while sensor 2 returns a *diagnostic* and *signal* current, sensor 3 only returns a *diagnostic* current. When no sensors are addressed, the net bus current drain is the sum of quiescent currents of all sensors on the bus (for 'n' sensors, the bus quiescent current drain is $n*I_Q$).

Bus Issues

At present, a maximum of 30 active sensors can coexist on the same bus, each with a different address. Address 0 is reserved for bus current calibration in software. This feature allows for fail-safe detection of signal current and eliminates detection problems caused by low signal current (I_S), the operation of sensors at various ambient temperatures, lot-to-lot variation of quiescent current, and the addition and replacement of sensors to the bus while in the field. Address 31 is designed to be inactive to allow for further address expansion of the bus (to 62 maximum addresses). In order to repeat the address cycle, the bus must be reset as shown in Figure 1 by bringing the supply voltage to below V_{RST}. Sensors have been designed not to 'wrap-around'.

Magnetic Sensing

The sensor IC has been designed to respond to an external magnetic field whose magnetic strength is greater than B_{OP}. It accomplishes this by amplifying the output of an on-chip Hall transducer and feeding it into a threshold detector. In order that bus current is kept to a minimum, the transducer and amplification circuitry is kept powered down until the sensor is addressed. Hence, the magnetic status is evaluated only when the sensor is addressed.

External Switch Sensing

The third pin of the IC (pin 3) may be used to detect the status of an external switch when magnetic field sensing is not desired (and in the absence of a magnetic field). The allowable states for the switch are 'open' and 'closed' (shorted to sensor ground).

Magnetic Actuation

Figure 2 shows the wiring of the UGN/UGS3055U when used as a magnetic threshold detector. Pin 1 of the sensor is wired to the positive terminal of the bus, pin 2 is connected to the bus negative terminal, and *pin 3 has no connection.*

Mechanical Actuation

Figure 3 shows the wiring of the UGN/UGS3055U when used to detect the status of a mechanical switch. In this case, pin 3 is connected to the positive terminal of the switch. The negative side of the switch is connected to the negative terminal of the bus. When the mechanical switch is closed (shorted to ground) and the correct bus address is detected by the IC, the sensor responds with a signal current. If the switch is open, only a diagnostic current is returned.

FIGURE 2
MAGNETICALLY ACTUATED SENSOR

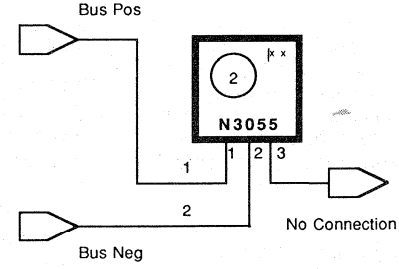


FIGURE 3
MECHANICALLY ACTUATED SENSOR

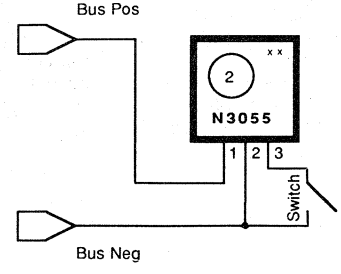
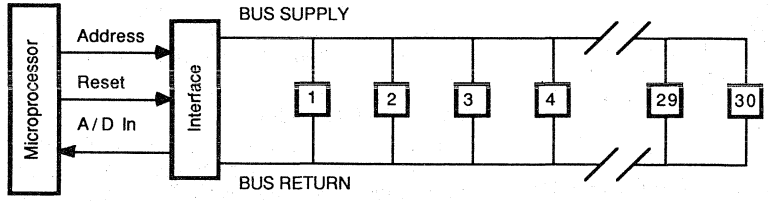


FIGURE 4
BUS INTERCONNECTION



Bus Configuration

A maximum of 30 sensors may be connected across the same two wire bus as shown in Figure 4. It is recommended that the sensors use a dedicated digital ground wire to minimize the effects of changing ground potential (as in the case of chassis ground in the automotive industry).

The bus was not designed to require two wire twisted pair wiring to the sensors; however, in areas of extreme EMI (electromagnetic interference), it may be advisable to install a small bypass capacitor (.01 μF for example) between the supply and ground terminals of each sensor instead of using the more expensive wiring.

Bus Driver

It is recommended that the bus be controlled by microprocessor-based hardware for the following reasons:

- Sensor address information may be stored in ROM in the form of a look up table.
- Bus faults can be pinpointed by the microprocessor by comparing the diagnostic response to the expected response in the ROM look up table.
- The microprocessor, along with an A/D converter, can also be used to self calibrate the quiescent currents in the bus and hence be able to easily detect a signal response.
- The microprocessor can also be used to filter out random line noise by digitally filtering the bus responses.
- The microprocessor can easily keep track of the signal responses, initiate the appropriate action; e.g., light a lamp, sound an alarm, and also pinpoint the location of the signal.

Optimally, the microprocessor is used to control bus-driving circuitry that will accept TTL level inputs to drive the bus and will return an analog voltage representation of the bus current.

Interface Schematic

The bus driver is easily designed using a few operational amplifiers, resistors, and transistors. Figure 5 shows a schematic of a recommended bus driver circuit that is capable of providing 6 to 9 V transitions, resetting the bus, and providing an analog measurement of the current for use by the A/D input of the microprocessor.

In Figure 5, the Address pin provides a TTL-compatible input that is used to control the Bus supply. A HIGH (5 V) input switches Q1 ON and sets the bus voltage to 6 V through the resistor divider R4, R5, and the Zener. A LOW input switches OFF Q1 and sets the bus voltage to 9 V. This voltage is fed into the positive input of the operational amplifier OP1 and is buffered and made available at Bus Supply (or sensor supply). Bus reset control is also available in the form of a TTL-compatible input. When this input, which is marked Reset, is HIGH, Q2 is switched ON and the positive input of the op amp is set to the saturation voltage of the transistor (approximately 0 V). This resets the bus.

A linear reading of the bus current is made possible by amplifying the voltage generated across R6 (which is I_{BUS} *R6). The amplifier, OP2, is a standard differential amplifier of gain R9/R7 (provided that R7 = R8, R9 = R10). The gain of the total transimpedance amplifier is given by:

$$V_{OUT} = I_{BUS} * R6 * R9/R7$$

This voltage is available at the terminal marked TO A/D.

Bus Control Software

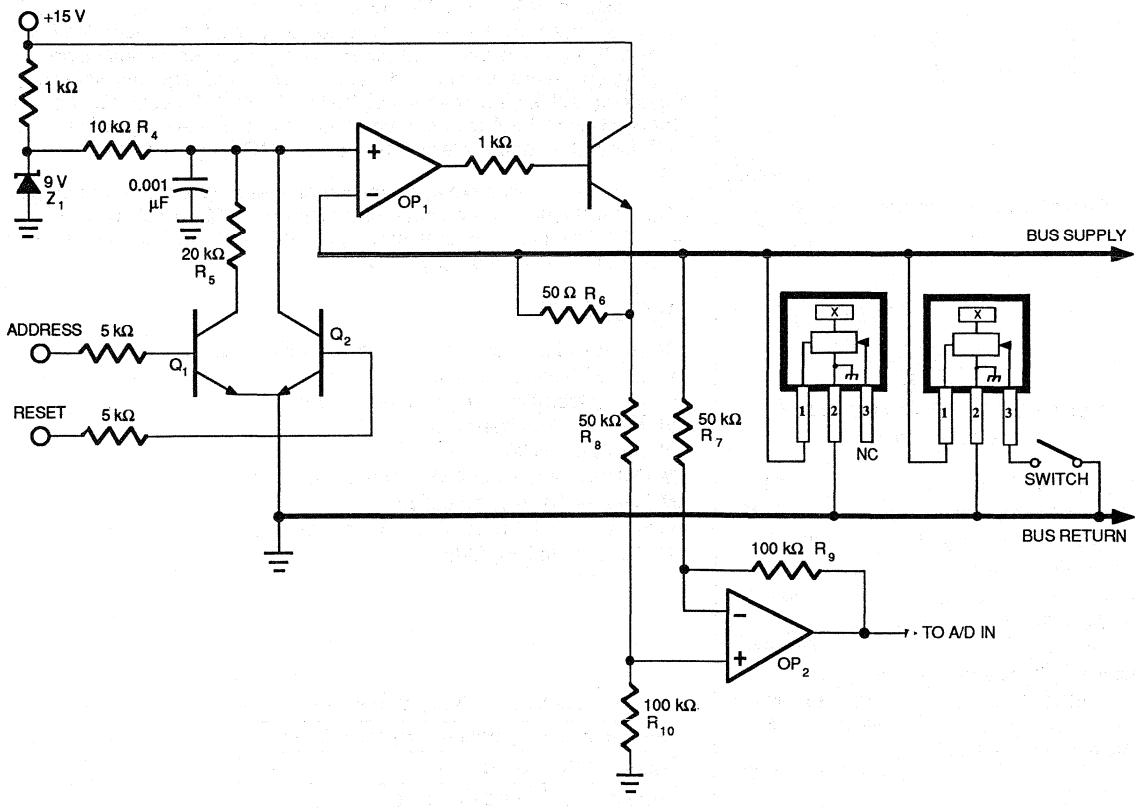
The processing of the bus current (available at pin A/D In) is best done by feeding it into the A/D input of a microprocessor. If the flexibility provided by a microprocessor is not desired, this signal could be fed into threshold detection circuitry; e.g., comparator, and the output used to drive a display.

Related References

1. G. AVERY, "Two Terminal Hall. Sensor," *ASSIGNEE: Sprague Electric Company, North Adams, MA, United States. Patent number 4,374,333; Feb. 1983.*

2. T. WROBLEWSKI and F. MEISTERFIELD, "Switch Status Monitoring System, Single Wire Bus, Smart Sensor Arrangement There Of," *ASSIGNEE: Chrysler Motor Corporation, Highland Park, MI, United States. Patent number 4,677,308; June 1987.*

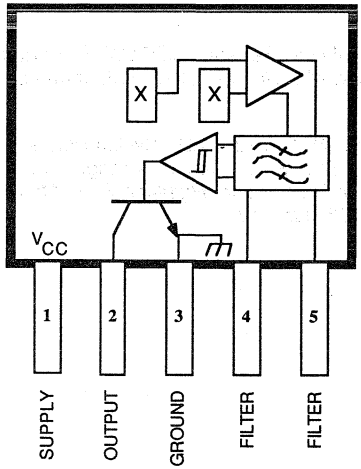
FIGURE 5
BUS INTERFACE SCHEMATIC



Dwg. EH-003

3059

HALL EFFECT GEAR-TOOTH SENSORS —AC COUPLED



Dwg. PH-011

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} . . . . . **24 V**
Reverse Battery Voltage, V_{RCC} . . . . . **-30 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . . **24 V**
Output Current, I_{OUT} . . . . . **25 mA**
Package Power Dissipation, P_D . . . . . **500 mW**
Operating Temperature Range, T_A
UGN3059KA . . . . . **-20°C to +85°C**
UGS3059KA . . . . . **-40°C to +125°C**
Storage Temperature Range, T_S . . . . . **-65°C to +150°C**

The UGN3059KA and UGS3059KA ac-coupled Hall effect gear-tooth sensors are monolithic integrated circuits that switch in response to changing differential magnetic fields created by moving ferrous targets. These devices are ideal for use in non-zero-speed, gear-tooth-based speed, position, and timing applications.

Both devices, when coupled with a back-biasing magnet, can be configured to turn ON or OFF with the leading or trailing edge of a gear-tooth or slot. Changes in fields on the magnet face caused by a moving ferrous mass are sensed by two integrated Hall transducers and are differentially amplified by on-chip electronics. Steady-state magnet and system offsets are eliminated using an on-chip differential band-pass filter. This filter also provides relative immunity to interference from RF and electromagnetic sources. The on-chip temperature compensation and Schmitt trigger circuitry minimizes shifts in effective working air gaps and switch points over temperature, allowing operation to low frequencies over a wide range of air gaps and temperatures.

Each Hall effect digital Integrated circuit includes a voltage regulator, two quadratic Hall effect sensing elements, temperature compensating circuitry, a low-level amplifier, band-pass filter, Schmitt trigger, and an open-collector output driver. The on-board regulator permits operation with supply voltages of 4.5 to 18 volts. The output stage can easily switch 20 mA over the full frequency response range of the sensor and is compatible with bipolar and MOS logic circuits.

The two devices provide a choice of operating temperature ranges. The UGN3059KA has an operating range of -20°C to +85°C. The UGS3059KA has an operating range of -40°C to +125°C. Both devices are packaged in a 5-pin plastic SIP.

PRELIMINARY

FEATURES

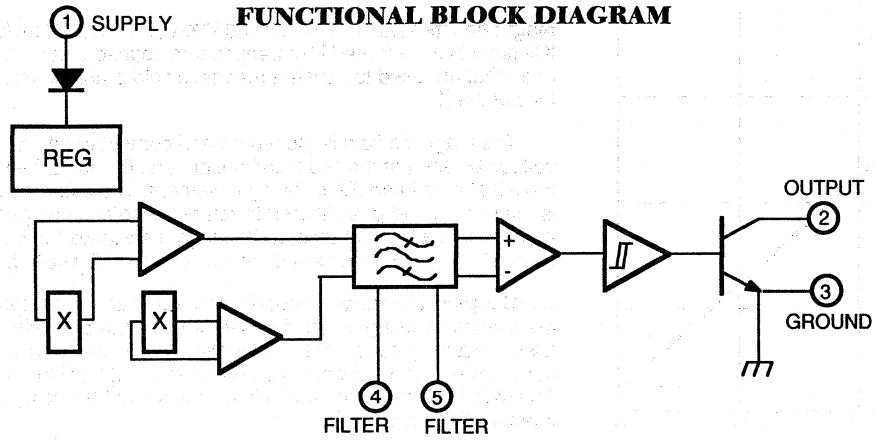
- Senses Motion of Ferrous Targets Such as Gears
- Large Effective Air Gap
- Wide Operating Temperature Range
- 4.5 V to 18 V Operation
- Operation to 30 kHz
- Output Compatible With All Logic Families
- Reverse Battery Protection
- Activate With Small, Inexpensive Magnets
- Resistant to RFI, EMI

Always order by complete part number:

Part Number	Operating Temperature Range
UGN3059KA	-20°C to +85°C
UGS3059KA	-40°C to +125°C

3059
HALL EFFECT GEAR-TOOTH SENSORS—AC COUPLED

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-008

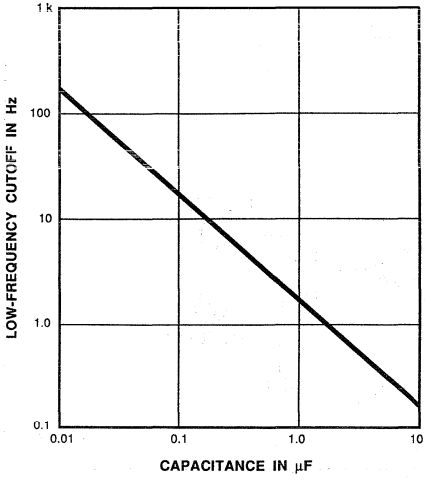
ELECTRICAL CHARACTERISTICS over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	18	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	—	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	—	10	µA
Supply Current	I_{CC}	V_{CC} = 18 V, B < B_{OP}	—	—	20	mA
High-Frequency Cutoff	f_{coh}	-3 dB	30	—	—	kHz
Output Rise time	t_r	V_{OUT} = 12 V, R_L = 820 Ω	—	0.04	0.2	µs
Output Fall time	t_f	V_{OUT} = 12 V, R_L = 820 Ω	—	0.18	0.3	µs

MAGNETIC CHARACTERISTICS over operating temperature range, V_{CC} = 12 V.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operate Point	B_{OP}	Output Switches OFF to ON	10	—	100	G
Release Point	B_{RP}	Output Switches ON to OFF	-100	—	-10	G
Hysteresis	B_{hys}	B_{OP}-B_{RP}	20	—	150	G

NOTES: Magnetic switch points are specified as the difference in magnetic fields at the two Hall elements.
As used here, negative flux densities are defined as less than zero (algebraic convention).
Typical values are at T_A = +25°C and V_{CC} = 12 V.



Dwg. GH-025

APPLICATIONS INFORMATION

Magnetic Operation. The UGN3059KA and UGS3059KA sensor ICs have two integrated Hall transducers spaced 0.088" (2.24 mm) apart that are used to sense a magnetic field gradient across the face of the IC.

The magnetic field is measured and converted into an analog voltage by each of the two Hall transducers, E1 and E2 where E1 is the left element and E2 is the right element. The difference voltage is amplified, band-pass filtered to remove dc offset components, and then fed into a Schmitt trigger. This trigger switches the output ON when B_{E1}-B_{E2} > B_{OP} and switches the output OFF when B_{E1}-B_{E2} < B_{RP}.

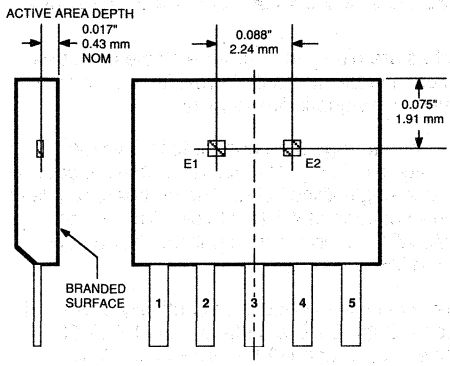
AC-Coupled Operation. Steady-state magnet and system offsets are eliminated using an on-chip differential band-pass filter. The lower frequency cut-off of this patented filter is set using an external capacitor the value of which can range from 0.01 μF to 10 μF. The high-frequency cut-off of this filter is set at 30 kHz by an internal integrated capacitor.

The differential structure of this filter enables the IC to reject single-ended noise on the ground or supply line and, hence, makes it resistant to radio-frequency and electromagnetic interference typically seen in hostile remote sensing environments. This filter configuration also increases system tolerance to capacitor degradation at high temperatures, allowing the use of an inexpensive external ceramic capacitor.

Low-Frequency Operation. Low-frequency operation of the sensor is set by the value of an external capacitor. The graph provides the low-frequency cut-off (-3 dB point) of the filter as a function of capacitance value. This information should be used with care. The graph assumes a perfect sinusoidal magnetic signal input. In reality, when used with gear teeth, the teeth create transitions in the magnetic field that have a much higher frequency content than the basic rotational speed of the target. This allows the device to sense speeds much lower than those indicated by the graph for a given capacitor value.

Capacitor Characteristics. The major requirement for the external capacitor is its ability to operate in a bipolar (non-polarized) mode. Another important requirement is the low leakage current of the capacitor (equivalent parallel resistance should be greater than 500 kΩ). To maintain proper operation with frequency, capacitor values should be held to within ±30% over the operating temperature range. Available non-polarized capacitors include ceramic, polyester, and some tantalum types. For low-cost operation, ceramic capacitors with temperature codes Z5S, Y5S, X5S, or X7S (depending on operating temperature range) or better are recommended. The commonly available Z5U temperature code should not be used in this application.

SENSOR LOCATION



Dwg. MH-007

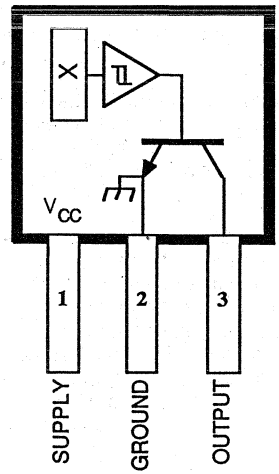
Magnet Biasing. In order to sense moving non-magnetized ferrous targets, the UGN3059KA or UGS3059KA must be back-biased by mounting it on a small permanent magnet. This can be accomplished by attaching the pole end of a magnet (AlNiCo 8, SmCo, or NeFe B) to the back of the package, opposite to the branded side. Either magnetic pole (north or south) can be used. The magnetic system, thus configured, can sense ferrous gear teeth out to 0.070" (1.75 mm) for typical wheel speed sensing targets or 0.100" (2.5 mm) for deep slotted ignition targets.

The UGN/UGS3059KA can also be used without a back-biasing magnet. In this configuration, the sensor can be used to detect a rotating ring magnet such as those found in brushless dc motors or in speed sensing applications. Here, the sensor detects the magnetic field gradient created by the moving magnetic poles.

Magnet Selection. The UGN/UGS3059KA can be used with a wide variety of commercially available permanent magnets. The selection of the magnet depends on the operational and environmental requirements of the sensing system. For systems that require high accuracy and large working airgaps or an extended temperature range, the usual magnet material of choice is rare earth samarium cobalt (SmCo). This magnet material has a high energy product and can operate over an extended temperature range. For systems that require low-cost solutions for an extended temperature range, AlNiCo 8 can be used. Due to its relatively low energy product, smaller operational airgaps can be expected. Neodymium iron boron (NeFeB) can be used over moderate temperature ranges when large working airgaps are required. Of these three magnet materials, AlNiCo 8 is the least expensive by volume and SmCo is the most expensive.

SERIES 3100

HALL EFFECT SWITCHES



Dwg. PH-003

Pinning is shown viewed from branded side.

These Hall effect switches are highly temperature stable and stress-resistant sensors best utilized in applications that provide steep magnetic slopes and low residual levels of magnetic flux density.

Each device includes a voltage regulator, quadratic Hall voltage generator, temperature stability circuit, signal amplifier, Schmitt trigger and open-collector output on a single silicon chip. The on-board regulator permits operation with supply voltages of 4.5 to 24 volts. The switch output can sink up to 20 mA. With suitable output pull up, they can be used directly with bipolar or MOS logic circuits.

The four package styles available provide a magnetically optimized package for most applications. Suffix LT is a surface-mount SOT 89 (TO-243AA) package; suffixes LL, U, and UA feature wire leads for through-hole mounting. Devices suitable for military applications with high-reliability screening and in a hermetic package (TO-260AA) are also available.

FEATURES

- 4.5 V to 24 V Operation
- Activate With Small, Commercially Available Permanent Magnets
- Solid-State Reliability... No Moving Parts
- Small Size
- Constant Output Amplitude
- Superior Temperature Stability
- Resistant to Physical Stress
- Directly Replace Series UGN and UGS3000T/U Switches

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **25 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . . **25 V**
Continuous Output Current, I_{OUT} . . . . **25 mA**
Operating Temperature Range, T_A
Prefix UGN . . . . . **-20°C to +85°C**
Prefix UGS . . . . . **-40°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C***

* Devices can be stored at +200°C for short periods of time.

Always order by complete part number, e.g., **UGN3113UA** .
See Magnetic Characteristics table for differences between devices.

ELECTRICAL CHARACTERISTICS at T_A + +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	150	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	<1.0	10	µA
Supply Current	I_{CC}	V_{CC} = 4.5 V, Output Open	—	4.7	8.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.04	2.0	µs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.18	2.0	µs

MAGNETIC CHARACTERISTICS in gauss

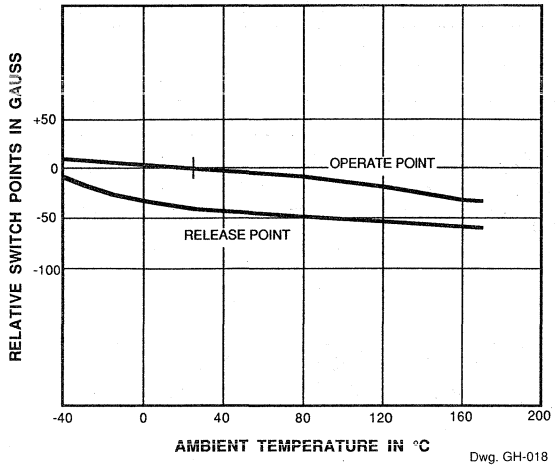
Characteristic	Part Number*	T_A = +25°C		T_A = -20°C to +85°C		T_A = -40°C to +125°C†	
		Min.	Max.	Min.	Max.	Min.	Max.
Operate Point, B_{OP}	3113	—	450	—	510	—	—
	3119	175	500	100	545	45	575
	3120	70	350	70	425	35	450
	3130	—	150	—	175	—	200
	3140	70	200	45	260	45	270
Release Point, B_{RP}	3113	30	—	20	—	—	—
	3119	125	450	50	495	25	555
	3120	50	330	50	405	25	430
	3130	-150	—	-175	—	-200	—
	3140	50	180	25	240	25	250
Hysteresis, B_{hys}	3113	20	—	10	—	—	—
	3119	50	—	50	—	20	—
	3120	20	—	20	—	20	—
	3130	20	—	20	—	20	—
	3140	20	—	20	—	20	—

NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention).

* Complete part number includes a prefix denoting operating temperature range (UGN or UGS) and a suffix denoting package type (LL, LT, U, or UA).

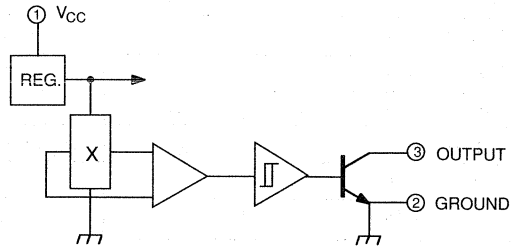
† Applicable to prefix UGS devices only (available with all devices except 3113).

TYPICAL CHARACTERISTICS AS FUNCTIONS OF TEMPERATURE



Dwg. GH-018

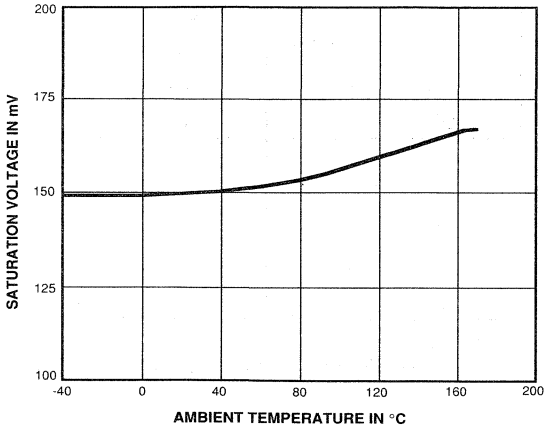
FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-005

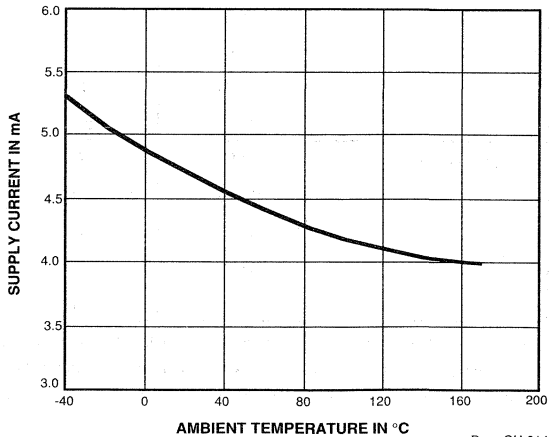
TYPICAL CHARACTERISTICS AS FUNCTIONS OF TEMPERATURE

OUTPUT SATURATION VOLTAGE



Dwg. GH-013

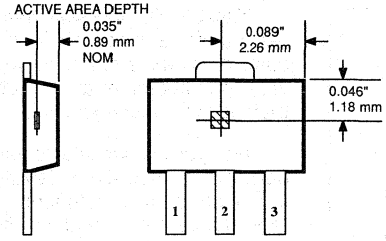
SUPPLY CURRENT



Dwg. GH-014

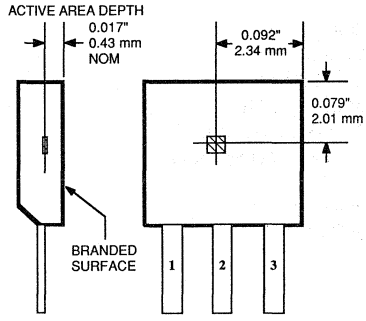
SENSOR LOCATIONS

SUFFIX "LL" AND "LT"



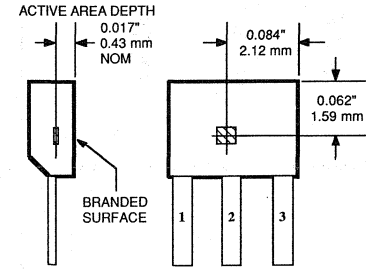
Dwg. MH-008

SUFFIX "U"



Dwg. MH-002-1

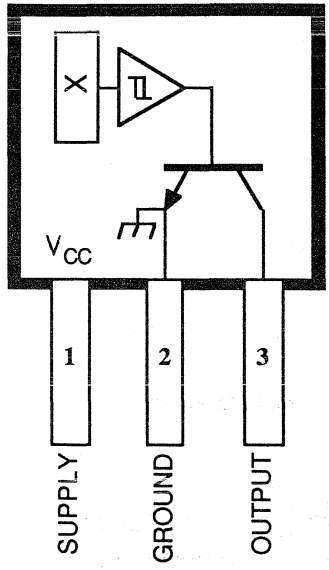
SUFFIX "UA"



Dwg. MH-011-1

3132 AND 3133

ULTRA-SENSITIVE BIPOLAR HALL EFFECT SWITCHES



Dwg. PH-003

Pinning is shown viewed from branded side.

These Hall effect switches are designed for magnetic actuation using a bipolar magnetic field, i.e., a north-south alternating field. They combine extreme magnetic sensitivity with excellent stability over varying temperature and supply voltage. The high sensitivity permits their use with multi-pole ring magnets over relatively large distances.

Each device includes a voltage regulator, quadratic Hall voltage generator, temperature stability circuit, signal amplifier, Schmitt trigger, and open-collector output on a single silicon chip. The on-board regulator permits operation with supply voltages of 4.5 to 24 volts. The switch output can sink up to 25 mA. With suitable output pull up, they can be used directly with bipolar or MOS logic circuits.

The four package styles available provide a magnetically optimized package for most applications. Suffix LT is a surface-mount SOT 89 (TO-243AA) package; suffixes LL, U, and UA feature wire leads for through-hole mounting. Prefix 'UGN' devices are rated for continuous operation over the temperature range of -20°C to +85°C; prefix 'UGS' devices over an extended range of -40°C to +125°C.

FEATURES

- 4.5 V to 24 V Operation
- Reverse Battery Protection
- Superior Temperature Stability
- Superior Supply Voltage Stability
- Activate with Multi-Pole Ring Magnets
- Solid-State Reliability...No Moving Parts
- Small Size
- Constant Output Amplitude
- Resistant to Physical Stress

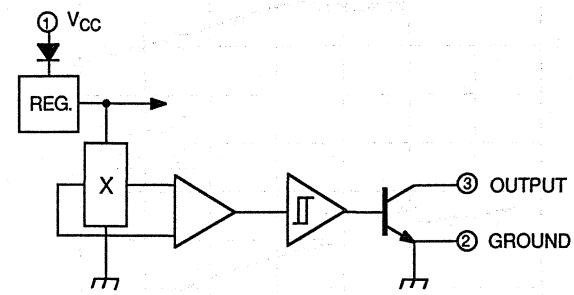
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **25 V**
Reverse Battery Voltage, V_{RCC} . . . . . **-35 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . . **25 V**
Continuous Output Current, I_{OUT} . . . **25 mA**
Operating Temperature Range, T_A
Prefix UGN . . . . . **-20°C to +85°C**
Prefix UGS . . . . . **-40°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Always order by complete part number, e.g., **UGN3132LL**.
See Magnetic Characteristics table for differences between devices.

3132 AND 3133
BIPOLAR HALL-EFFECT SWITCHES

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-005-2

ELECTRICAL CHARACTERISTICS at T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	-	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B ≥ B_{OP}	-	145	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B ≤ B_{RP}	-	<1.0	10	µA
Supply Current	I_{CC}	V_{CC} = 24 V, B ≤ B_{RP}	-	4.3	9.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	-	0.04	2.0	µs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	-	0.18	2.0	µs

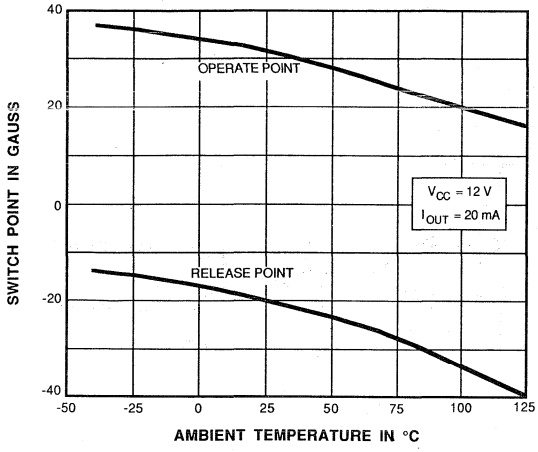
MAGNETIC CHARACTERISTICS over operating temperature and voltage range.

Characteristic	Symbol	Device Type*	Limits			
			Min.	Typ.	Max.	Units
Operate Point	B_{OP}	3132	—	32	95	G
		3133	—	32	75	G
Release Point	B_{RP}	3132	-95	-20	—	G
		3133	-75	-20	—	G
Hysteresis	B_{hys}	Both	30	52	—	G

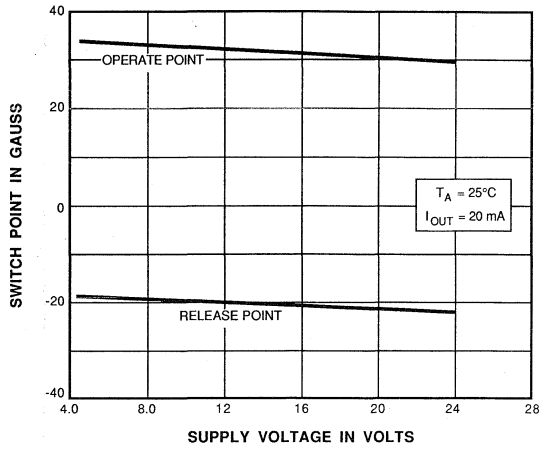
NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention.)
Typical values are at T_A = +25°C and V_{CC} = 12 V.

* Complete part number includes a prefix denoting operating temperature range (UGN or UGS) and a suffix denoting package type (LL, LT, U, or UA).

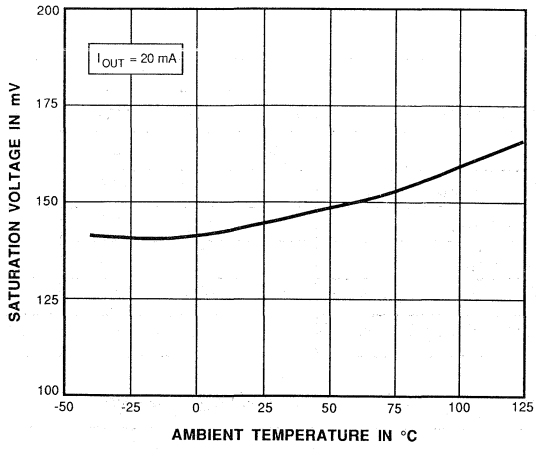
TYPICAL CHARACTERISTICS



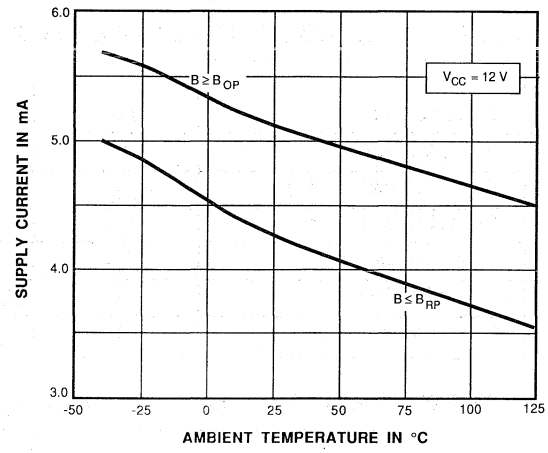
Dwg. GH-022



Dwg. GH-021



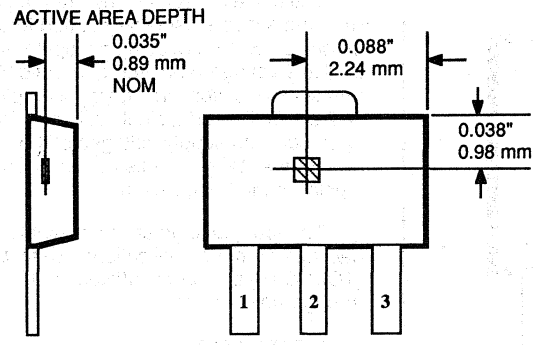
Dwg. GH-024



Dwg. GH-023

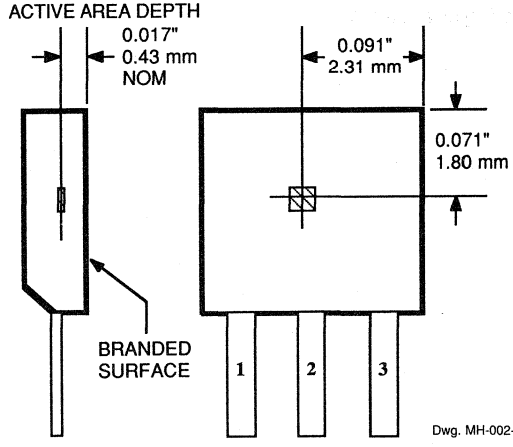
SENSOR LOCATIONS

SUFFIX "LL" & SUFFIX "LT"



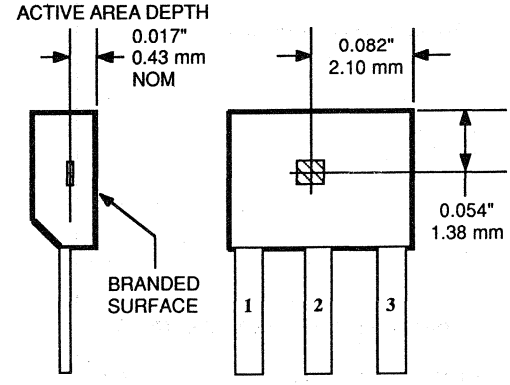
Dwg. MH-008-2

SUFFIX "U"



Dwg. MH-002-2

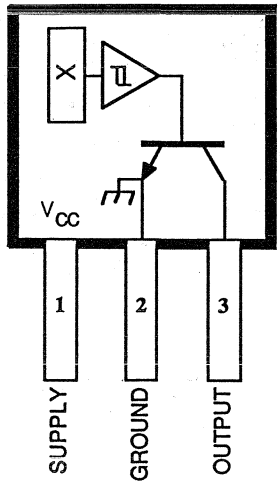
SUFFIX "UA"



Dwg. MH-011-2

3175 AND 3177

HALL EFFECT LATCHES



Dwg. PH-003

Pinning is shown viewed from branded side.

These Hall effect latches are temperature-stable and stress-resistant sensors especially suited for electronic commutation in brushless dc motors using multipole ring magnets. Each device includes a voltage regulator, quadratic Hall voltage generator, temperature compensation circuit, signal amplifier, Schmitt trigger, and an open-collector output on a single silicon chip. The on-board regulator permits operation with supply voltages of 4.5 to 24 volts. The switch output can sink 10 mA. With suitable output pull up, they can be used directly with bipolar or MOS logic circuits.

The four package styles available provide a magnetically optimized package for most applications. Suffix LT is a surface-mount SOT 89 (TO-243AA) package; suffixes LL, U, and UA feature wire leads for through-hole mounting.

FEATURES

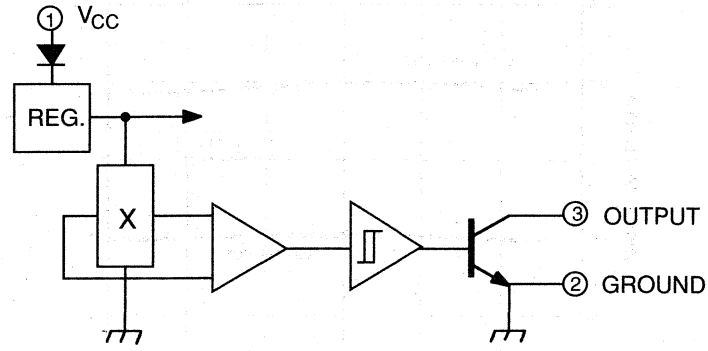
- Symmetrical Response
- 4.5 V to 24 V Operation
- Open-Collector Output
- Reverse Battery Protection
- Activate With Small, Commercially Available Permanent Magnets
- Solid-State Reliability ... No Moving Parts
- Small Size
- Superior Temperature Stability
- Resistant to Physical Stress

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **24 V**
Reverse Battery Voltage, V_{RCC} . . . . . **-35 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . . **24 V**
Continuous Output Current, I_{OUT} . . . **15 mA**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Always order by complete part number, e.g., **UGN3175LL** .
See Magnetic Characteristics table for differences between devices.

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-005-2

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{CC} = 24 V, I_{OUT} = 10 mA, B > B_{OP}	—	200	300	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	0.05	5.0	µA
Supply Current	I_{CC}	V_{CC} = 4.5 V, Output Open	—	5.0	10	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 1.1 kΩ, C_L = 20 pF	—	0.04	2.0	µs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 1.1 kΩ, C_L = 20 pF	—	0.18	2.0	µs

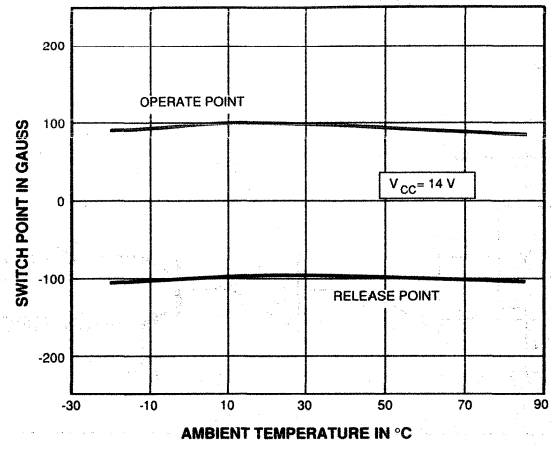
MAGNETIC CHARACTERISTICS in gauss; V_{CC} = 4.5 V to 24 V.

Characteristic	Part Number*	T_A = +25°C			T_A = -20°C to +85°C		
		Min.	Typ.	Max.	Min.	Typ.	Max.
Operate Point, B_{OP}	UGN3175	25	—	170	15	—	180
	UGN3177	50	—	150	25	—	150
Release Point, B_{RP}	UGN3175	-170	—	-25	-180	—	-15
	UGN3177	-150	—	-50	-150	—	-25
Hysteresis, B_{hys}	UGN3175	100	200	—	80	180	—
	UGN3177	100	200	—	50	180	—

NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention).

* Complete part number includes a suffix denoting package type (LL, LT, U, or UA).

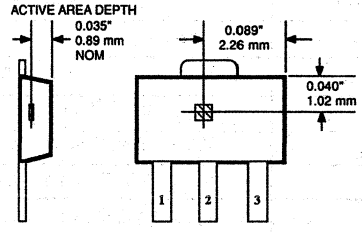
TYPICAL OPERATING CHARACTERISTICS



Dwg. GH-020

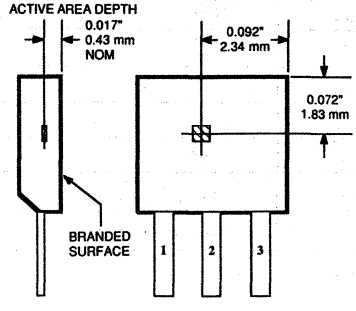
SENSOR LOCATIONS

Suffix "LL" & Suffix "LT"



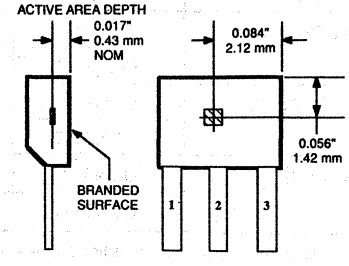
Dwg. MH-008-1

Suffix "U"



Dwg. MH-002-3

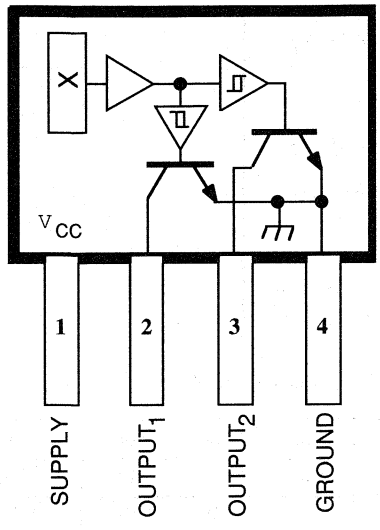
Suffix "UA"



Dwg. MH-011

3235

DUAL OUTPUT HALL EFFECT SWITCH



Dwg. PH-007

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Power Supply, V_{CC} . . . . . **25 V**
Reverse Battery Voltage, V_{RCC} . . . . . **-30 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . . **25 V**
Output ON Current, I_{OUT} . . . . . **50 mA**
Operating Temperature Range,
T_A . . . . . **-20°C to + 85°C**
Storage Temperature Range
T_S . . . . . **-65°C to +150°C**

Type UGN3235K Hall effect sensors are bipolar integrated circuits designed for commutation of brushless dc motors, and other rotary encoding applications using multi-pole ring magnets. The device features two outputs which are independently activated by magnetic fields of opposite polarity.

Each sensor IC includes a Hall voltage generator, two Schmitt triggers, a voltage regulator, output transistors, and on-board reverse polarity protection. The regulator enables these devices to operate from voltages ranging between 4.5 V and 24 V. On-chip compensation circuitry stabilizes the switch points over temperature.

Each open-collector output is independently operated by the proper amount and polarity of incident magnetic flux. Output 1 responds only to the positive flux from the south pole of a magnet, Output 2 to the negative flux from the north pole of a magnet. When the sensor experiences the field of a south magnetic pole greater than the maximum operate point of Output 1, that output switches to the LOW state and Output 2 is unaffected. When the incident flux falls below the minimum release point for Output 1, that output returns to the HIGH state and Output 2 remains unchanged.

Output 2 independently responds in the same manner to the negative flux from the north magnetic pole of a magnet. Figure 1 shows a zone in the region of 0 G, t_H, where both outputs are in the HIGH or OFF state. This constitutes a delay that is independent of rate of change of the incident magnetic field and ensures that both outputs are never ON simultaneously. This is an essential feature for driving brushless dc motors with a minimum of reactive transient currents.

The UGN3235K is supplied in a four-pin plastic single in-line package (SIP) measuring just 0.205" wide x 0.135" high x 0.060" thick (5.2 x 3.4 x 1.55 mm).

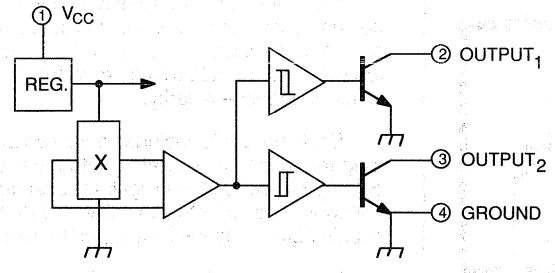
FEATURES

- Reliable and Rugged Magnetic Sensing Switch
- Two Outputs Independently Switched by North and South Poles
- Independent Actuation of Outputs Minimizes Inductive-Load Reactive Transient
- Built-in Hysteresis Minimizes Interference from Stray Fields
- Operates from 4.5 V to 24 V
- Outputs Compatible with All Logic Levels
- On-Board Reverse Polarity Protection
- Open-Collector, Active-Low Outputs

Always order by complete part number: **UGN3235K** .

3235
DUAL OUTPUT HALL EFFECT SWITCH

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-003A

ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}		4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{CC} = 24 V, I_{OUT} = 20 mA	—	160	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, V_{CC} = 24 V	—	—	1.0	µA
Supply Current	I_{CC}	V_{CC} = 24 V, Output Open	—	6.0	8.0	mA
Output Rise Time	t_r	V_{CC} = 14 V, R_L = 820 Ω, C_L = 20 pF	—	0.04	0.4	µs
Output Fall Time	t_f	V_{CC} = 14 V, R_L = 820 Ω, C_L = 20 pF	—	0.18	0.4	µs

MAGNETIC CHARACTERISTICS at V_{CC} = 4.5 V to 24 V

Characteristic	Test Conditions	Output	Min.	Max.	Units
Operate Point, B_{OP}	T_A = +25°C	Q1 Q2	50 -175	175 -50	G G
Operate Point, B_{OP}	T_A = -20°C to +85°C	Q1 Q2	35 -200	200 -35	G G
Release Point, B_{RP}	T_A = +25°C	Q1 Q2	25 -160	160 -25	G G
	T_A = -20°C to +85°C	Q1 Q2	15 -190	190 -15	G G
Hysteresis, B_H	T_A = +25°C	Q1 & Q2	15	100	G
	T_A = -20°C to +85°C	Q1 & Q2	15	110	G

OUTPUT SWITCHING CHARACTERISTICS

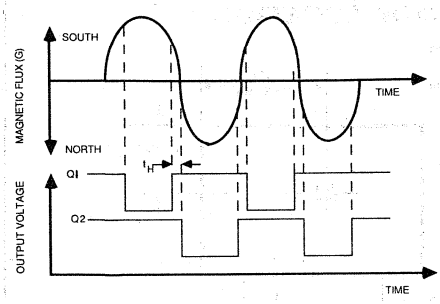


FIGURE 1

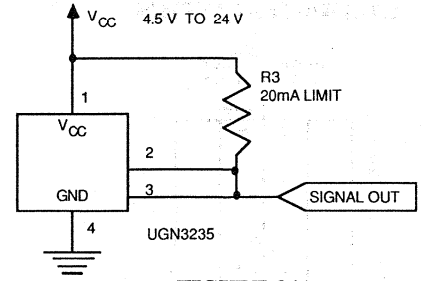


FIGURE 2A

MOTOR COIL DRIVER

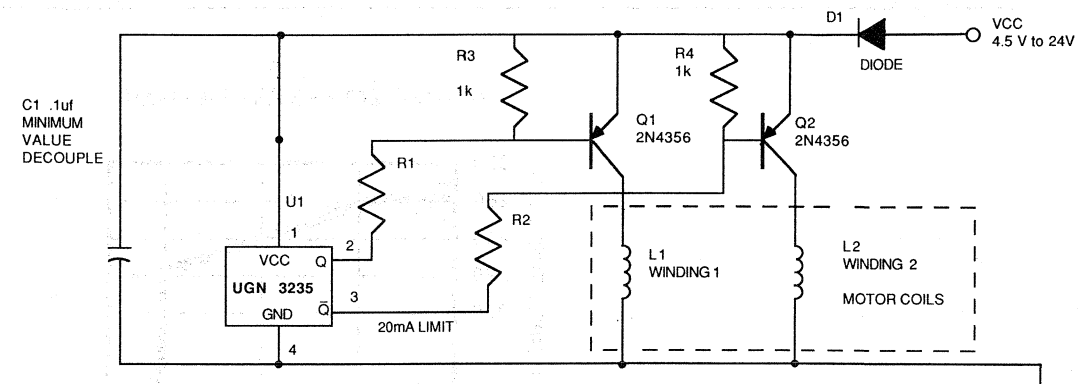
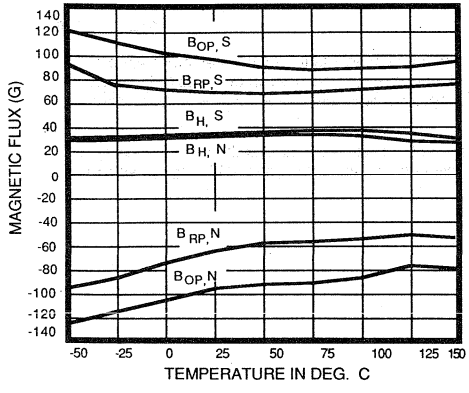


FIGURE 2B

SWITCH POINTS VERSUS TEMPERATURE



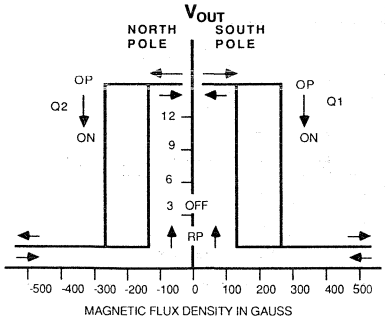
APPLICATIONS

Figure 2A gives a method of sensing the presence of either a north or south magnetic pole. Since the UGN3235K is an open collector device, it is possible to directly connect (OR-wire) the two outputs. This causes the output to go LOW when a north or south pole of sufficient magnitude is sensed.

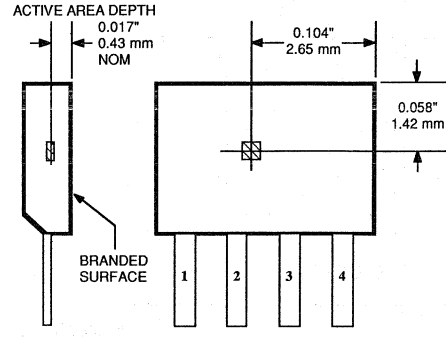
The device connected in this manner suits many applications, ranging from doubling the resolution of a ring-magnet encoder, to zero-crossing detection. Figure 1 shows that t_H is centered around the zero-G portion of the magnetic field plot. Thus, by decoding the HIGH portion of the UGN3235K OR-wired output, the zero-crossing can be encoded.

Figure 2B shows that the UGN3235K makes it possible to implement a very efficient brushless dc motor using a minimum number of components. Referring again to Fig. 1, the dead time (t_H) of the switching characteristics allow the motor coil fields to decay sufficiently. This avoids both excessive reactive voltages and the magnetic drag resulting from the motor coils working in opposition to each other.

HYSTERESIS CHARACTERISTICS

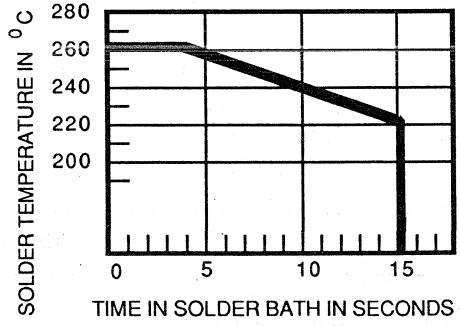


SENSOR LOCATION



Dwg. MH-001-1

GUIDE TO INSTALLATION

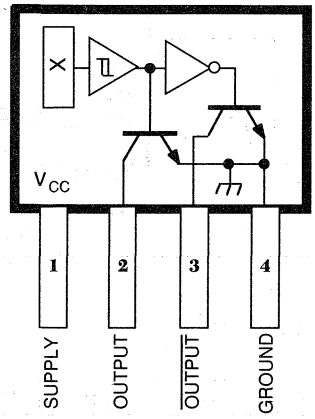


Dwg. No. A-12,062

1. All Hall effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package. Use of epoxy glue is recommended. Other types may deform the epoxy package.
2. To prevent permanent damage to the Hall cell, heat-sink the leads during hand soldering. Recommended maximum conditions for wave soldering are shown in the graph above.

3275

COMPLEMENTARY-OUTPUT HALL EFFECT LATCH



Dwg. PH-002

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . . **25 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . . **25 V**
Output ON Current, I_{OUT} . . . . . **50 mA**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Type UGN3275K latching Hall Effect sensors are bipolar integrated circuits designed for electronic commutation of brushless dc motors. They feature dual complementary outputs. The latches are typically used to sense matched magnetic flux densities of alternating polarity from multipole ring magnets.

Each sensor IC includes a Hall voltage generator, operational amplifier, Schmitt trigger, voltage regulator, and dual bipolar output transistors. The regulator allows use of the integrated circuit with supply voltages of 4.5 V to 24 V.

If the Hall cell is exposed to a magnetic flux density greater than the operate threshold (B_{OP}), OUTPUT goes low (turns ON) and $\overline{\text{OUTPUT}}$ goes high (turns OFF). The outputs will hold (latch) this state until magnetic field reversal exposes the Hall cell to a magnetic flux density below the release threshold (B_{RP}) when OUTPUT will go high (OFF) and $\overline{\text{OUTPUT}}$ will go low (ON). This state is also latched. Under any condition one output is ON while the other is OFF. Because the operating state switches only with magnetic field reversal, and not merely with a change in the strength, these integrated circuits qualify as true Hall effect latches.

Similar devices with a 500 mA continuous output current rating are available as the UGN5275K.

These complementary-output Hall Effect latches are supplied in a four-pin plastic SIP, 0.200" (5.08 mm) wide, 0.130" (3.3 mm) high, and 0.060" (1.54 mm) thick.

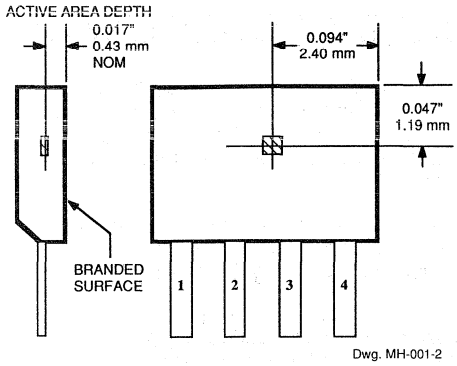
FEATURES

- Operable with Multipole Ring Magnets
- High Reliability
- Small Size
- Output Compatible with All Digital Logic Families
- 4.5 V to 24 V Operation
- High Hysteresis Level Minimizes Stray-Field Problems
- Complementary Outputs

Always order by complete part number: **UGN3275K** .

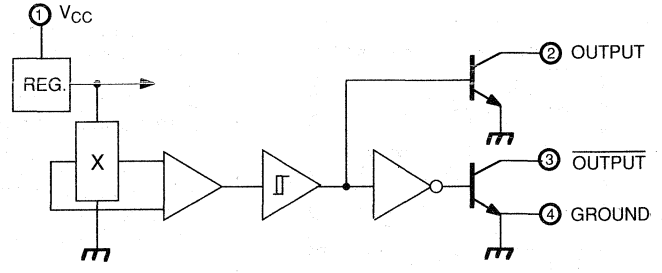
3275
COMPLEMENTARY OUTPUT HALL EFFECT LATCH

SENSOR LOCATION



Dwg. MH-001-2

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-002

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{CC} = 4.5 V, I_{OUT} = 20 mA, B > B_{OP}	—	—	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, V_{CC} = 24 V, B < B_{RP}	—	—	10	µA
Supply Current	I_{CC}	V_{CC} = 24 V, B < B_{RP}	—	—	7.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.04	0.4	µs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.18	0.4	µs

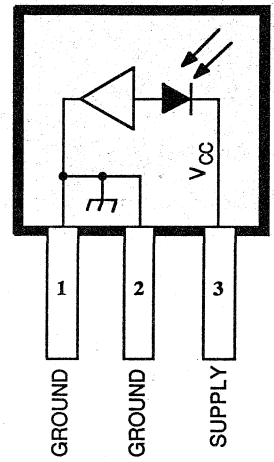
MAGNETIC CHARACTERISTICS

Characteristic	Symbol	T_A = +25°C		T_A = -20°C to +85°C		Units
		Min.	Max.	Min.	Max.	
Operate Point	B_{OP}	25	250	15	250	G
Release Point	B_{RP}	-250	-25	-250	-15	G
Hysteresis	B_H	100	—	100	—	G

NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention).

3311 AND 3312

PRECISION LIGHT SENSORS with calibrated Current Amplifiers



Dwg. PH-008

Direct replacements for photocells and phototransistors, the ULN3311T and ULN3312T precision light sensors are two-terminal monolithic integrated circuits that linearly convert light level into electrical current. The light-controlled current sources are linear over a wide range of supply voltages and light levels and require no external calibration.

Each precision light sensor (PLS) consists of a photodiode and a calibrated current amplifier. The design of the amplifier allows derivation of its supply current from the same terminal as the photodiode cathode and amplifier output. Since this supply current is a linear function of the photodiode current, it acts as part of the signal current. On-chip resistor-trimming techniques are used during manufacture to adjust each PLS to specified sensitivity. A 100 $\mu W/cm^2$ GaAlAs LED emission provides the light source for this calibration.

The ULN3311T and ULN3312T are supplied in an inexpensive clear plastic package. Both devices are rated for operation over the temperature range of -40°C to +70°C.

FEATURES

- Two-Terminal Operation
- Linear Over a Wide Range
- Precalibrated
- Wide Operating Voltage Range
- High Output

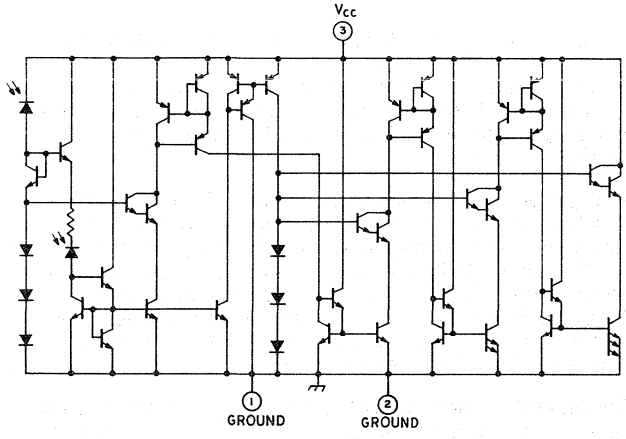
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **24 V**
Operating Temperature Range,
T_A . . . . . **-40°C to +70°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +110°C**

Always order by complete part number, e.g., **ULN3311T** .
See Characteristics table for differences between devices.

3311 AND 3312
PRECISION LIGHT SENSORS

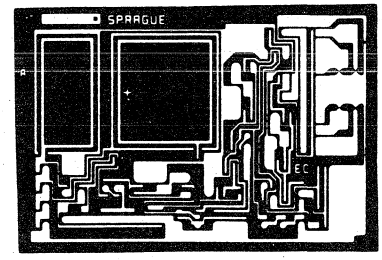
SCHEMATIC



Dwg. No. A-11,996

UNPACKAGED CHIP

0.053" x 0.077" (1.35 mm x 1.96 mm)



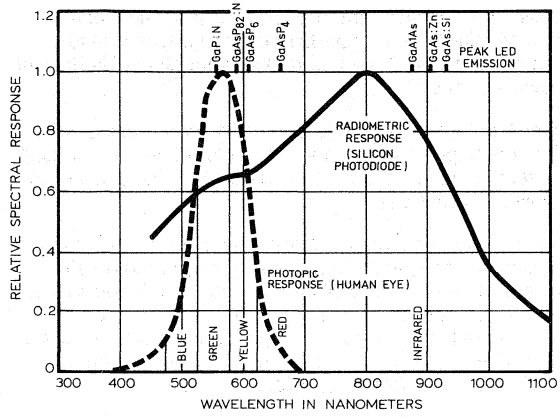
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 12 V

Characteristics	Device Type	Limits			Units
		Min.	Typ.	Max.	
Initial Accuracy at 100 μW/cm²	Both	—	—	±7.2	%
Sensitivity	ULN3311T	280	—	350	nA/μW/cm²
	ULN3312T	350	—	420	nA/μW/cm²
Operating Voltage Range	Both	2.7	12	24	V
Output Linearity, 10 to 10k μW/cm²	Both	—	—	±7.2	%
Dark Current	Both	—	—	100	nA
Power Supply Rejection, $(\Delta I_0/I_0)\Delta V$	Both	40	50	—	dB
Temperature Coefficient of Sensitivity	Both	—	3500	—	ppM/°C

NOTE: Light source is an infrared LED with a peak output wavelength of 880 nm.

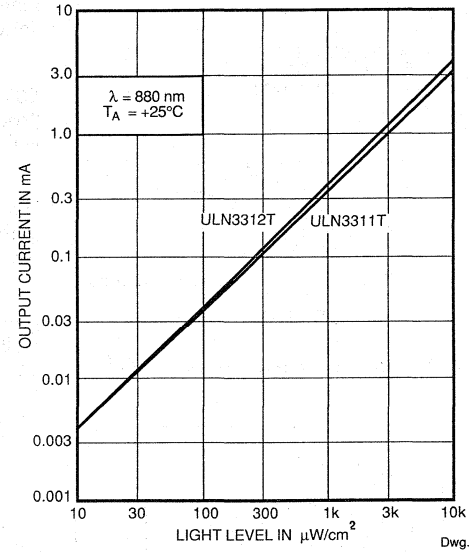
TYPICAL CHARACTERISTICS

RELATIVE SPECTRAL RESPONSE AS A FUNCTION OF WAVELENGTH OF LIGHT



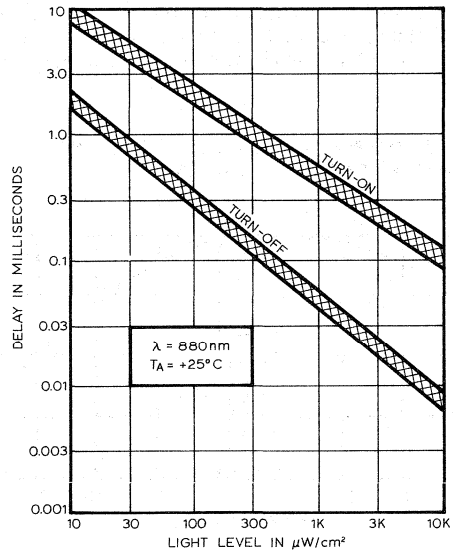
Dwg. No. A-12,135A

OUTPUT CURRENT AS A FUNCTION OF ILLUMINANCE



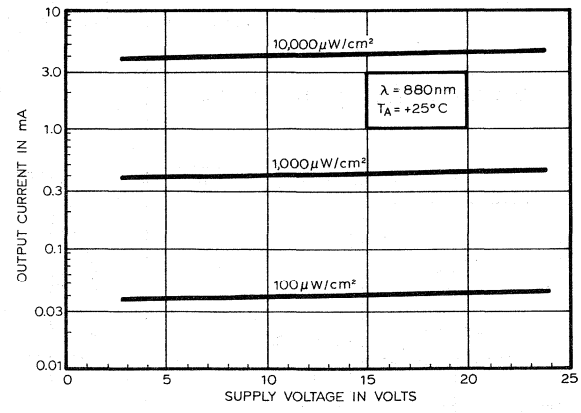
Dwg. GH-019

PROPABATION DELAY AS A FUNCTION OF ILLUMINANCE



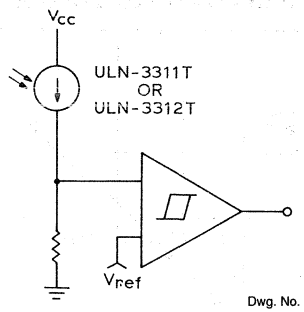
Dwg. No. A-12,138A

OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



Dwg. No. A-12,137A

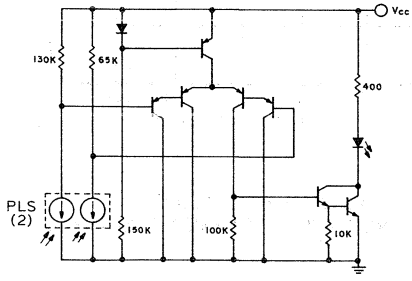
LIGHT-LEVEL DETECTOR USING PLS



Dwg. No. A-14,270

FIGURE 1

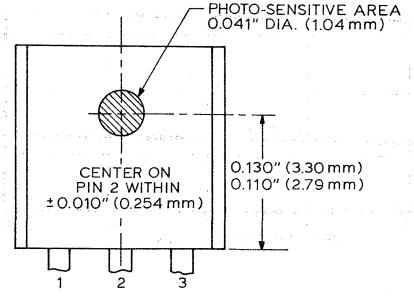
DIFFERENTIAL EDGE DETECTOR



Dwg. No. A-11,995

FIGURE 2

SENSOR-CENTER LOCATION



Dwg. No. A-14,275

APPLICATIONS INFORMATION

Photocells exhibit a change in resistance proportional to light intensity. However, they are highly inaccurate. They exhibit light memory, which makes their response dependent on the previous light level.

Phototransistors exhibit no light memory, but show as much as 50% variation in sensitivity among parts of the same type due to process and beta variations. Output current as a function of light level is linear only over a very small range.

Photodiodes have an output current that is a linear function of illumination, but the output is very small. The output current is typically in the range of tens of nanoamperes. These devices also show wide unit-to-unit sensitivity variations.

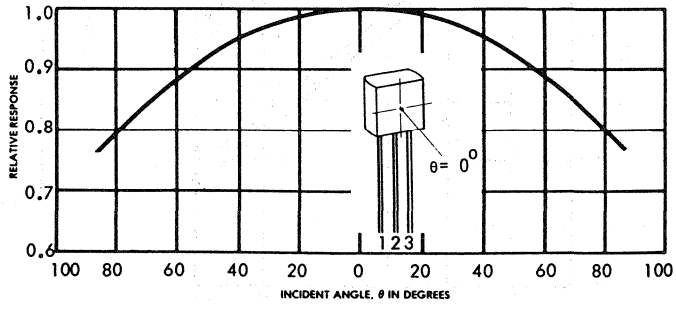
These precision light sensors are two-terminal replacements for photocells, phototransistors, and photodiodes. They are internally calibrated, have relatively high output currents, and are linear over a very wide range of light levels. Low-level amplifiers and adjustable controls can be eliminated. The precision light sensors are also ideal for use in arrays where matched characteristics are often required. Unpackaged chips are available on special order.

TYPICAL APPLICATIONS

Figure 1 shows a ULN3311T or ULN3312T integrated circuit replacing a photocell or phototransistor for the precise linear detection of a light level. Use of the precision light sensor eliminates the need for external calibration because it is calibrated to an initial accuracy of better than 7.2% during manufacture.

In Figure 2, two precision light sensors are used in a differential configuration to detect the edge of an object. When the light level on the first sensor is half of that on the second, the circuit switches. This circuit operates over a wide range of ambient light levels. No external calibration is required.

RELATIVE RESPONSE AS A FUNCTION OF THE ANGLE OF INCIDENCE

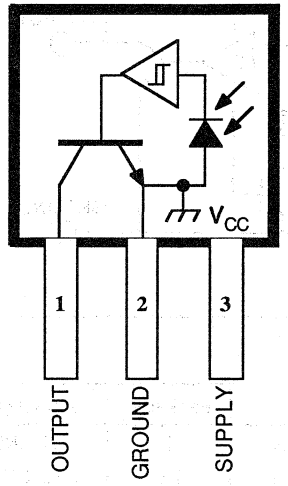


Dwg. No. A-12,134

3330, 3360, 3363

OPTOELECTRONIC SWITCHES

ULN3330/60/63T



Dwg. PH-009

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **15 V**
Output Voltage, V_{OUT} . . . . . **15 V**
Output Current, I_{OUT} . . . . . **25 mA**
Operating Temperature Range,
T_A . . . . . **-40°C to +70°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +110°C**

The ULN3330T/TA, ULN3360T, and ULN3363T optoelectronic switches provide light detection and low-level signal processing in single three-lead packages. The monolithic integrated circuits, requiring no external components, meet the need for cost-effective, light-sensing devices in consumer and industrial applications. Their high sensitivity makes them ideal for low-level light detection in optically noise-free environments.

Each optoelectronic IC includes a 0.030" x 0.030" (0.76 x 0.76 mm) photodiode, a high-gain current amplifier, a comparator with 12% hysteresis, output driver stage, and voltage regulator.

The ULN3330T/TA and ULN3360T switches turn ON as illumination of the photodiode falls below 55 $\mu W/cm^2$ at 880 nm. An internal latch provides hysteresis: The output turns OFF when illumination exceeds the turn-on threshold by approximately 12%.

The ULN3363T switch has an inverted output characteristic. It turns OFF as illumination falls below 55 $\mu W/cm^2$ at 880 nm; it remains OFF until increasing illumination at the photodiode typically reaches 62 $\mu W/cm^2$.

The ULN3330T/TA and ULN3363T have buffered open-collector outputs for current-sink applications. Typical loads include incandescent lamps, LEDs, sensitive relays, or dc motors.

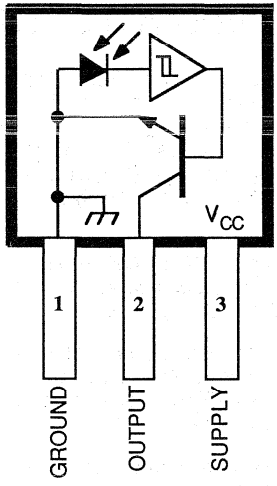
Output circuitry for the ULN3360T includes an internal 5.4 kΩ pull-up resistor that enables its direct use with microprocessors and TTL logic.

FEATURES

- Photodiode with:
  - On-Chip Amplifier
  - On-Chip Comparator with Hysteresis
  - On-Chip Power Driver
  - On-Chip Voltage Regulator
- Sensitive Switch Points
- Operation to 30 kHz

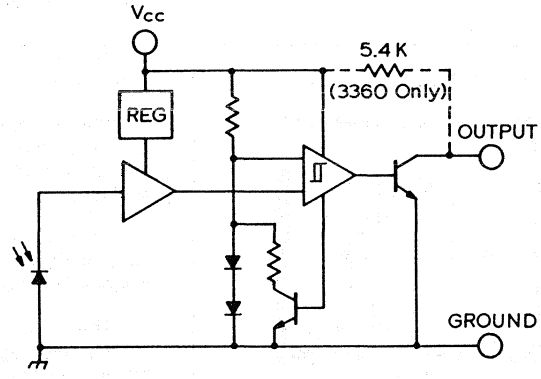
Always order by complete part number, e.g., **ULN3330T** .
See matrix on next page.

ULN3330TA



Dwg. PH-010

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,264

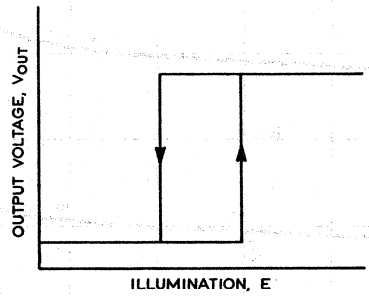
Device Type	Output	Package	Pinout (1-2-3)
ULN3330T	Open Collector	T	OUT-GND-V_{CC}
ULN3330TA	Open Collector	TA	GND-OUT-V_{CC}
ULN3360T	5.4 kΩ Pull-Up	T	OUT-GND-V_{CC}
ULN3363T	Inv. Open Collector	T	OUT-GND-V_{CC}

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 6.0 V, λ = 880 nm

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage Range	V_{CC}		4.0	6.0	15	V
Supply Current	I_{CC}		—	4.0	8.0	mA
Light Threshold Level	E_{ON}	Output ON	45	55	65	μW/cm²
	E_{OFF}	Output OFF	—	62	—	μW/cm²
Hysteresis	ΔE	$(E_{OFF} - E_{ON})/E_{OFF}$	10	13	16	%
Output ON Voltage	V_{OUT}	I_{OUT} = 15 mA	—	300	500	mV
		I_{OUT} = 25 mA	—	500	800	mV
Output OFF Current	I_{OUT}	V_{OUT} = 15 V	—	—	1.0	μA
Output Fall Time	t_f	90% to 10%	—	200	500	ns
Output Rise Time	t_r	10% to 90%	—	200	500	ns

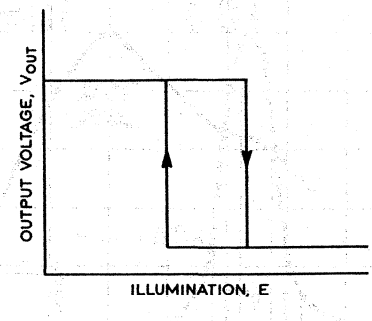
TYPICAL TRANSFER CHARACTERISTICS

ULN3330T/TA AND ULN3360T



Dwg. No. A-11,128

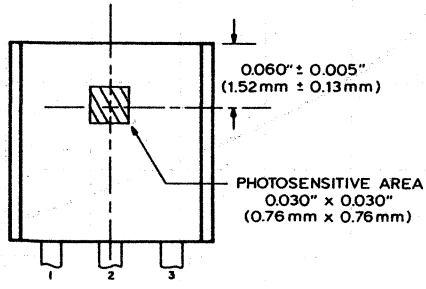
ULN3363T



Dwg. No. A-13,265

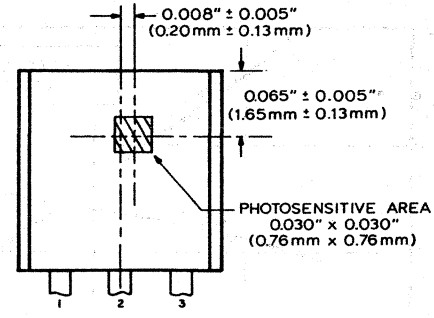
SENSOR LOCATIONS

SUFFIX 'T'



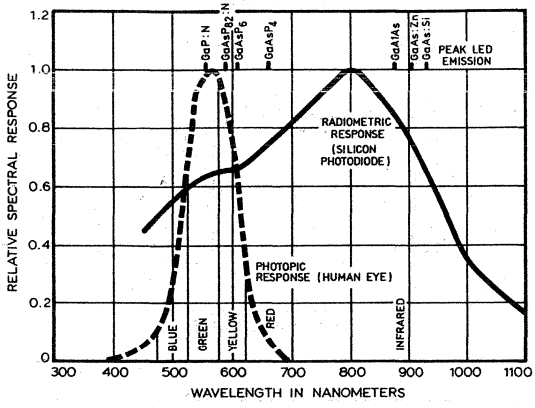
Dwg. No. A-13,301

SUFFIX 'TA'



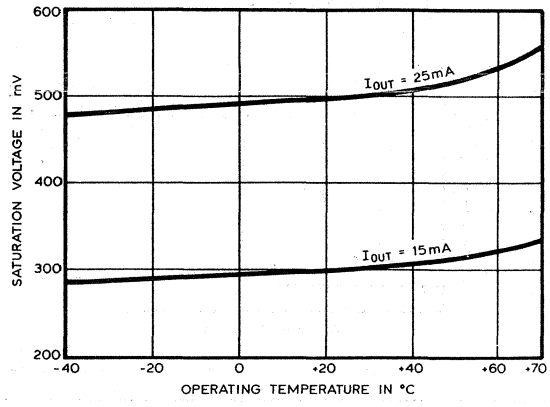
Dwg. No. A-11,994C

RELATIVE SPECTRAL RESPONSE AT T_A = +25°C AS A FUNCTION OF WAVELENGTH OF LIGHT



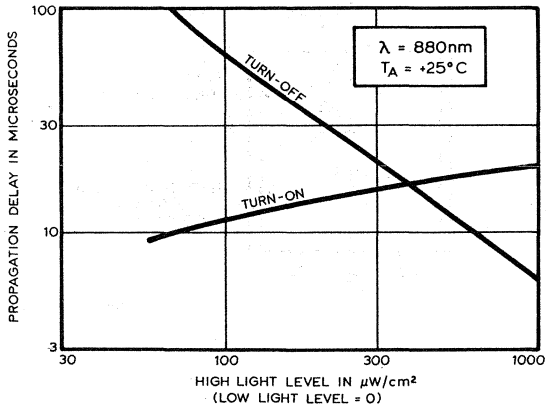
Dwg. No. A-12,135A

OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OPERATING TEMPERATURE



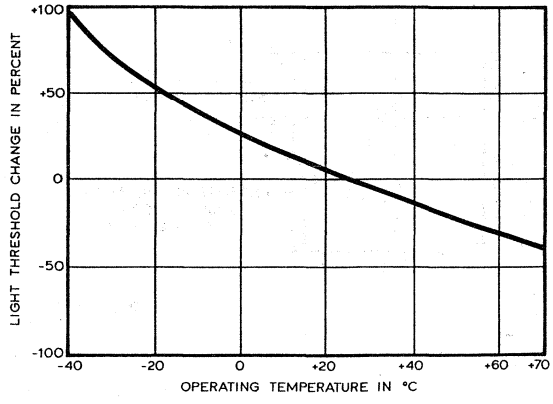
Dwg. No. A-12,307

PROPAGATION DELAY AS A FUNCTION OF LIGHT LEVEL



Dwg. No. A-12,308

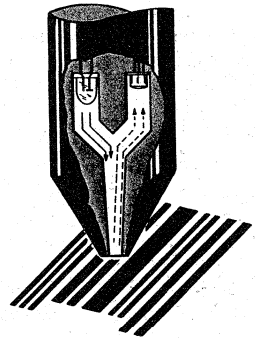
LIGHT-THRESHOLD CHANGE AS A FUNCTION OF OPERATING TEMPERATURE



Dwg. No. A-12,309

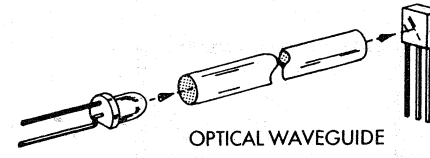
TYPICAL APPLICATIONS*

BAR CODE READER



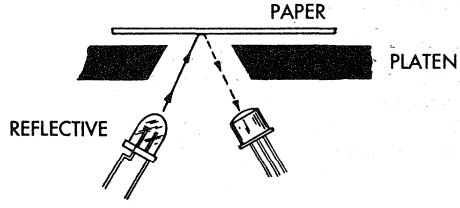
Dwg. No. A-13,266

OPTICAL ISOLATOR

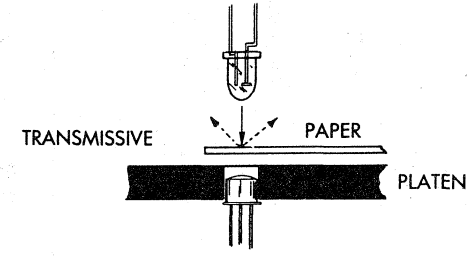


Dwg. No. A-13,267

SHEET DETECTOR

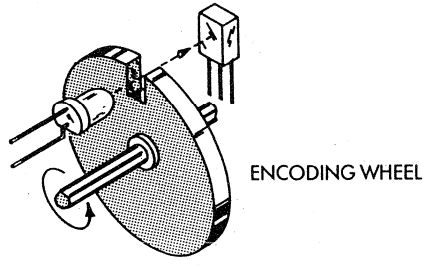


Dwg. No. A-13,268

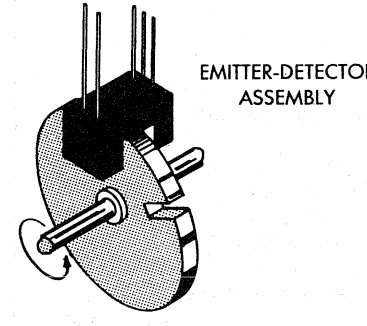


Dwg. No. A-13,269

OPTICAL ENCODER



Dwg. No. A-13,270

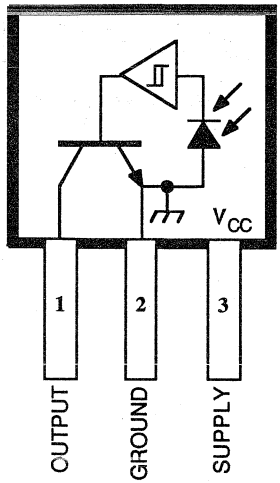


Dwg. No. A-13,271

*Optics and ambient light shields omitted for clarity.

3390

OPTOELECTRONIC SWITCH —TWILIGHT SENSOR



Dwg. PH-009

Designed for use in twilight sensing applications and in emergency and outdoor lighting, the ULN3390T optoelectronic switch is a monolithic integrated circuit containing a photodiode, low-level amplifier, comparator, voltage regulator, and output driver. The comparator is fabricated to give the sensor a built-in typical hysteresis value of 50 percent.

With temperature-compensated trip points, protection against damage by bright light, and increased hysteresis values, the ULN3390T represents a significant design improvement over previous optoelectronic switches. The integrated sensor is more stable over time and temperature than cadmium sulfide cell assemblies, requires fewer components, and has calibrated switching characteristics.

The UNL3390T switch typically turns ON as illumination falls below 10 $\mu W/cm^2$ at 880 nm. Internal hysteresis prevents deactivation until illumination exceeds 20 $\mu W/cm^2$. The switching points can be factory-adjusted to customer specifications.

FEATURES

- Photodiode with On-Chip
  - Amplifier
  - Comparator
  - Output Driver
  - Voltage Regulator
- 50% Hysteresis
- Temperature Compensation

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **25 V**
Output Voltage, V_{OUT} . . . . . **25 V**
Output Current, I_{OUT} . . . . . **25 mA**
Operating Temperature Range,
T_A . . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +110°C**

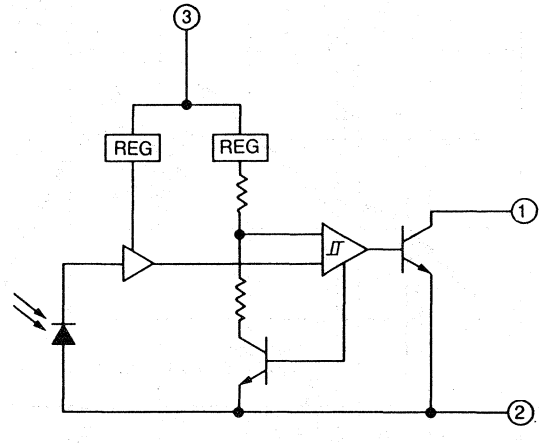
Always order by complete part number: **ULN3390T** .

3390
OPTOELECTRONIC SWITCH

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 6 V (unless otherwise noted).

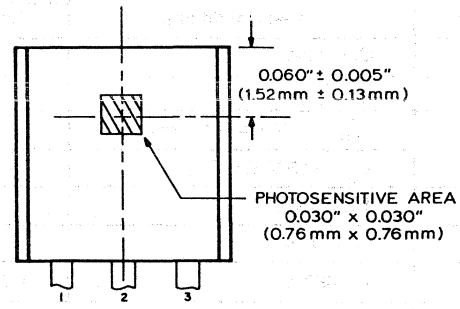
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	Operating	4.0	—	16	V
Supply Current	I_{CC}	$E > E_{OFF}$	—	3.0	10	mA
Output Saturation Voltage	$V_{OUT(sat)}$	I_{OUT} = 15 mA, $E \leq 6\ \mu W/cm^2$	—	300	500	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 15 V, $E > E_{OFF}$	—	0.1	10	µA
Output Rise Time	t_r	10% to 90%	—	200	500	ns
Output Fall Time	t_f	90% to 10%	—	200	500	ns
Light Threshold Level	E_{ON}	λ = 880 nm	6.0	10	14	$\mu W/cm^2$
	E_{OFF}	λ = 880 nm	—	20	—	$\mu W/cm^2$
Hysteresis	ΔE	$(E_{OFF}-E_{ON})/E_{OFF}$	45	50	65	%

FUNCTIONAL BLOCK DIAGRAM



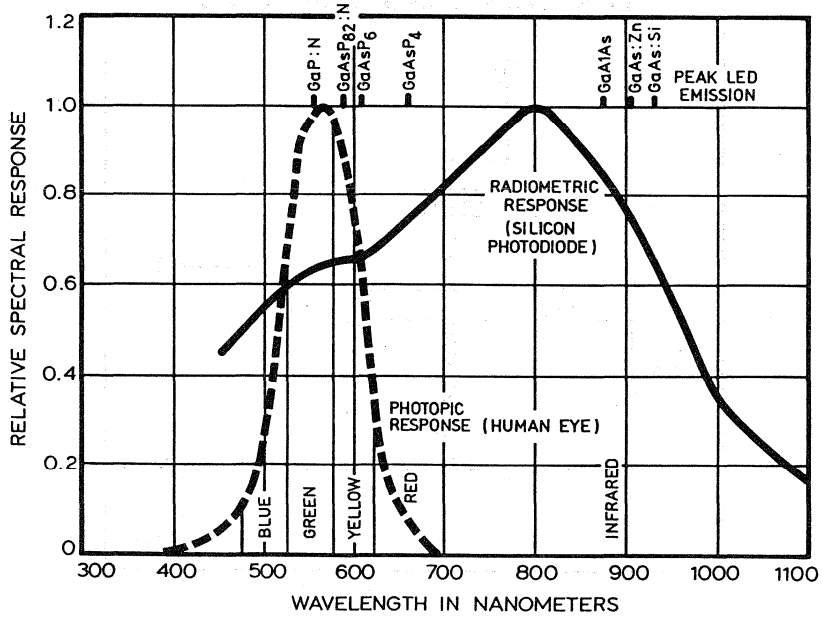
Dwg. W-154

SENSOR-CENTER LOCATION



Dwg. No. A-13,301

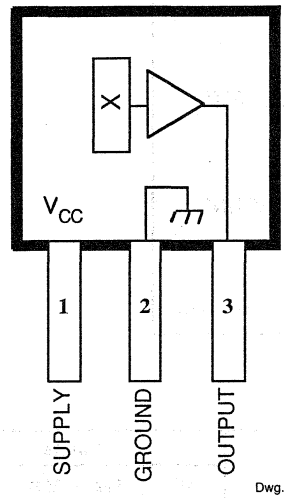
RELATIVE SPECTRAL RESPONSE AT T_A = +25°C AS A FUNCTION OF WAVELENGTH OF LIGHT



Dwg. No. A-12,135A

3501

LINEAR OUTPUT HALL EFFECT SENSORS



Dwg. PH-006

Pinning is shown viewed from branded side.

Utilizing the Hall effect for sensing a magnetic field, UGN3501U and UGN3501UA integrated circuits provide a linear single-ended output that is a function of magnetic field intensity.

These devices can sense relatively small changes in a magnetic field — changes that are too small to operate a Hall effect switch. They can be capacitively coupled to an amplifier, to boost the output to a higher level.

The UGN3501U/UA include a Hall cell, linear amplifier, emitter-follower output, and a voltage regulator. Integrating the Hall cell and the amplifier into one monolithic device minimizes problems related to the handling of millivolt analog signals.

Both devices are rated for continuous operation over the temperature range of 0°C to +70°C and over a supply voltage range of 8 V to 12 V.

FEATURES

- Excellent Sensitivity
- Flat Response to 25 kHz (typ.)
- Internal Voltage Regulation
- Excellent Temperature Stability

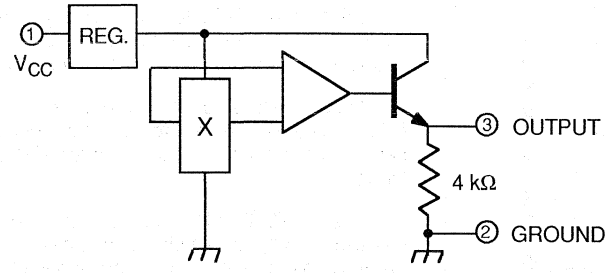
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **16 V**
Output Current, I_{OUT} . . . . . **4 mA**
Magnetic Flux Density, B . . . . . **Unlimited**
Operating Temperature Range,
T_A . . . . . **0°C to +70°C**
Storage Temperature Range,
T_S . . . . . **- 65°C to +150°C**

Always order by complete part number:

Part Number	Package
UGN3501U	3-Pin Mini-SIP
UGN3501UA	3-Pin Ultra-Mini-SIP

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-006

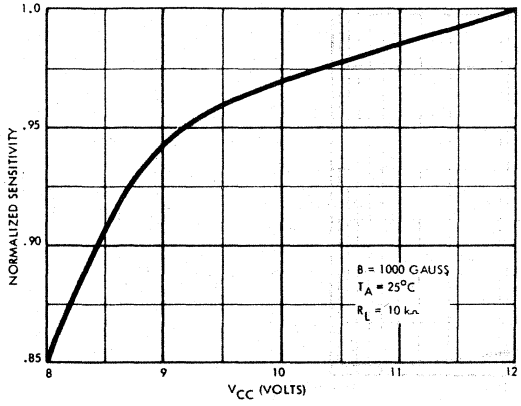
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 12 V

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operating Voltage	V_{CC}		8.0	—	12	V
Supply Current	I_{CC}	V_{CC} = 12 V	—	10	20	mA
Quiescent Output Voltage	V_{OUT}	B = 0 G, Note 1	2.5	3.6	5.0	V
Sensitivity	ΔV_{OUT}	B = 1000 G, Notes 1, 2	0.35	0.7	—	mV/G
Frequency Response	BW	f_H - f_L at - 3 dB	—	25	—	kHz
Broadband Output Noise	e_n	f = 10 Hz to 10 kHz	—	0.1	—	mV
Output Resistance	R_0		—	100	—	Ω

NOTE 1. All output voltage measurements are made with a voltmeter having an input impedance of 10 kΩ or greater.

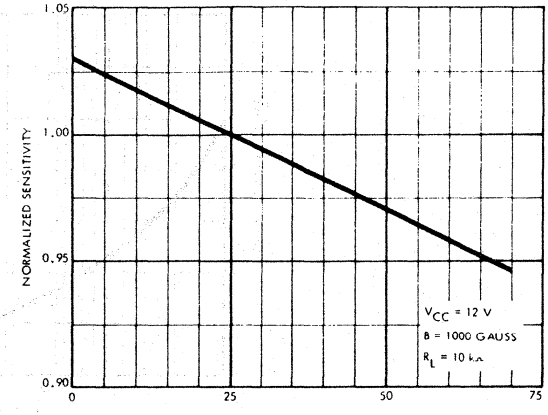
NOTE 2. Magnetic flux density is measured at the most sensitive area of the device, which is 0.017" ± 0.001" (0.43 ± 0.03 mm) below the branded side of the "U" package.

NORMALIZED SENSITIVITY AS A FUNCTION OF V_{CC}



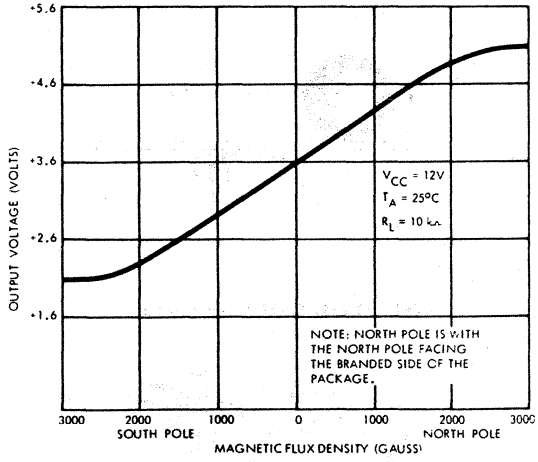
Dwg. No. A-10,522

NORMALIZED SENSITIVITY AS A FUNCTION OF TEMPERATURE



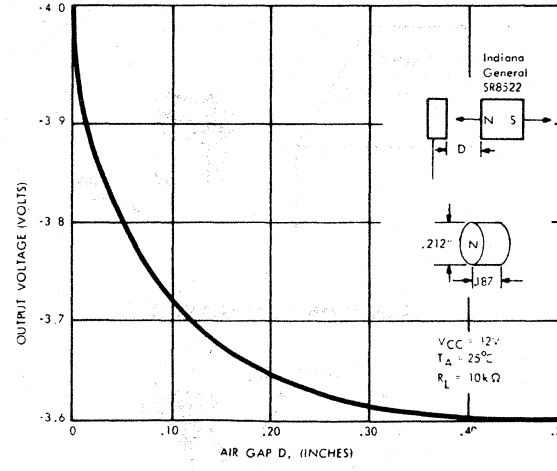
Dwg. No. A-10,521

OUTPUT VOLTAGE AS A FUNCTION OF MAGNETIC FLUX DENSITY



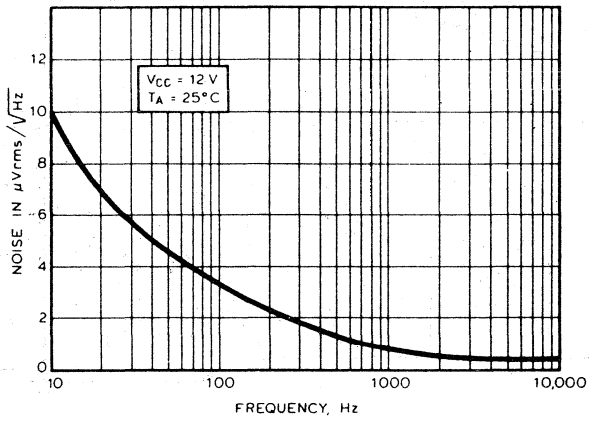
Dwg. No. A-10,523

OUTPUT VOLTAGE AS A FUNCTION OF AIR GAP



Dwg. No. A-10,519

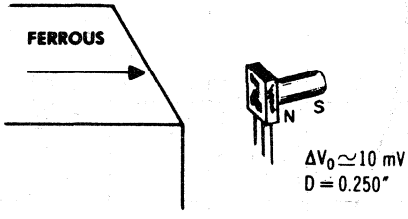
NOISE SPECTRAL DENSITY AS A FUNCTION OF FREQUENCY



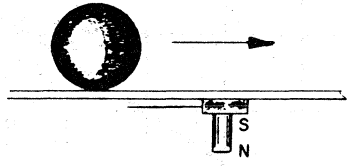
Dwg. No. A-10,520A

TYPICAL APPLICATIONS

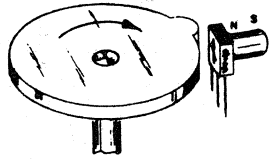
SENSITIVE PROXIMITY DETECTOR



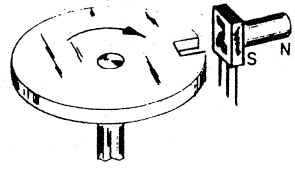
FERROUS METAL SENSOR



LOBE OR COG SENSOR



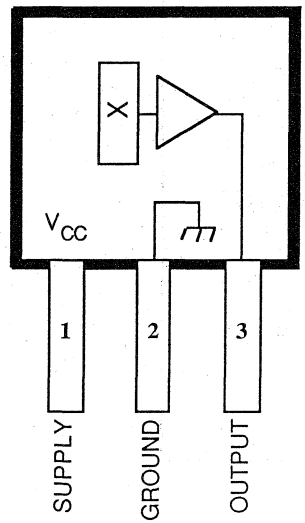
NOTCH OR HOLE SENSOR



For reference only - an Alnico VIII permanent magnet, 0.212" (5.38 mm) in diameter and 0.187" (4.75 mm) long is approximately 800 gauss at the surface. A samarium cobalt permanent magnet, 0.100" (2.54 mm) square and 0.040" (1:02 mm) thick is approximately 1200 gauss at its surface.

3503

RATIOMETRIC, LINEAR HALL EFFECT SENSORS



Dwg. PH-006

Pinning is shown viewed from branded side.

Type UGN3503U/UA and UGS3503U/UA Hall effect sensors accurately track extremely small changes in magnetic flux density—changes generally too small to operate Hall effect switches.

As motion detectors, gear tooth sensors, and proximity detectors, they are magnetically driven mirrors of mechanical events. As sensitive monitors of electromagnets, they can effectively measure a system's performance with negligible system loading while providing isolation from contaminated and electrically noisy environments.

Each Hall effect integrated circuit includes a Hall sensing element, linear amplifier, and emitter-follower output stage. Problems associated with handling tiny analog signals are minimized by having the Hall cell and amplifier on a single chip.

The UGN3503U and UGN3503UA are rated for continuous operation over the temperature range of -20°C to +85°C. The UGS3503U and UGS3503UA operate over an extended temperature range of -40°C to +125°C.

FEATURES

- Extremely Sensitive
- Flat Response to 23 kHz
- Low-Noise Output
- 4.5 V to 6 V Operation
- Magnetically Optimized Package

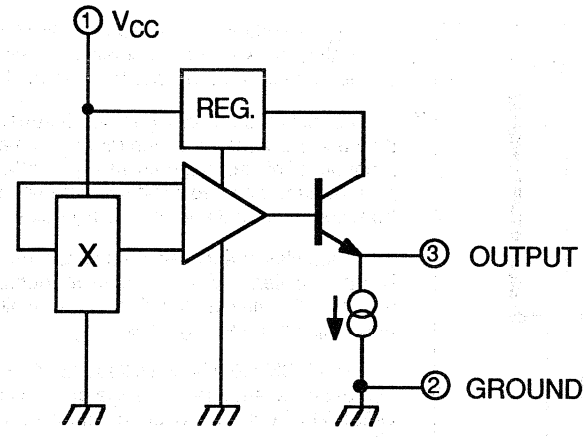
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **8 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Operating Temperature Range, T_A
UGN3503U/UA. . . . . **-20°C to +85°C**
UGS3503U/UA . . . . . **-40°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Always order by complete part number:

Part Numbers	Operating Temp.	Package
UGN3503U UGN3503UA	-20°C to +85°C	3-Pin Mini-SIP 3-Pin Ultra-Mini-SIP
UGS3503U UGS3503UA	-40°C to +125°C	3-Pin Mini-SIP 3-Pin Ultra-Mini-SIP

FUNCTIONAL BLOCK DIAGRAM

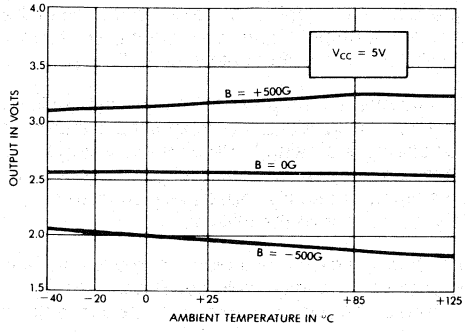


ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 5 V

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Voltage	V_{CC}		4.5	—	6.0	V
Supply Current	I_{CC}		—	9.0	14	mA
Quiescent Output Voltage	V_{OUT}	B = 0 G	2.25	2.50	2.75	V
Sensitivity	ΔV_{OUT}	B = 0 G to ±900 G	0.75	1.30	1.72	mV/G
Bandwidth (-3 dB)	BW		—	23	—	kHz
Broadband Output Noise	V_{out}	BW = 10 Hz to 10 kHz	—	90	—	µV
Output Resistance	R_{OUT}		—	50	—	Ω

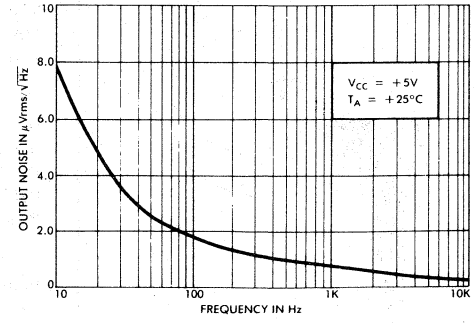
All output-voltage measurements are made with a voltmeter having an input impedance of at least 10 kΩ.
Magnetic flux density is measured at most sensitive area of device located 0.016" ±0.002" (0.41 mm ±0.05 mm) below the branded face of the 'U' package.

OUTPUT VOLTAGE AS A FUNCTION OF TEMPERATURE



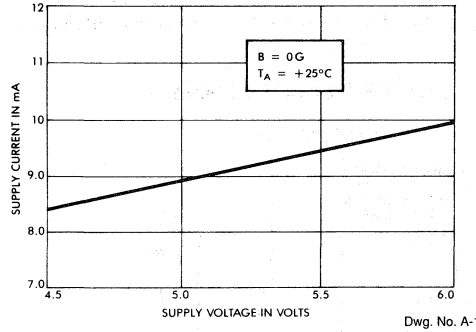
Dwg. No. A-12,573

OUTPUT NOISE AS A FUNCTION OF FREQUENCY



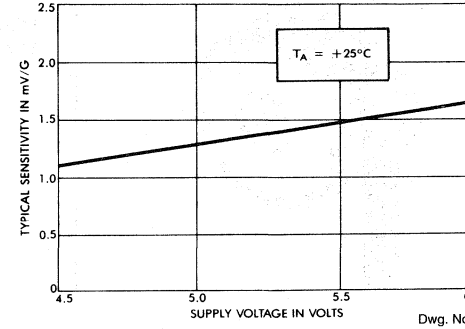
Dwg. No. A-12,505

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



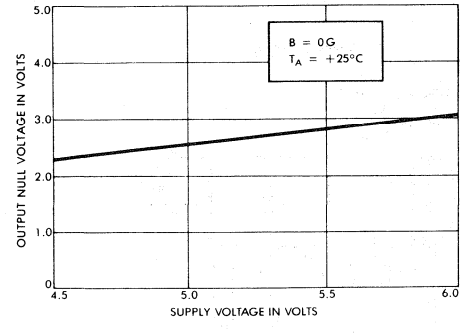
Dwg. No. A-12,506

DEVICE SENSITIVITY AS A FUNCTION OF SUPPLY VOLTAGE



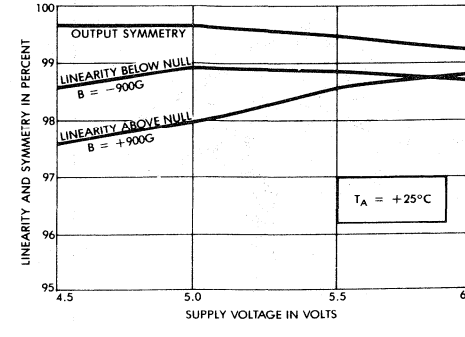
Dwg. No. A-12,507

OUTPUT NULL VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



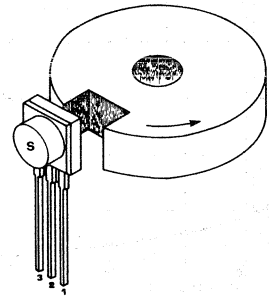
Dwg. No. A-12,508

LINEARITY AND SYMMETRY AS A FUNCTION OF SUPPLY VOLTAGE



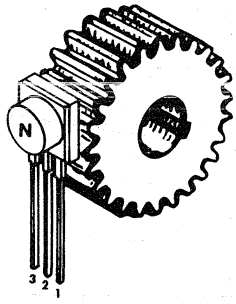
Dwg. No.. A-12,509

NOTCH SENSOR



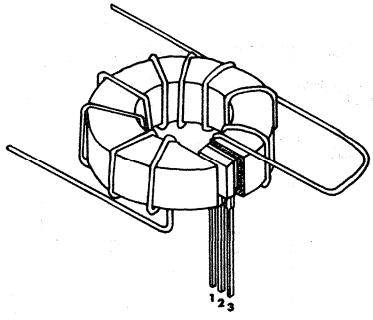
Dwg. No. A-12,574

GEAR TOOTH SENSOR



Dwg. No. A-12,512

CURRENT MONITOR



Dwg. No. A-12,513

OPERATION

The output null voltage (B = 0 G) is nominally one-half the supply voltage. A south magnetic pole, presented to the branded face of the Hall effect sensor will drive the output higher than the null voltage level. A north magnetic pole will drive the output below the null level.

In operation, instantaneous and proportional output-voltage levels are dependent on magnetic flux density at the most sensitive area of the device. Greatest sensitivity is obtained with a supply voltage of 6 V, but at the cost of increased supply current and a slight loss of output symmetry. The sensor's output is usually capacitively coupled to an amplifier that boosts the output above the millivolt level.

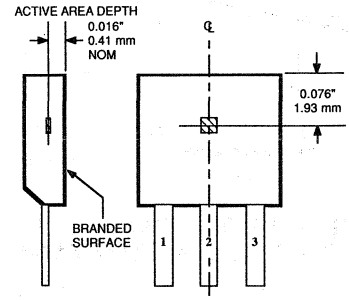
In two applications shown, a permanent bias magnet is attached with epoxy glue to the back of the epoxy package. The presence of ferrous material at the face of the package acts as a flux concentrator.

The south pole of a magnet is attached to the back of the package if the Hall effect IC is to sense the presence of ferrous material. The north pole of a magnet is attached to the back surface if the integrated circuit is to sense the absence of ferrous matrial.

Calibrated linear Hall devices, which can be used to determine the actual flux density presented to the sensor in a particular application, are available.

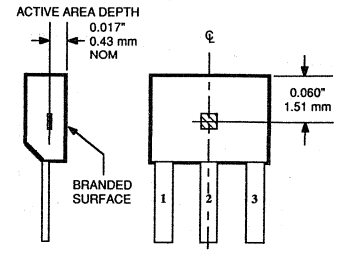
SENSOR LOCATIONS

SUFFIX "U"



Dwg. MH-002-5

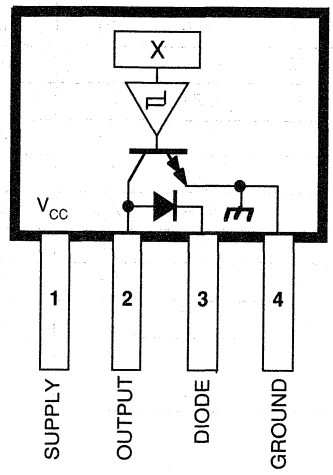
SUFFIX "UA"



Dwg. MH-011-3

5140

PROTECTED POWERHALL® SENSOR — LAMP/SOLENOID DRIVER



Pinning is shown viewed from branded side.

Dwg. PH-001

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} . . . . . **28 V**
Reverse Battery Voltage, V_{RCC} . . . . . **-45 V**
Output OFF Voltage, V_{OUT} . . . . . **45 V**
Over-Current Protected Output Voltage, V_{OUT} . . . . . **25 V**
Output ON Current, I_{OUT} . . . . . **900 mA***
Magnetic Flux Density, B . . . . . **Unlimited**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-40°C to +85°C**
Storage Temperature Range, T_S . . . . . **-65°C to +150°C**

* Output is current limited at approximately 900 mA and junction temperature limited if current in excess of 900 mA is attempted. See Circuit Description and Applications for further information.

The UGQ5140K unipolar Hall effect switch is a monolithic integrated circuit designed for magnetic actuation of low-power incandescent lamps or inductive loads such as relays or solenoids. Included on chip is a Darlington power output that is capable of continuously sinking in excess of 300 mA. Internal protection circuitry limits surge (lamp turn-ON) or fault currents to approximately 900 mA. A sensitive magnetic threshold allows the device to be used in conjunction with inexpensive magnets or in applications that require relatively large operating distances.

Each sensor/driver includes a magnetic sensing Hall voltage generator, operational amplifier, Schmitt trigger, voltage regulator, and an open-collector, high-gain Darlington power output stage. The regulator allows use of the device with supply voltages of 4.5 V to 28 V. On-chip compensation circuitry stabilizes switch-point performance over temperature. The magnetic operation of this device is similar to that of the UGN3140U Hall effect switch.

The sensitive magnetic switch point coupled with the power output, current limiting, and thermal limiting circuitry allow the UGQ5140K to magnetically actuate various loads without requiring any external components.

The UGQ5140K is rated for operation over an extended temperature range of -40°C to +85°C. It is supplied in a four-pin mini-SIP plastic package, 0.200" (5.08 mm) wide, 0.130" (3.30 mm) high, and 0.060" (1.54 mm) thick.

FEATURES

- Magnetically Actuated Power Switch
- Temperature-Compensated Switch Points
- High Current Sink Capability
  - 300 mA Continuous
  - 900 mA Peak Current Limit
- Output Short Circuit Protection
- Low Quiescent Standby Current
- Linear Thermal Limiting
- Automotive Temperature Range
  - -40°C to +85°C, Operating
- Internal Inductive Flyback/Clamp Diode Protection
- Reverse Battery Protection
- Low-Profile 4-Pin Mini-SIP

Always order by complete part number: **UGQ5140K** .

5140
PROTECTED POWERHALL® SENSOR

ELECTRICAL CHARACTERISTICS at T_A = -40°C to +85°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted).

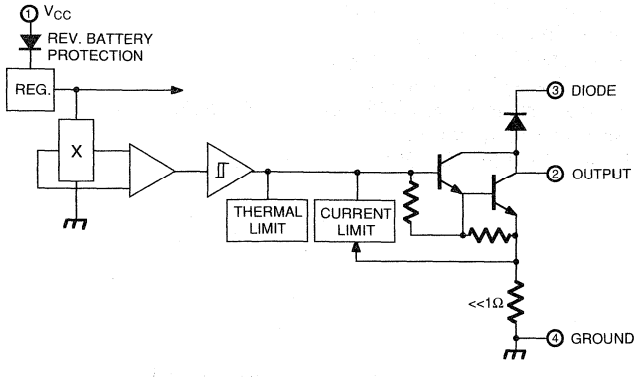
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	Operating	4.5	12	24	V
Output Leakage Current	I_{OUT}	V_{OUT} = 24 V	—	<1.0	10	µA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA	35	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 300 mA, V_{CC} = 24 V	—	0.84	1.2	V
Over-Current Limit	I_{LIMIT}	V_{CC} = V_{OUT} = 12 V, B ≥ 500 G	—	900	—	mA
Output Rise Time	t_r	V_{CC} = 12 V, V_{BB} = 18 V,	—	0.04	2.0	µs
Output Fall Time	t_f	R_L = 1.1 kΩ, C_L = 20 pF	—	0.04	2.0	µs
Supply Current	I_{CC}	Output OFF	—	5.5	10	mA
Diode Forward Voltage	V_F	I_F = 300 mA	—	1.1	1.5	V
Diode Leakage Current	I_R	V_R = 35 V	—	<1.0	50	µA
Thermal Limit	T_{LIMIT}	V_{CC} = V_{OUT} = 12 V, B ≥ 500 G, I_{OUT} = 10 mA	—	165	—	°C

Typical Data is at T_A = +25°C and is for design information only.

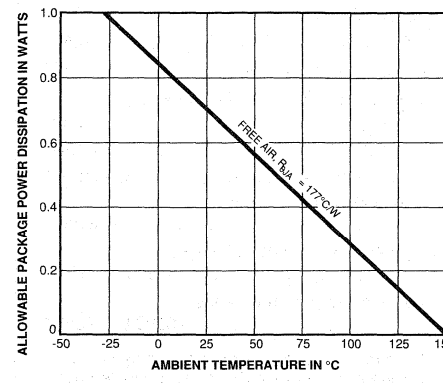
MAGNETIC CHARACTERISTICS at V_{CC} = 4.5 V to 24 V.

Characteristic	Symbol	T_A = +25°C			T_A = -40°C to +85°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Magnetic Operate Point	B_{OP}	70	155	200	45	—	240	G
Magnetic Release point	B_{RP}	50	100	180	25	—	220	G
Hysteresis	B_H	20	55	—	20	—	—	G

FUNCTIONAL BLOCK DIAGRAM

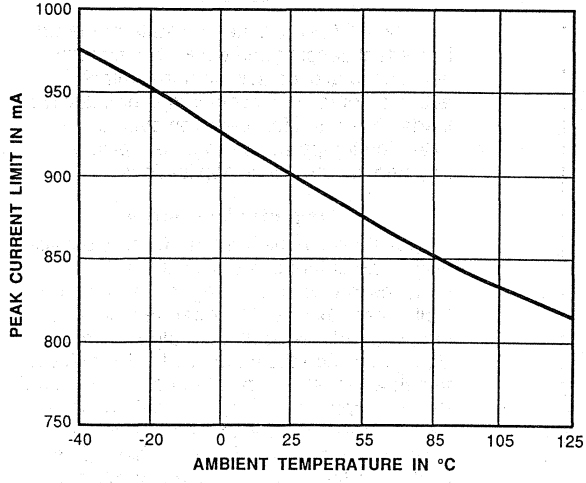


Dwg. FH-001

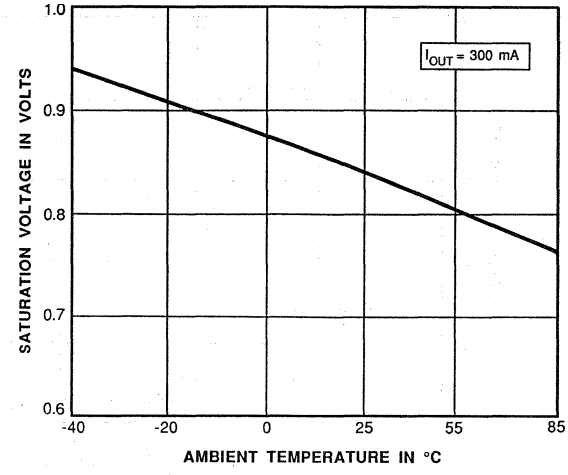


Dwg. GH-001

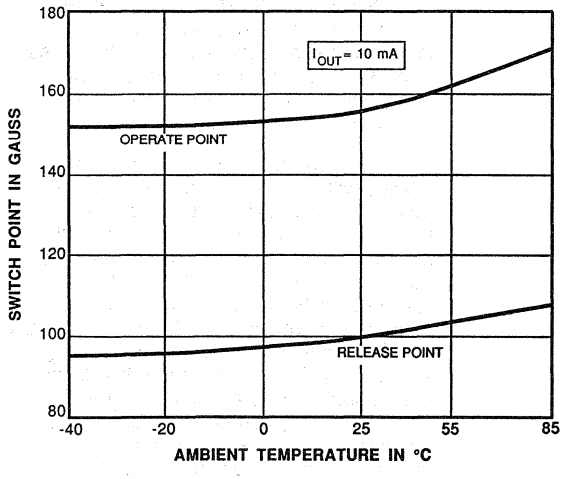
TYPICAL OPERATING CHARACTERISTICS



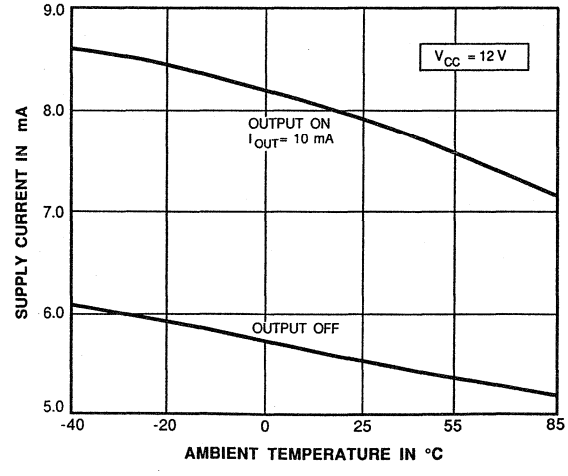
Dwg. GH-004



Dwg. GH-002

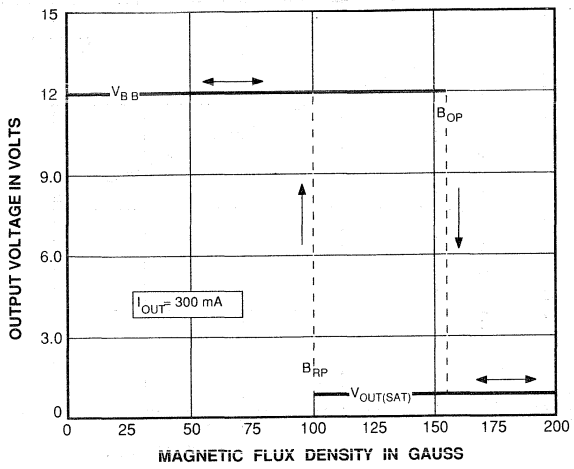


Dwg. GH-006



Dwg. GH-003

TYPICAL TRANSFER CHARACTERISTICS at T_A = +25°C



Dwg GH-007

CIRCUIT DESCRIPTION AND OPERATION

The UGQ5140K merges state-of-the-art Hall effect sensing and power driving technologies to allow precision non-contact actuation of incandescent lamps or inductive loads. It is rated for operation over an extended temperature range as typically required in automotive applications.

Magnetic Operation

As shown in the Transfer Characteristics graph, the output of the device (pin 2) switches low when the magnetic field at the Hall sensor exceeds the operate point threshold (B_{OP}). At this point, the output voltage is $V_{OUT(SAT)}$. When the magnetic field is reduced to below the release point threshold (B_{RP}), the device output goes high. The difference in the magnetic operate and release points is called the hysteresis (B_H) of the part. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Current and Thermal Limiting

Output short circuits may be caused by faulty connectors, crimped wiring harnesses, or blown loads. In such cases, current and thermal limit circuitry will protect the output transistor against destruction.

Current through the output transistor is sensed with a low-value on-chip aluminum resistor. The voltage drop across this resistor is fed back to control the base drive of the output stage. This feedback prevents the output transistor from exceeding its maximum current density rating by limiting the output current to approximately 900 mA. It may also cause the output voltage to increase ($V_{OUT} = V_{BB} - [I_{LIMIT} \times R_L]$). In this mode, the device will dissipate an increased amount of power ($P_D = V_{OUT} \times I_{LIMIT}$) and the output transistor will be thermally stressed. This stress, unless protected against (as in the UGQ5140K), will cause the device junction temperature to rise until it fails catastrophically.

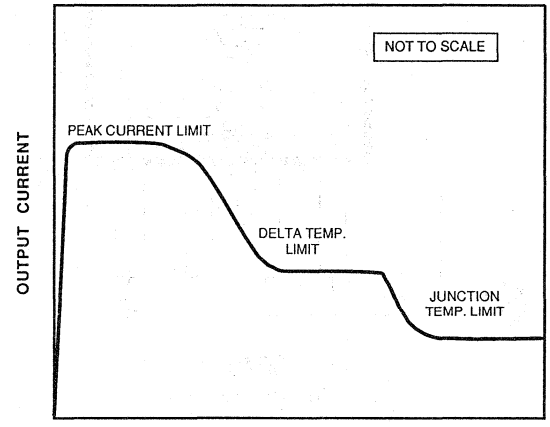
Thermal stress protection is provided in two manners; delta temperature protection, and junction temperature protection. Under worst-case conditions (see Figures 1 and 2), if the output is shorted to supply, the output transistor will heat up much faster than the rest of the integrated circuit. This condition could cause localized failure in the output transistor. To prevent damage, a delta temperature limiting scheme is used. If a large thermal gradient is sensed across the device, the output transistor base drive is reduced to lower the output current. This reduces the power (heat) generated by the output transistor.

When thermal stresses cause the junction temperature to reach approximately +165°C, a linear thermal limiting circuit is activated. This circuit linearly reduces the base drive of the output transistor to maintain a constant junction temperature of 165°C. In this mode, the output current will be a function of the heat dissipating characteristics of the package and its environment. Linear thermal limiting eliminates the low-frequency thermal oscillation problems experienced by thermal shutdown (ON-OFF) schemes.

The output characteristics are shown in Figures 1 and 2. Note the three distinct operating regions: peak limit, delta limit, and thermal limit. In practice the output voltage and current may exhibit some oscillations during peak current limiting due to output load characteristics. These oscillations are of very-short duration (typically 50 ms) and may be damped with an external capacitor between pins 2 and 4.

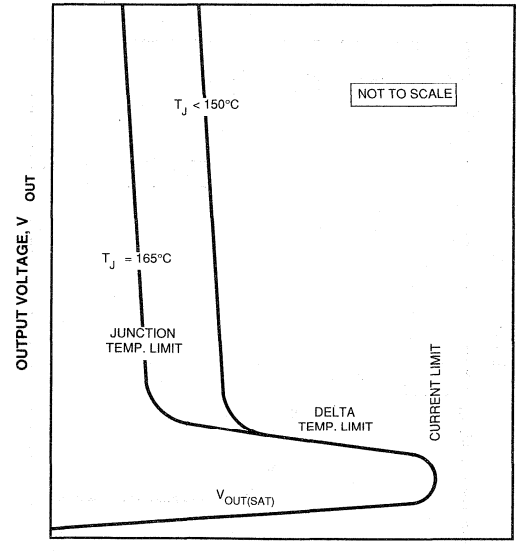
When the fault condition that caused the output overload is corrected, the device returns to normal operating mode.

FIGURE 1
OUTPUT CURRENT UNDER SHORT-CIRCUIT CONDITIONS



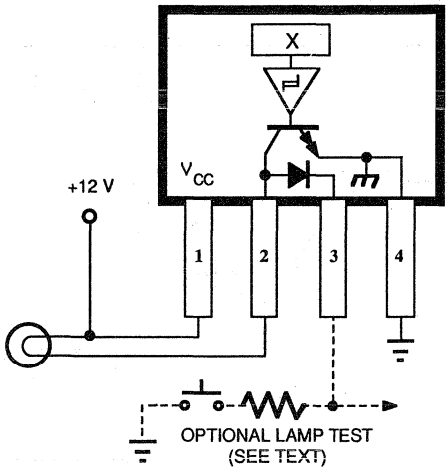
Dwg. WH-002

FIGURE 2
OUTPUT VOLTAGE vs OUTPUT CURRENT



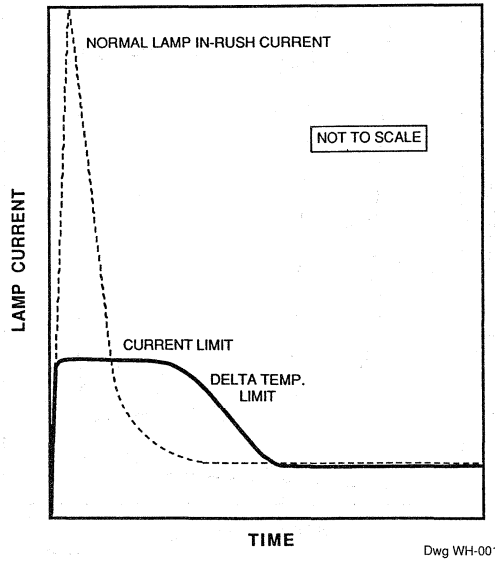
Dwg. GP-013-1

FIGURE 3
TYPICAL LAMP DRIVER APPLICATION



Dwg. EH-001

FIGURE 4
LAMP CURRENT vs TIME



Dwg WH-001

TYPICAL APPLICATIONS

Incandescent Lamp Driver

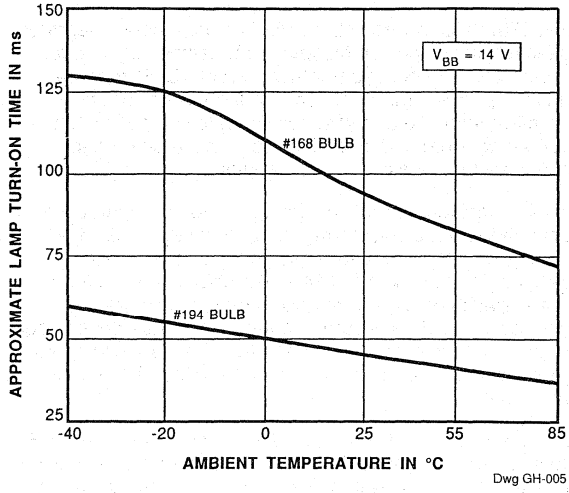
High incandescent lamp turn-ON currents (commonly called in-rush currents) can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warming resistors protect both driver and lamp but use significant power when the lamp is OFF while current-limiting resistors waste power when the lamp is ON. Lamps with steady-state current ratings to 300 mA can be driven by the UGQ5140K (Figure 3) without the need for warming or current limiting resistors. In applications using several sensor/drivers to control multiple lamps, the internal clamp diodes may be connected together to an appropriate current-limiting resistor and simple "lamp test" switch.

As shown in Figure 4, when an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and will normally allow a 10x to12x peak in-rush current. As the lamp warms up, the filament resistance increases to its rated value and the lamp current is reduced to its steady-state rating. When switching a lamp with the UGQ5140K, the internal current-limiting circuitry limits the peak current to approximately 900 mA. The device will stay in the current limit and delta temperature limit modes until the lamp resistance increases to its rated steady-state value (Figure 4). A side-effect of this current-limiting feature is that lamp turn-on times will increase. Typical lamp turn-on times are shown in Figure 5.

Inductive Load Driver

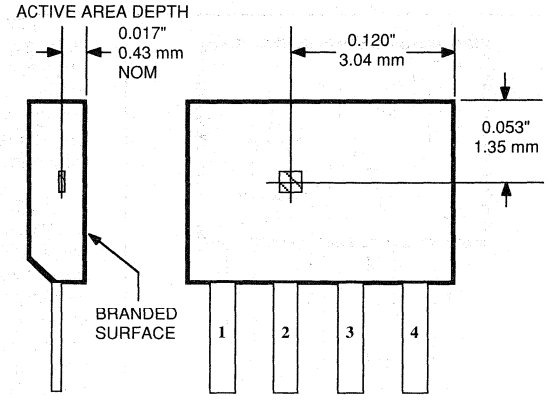
Connecting the internal clamp diode (pin 3) to the positive supply allows relays or other inductive loads to be driven directly, as shown in Figure 6. The internal diode prevents damage to the output transistor by clamping the high-voltage spikes which occur when turning OFF an inductive load. An optional external Zener diode can be used to increase the flyback voltage, providing a much faster inductive load turn-OFF current decay, resulting in faster dropout (reduced relay contact arcing), and improved performance. The maximum Zener voltage, plus the load supply voltage, plus the clamp diode forward voltage should not exceed 35 volts.

FIGURE 5
LAMP TURN-ON TIME



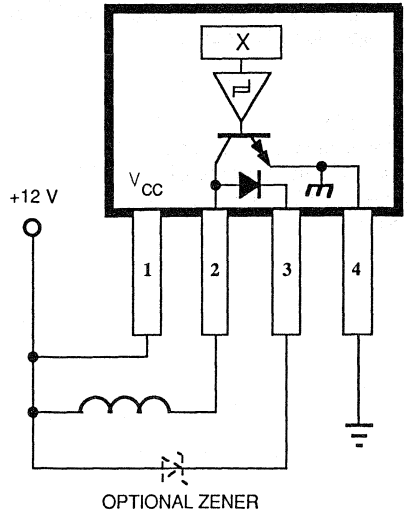
Dwg GH-005

SENSOR LOCATION AREA

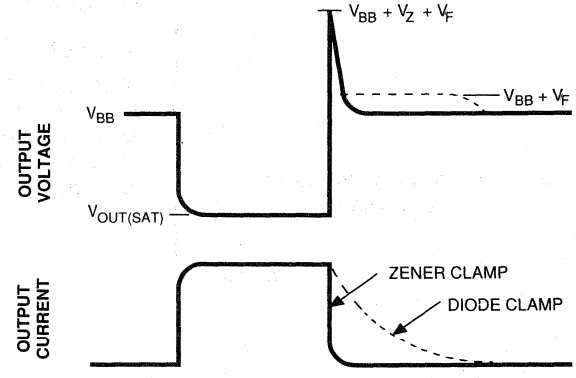


Dwg. MH-001A

FIGURE 6
TYPICAL RELAY/SOLENOID DRIVER APPLICATION



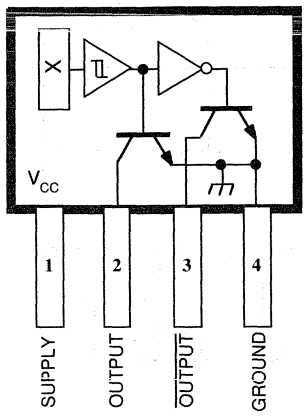
Dwg. EH-002



Dwg. WP-001-1

5275

COMPLEMENTARY OUTPUT POWER HALL™ LATCH



Dwg. PH-002

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} . . . . . **14 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Output OFF Voltage, V_{CE} . . . . . **60 V**
Output ON Current, I_C
Continuous . . . . . **0.5 A**
Peak (Start Up) . . . . . **0.9 A**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**
Package Power Dissipation,
P_D . . . . . **750 mW**

Type UGN5275K latching Hall effect sensors are bipolar integrated circuits designed for electronic commutation of brushless dc motors. They feature open-collector complementary power outputs that are capable of sinking up to 300 mA continuously. Increased current ratings, complementary outputs, and sensitive switching points that are stable over temperature and time ideally suit these devices for minimum-component brushless dc motor designs.

Each sensor IC includes a Hall voltage generator, an operational amplifier, a Schmitt trigger, a voltage regulator, and large-area dual NPN output transistors. The regulator enables the IC to operate with supply voltages ranging from 4.5 V to 14 V. On-chip compensation circuitry stabilizes switch point performance over temperature. The large bipolar junction output transistors are fed by a unique driver stage which minimizes power dissipation within the IC. The magnetic operation of this device is similar to that of the UGN3275K complementary-output Hall effect latch.

Output Q of the IC switches to the LOW state when the internal Hall generator experiences a magnetic field that exceeds the rated operate point. Output $\overline{Q}$ switches HIGH within one µs of the Output Q change of state. When the device is exposed to a sufficient magnetic field of opposite polarity, Output Q returns to the HIGH state, and Output $\overline{Q}$ returns to the LOW state.

The UGN5275K is rated for operation over a temperature range of -20°C to +85°C, and is supplied in an environmentally rugged, four-pin miniature plastic SIP. Please consult the factory for alternate packaging and custom magnetic requirements.

FEATURES

- High Sink-Current Capability
- Magnetic Sensing, Complementary-Output Latch
- On-Chip Schmitt Trigger Provides Hysteresis
- Temperature-Compensated Switch Points
- Rugged, Low-Profile SIP

Always order by complete part number: **UGN5275K** .

5275
COMPLEMENTARY OUTPUT POWERHALL™ LATCH

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 14 V (unless otherwise noted).

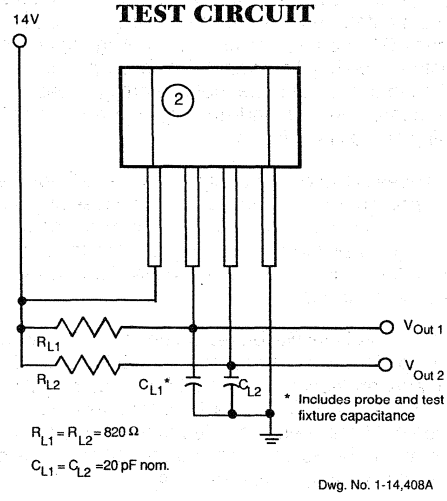
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}		4.5	—	14	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{CC} = 14 V, I_C = 300 mA	—	400	600	mV
Output Leakage Current	I_{CEX}	V_{CE} = 14 V, V_{CC} = 14 V	—	—	10	µA
Supply Current	I_{CC}	V_{CC} = 14 V, Output Open	—	18	30	mA
Output Rise Time	t_r	V_{CC} = 14 V, R_L = 45 Ω, C_L = 20 pF	—	0.3	1.5	µs
Output Fall Time	t_f	V_{CC} = 14 V, R_L = 45 Ω,C_L = 20 pF	—	0.3	1.5	µ
Switch Time Differential	Δt	V_{CC} = 14 V, R_L = 45 Ω, C_L = 20 pF	—	1.0	3.0	µs

MAGNETIC CHARACTERISTICS

Characteristic	Symbol	T_A = +25°C		T_A = -20°C to +85°C		Units
		Min.	Max.	Min.	Max.	
Operate Point	B_{OP}	25	250	15	250	G
Release Point	B_{RP}	-250	-25	-250	-15	G
Hysteresis	B_{hys}	100	—	100	—	G

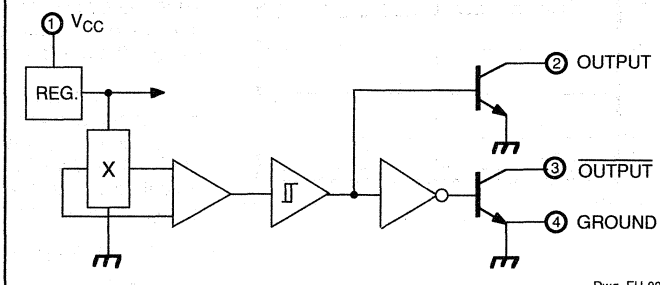
NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention).

TEST CIRCUIT



Dwg. No. 1-14,408A

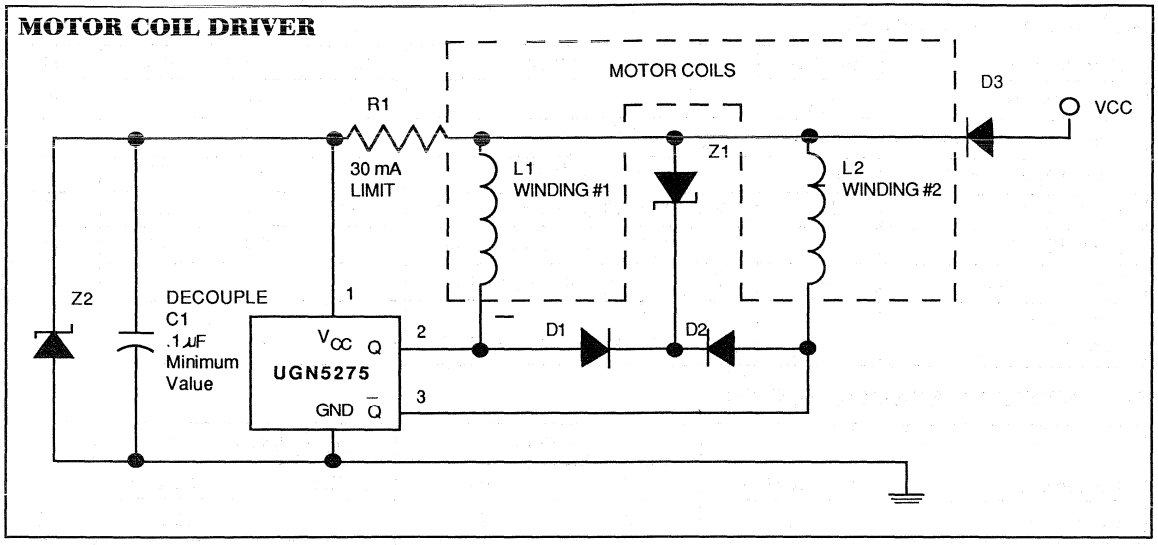
FUNCTIONAL BLOCK DIAGRAM



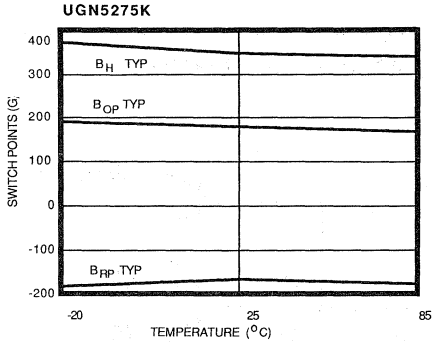
Dwg. FH-002

FIGURE 2

MOTOR COIL DRIVER



SWITCH POINTS VERSUS TEMPERATURE



APPLICATIONS

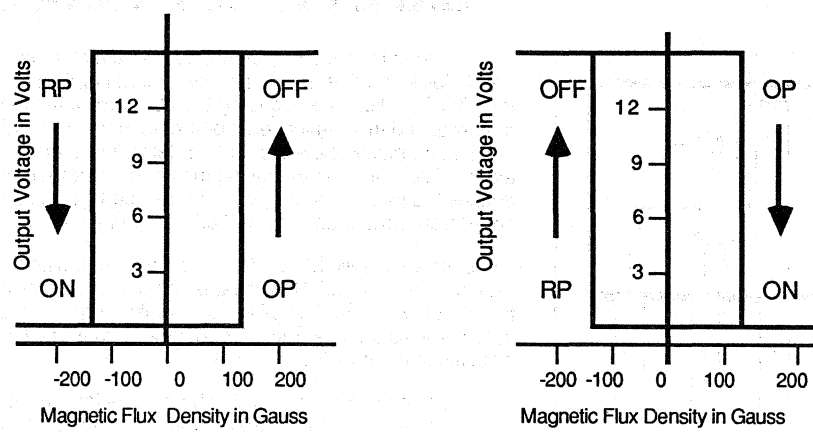
The increased current sinking capability of the UGN5275K ideally suits it for building small, inexpensive brushless dc motors using a minimum number of external components. Figure 2 shows that the only components required to commutate motor windings L1 and L2 are the Hall effect IC, flyback diodes D1 and D2, and one decoupling capacitor. The remaining components are optional for improving motor performance. Care should be taken to ensure that the motor winding impedances are high enough to guarantee that start-up surge currents do not exceed the maximum rating of the Hall effect IC.

In the circuit shown, diodes D1 and D2 supply a flyback path for the current of each winding to prevent reactive voltages from exceeding the sustained voltage rating of the Hall-effect IC output transistors. Zener diode Z1 enables the windings to switch more rapidly by allowing the output voltage to rise above the source voltage, while simultaneously clamping the extreme reactive voltages.

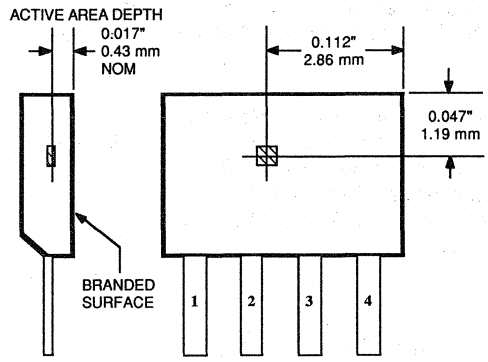
The maximum output voltage level will be restricted to the following: $V_{CC} - V_{D3} + V_Z + V_{D1}$ (blocking diode D3 voltage drop). Blocking diode D3 provides reverse input-polarity protection, and should be used only if reverse battery voltage is a possibility. Capacitor C1 decouples the Hall-effect IC from any high dv/dt transients injected onto the V_{CC} rail to prevent regulator latch-up within the device. Zener diode Z2 and resistor R1 are required for operation from a V_{CC} exceeding 14 V.

5275
COMPLEMENTARY OUTPUT POWERHALL™ LATCH

HYSTERESIS CHARACTERISTICS

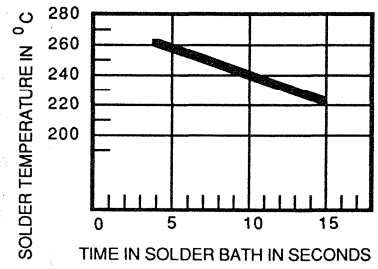


SENSOR LOCATION



Dwg. MH-001-3

GUIDE TO INSTALLATION



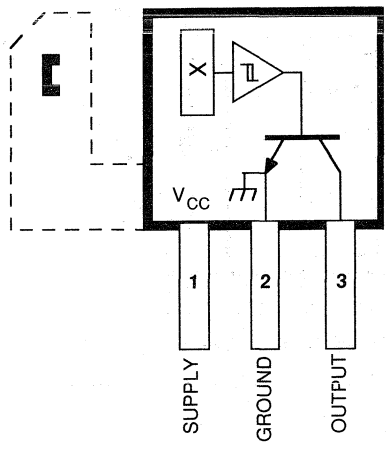
Dwg. No. A-12,062

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package. Use of epoxy glue is recommended. Other types may deform the epoxy package.

2. To prevent permanent damage to the Hall cell, heat-sink the leads during hand-soldering. Recommended maximum conditions for wave soldering are shown in the graph above.

6450

HALL EFFECT VANE SWITCH



Dwg. PH-004

A rugged magnetically activated Hall-effect vane switch, the UMN6450X can directly replace less robust optical equivalents. Ideal for critical applications requiring the ability to withstand hostile electrical, chemical and mechanical environments, each vane switch is housed in a miniature plastic package that contains and protects the magnet and electronic circuitry. The housing includes a channel which precisely defines the path of vane travel. The device is available for through-board assemblies, and is supplied with a digital output.

Each vane switch includes on a single monolithic chip, a voltage regulator, a quadratic Hall voltage generator, temperature compensation circuitry, a signal amplifier, a Schmitt trigger and an open collector output transistor. The Hall effect device is optimized for the magnet installed in the housing.

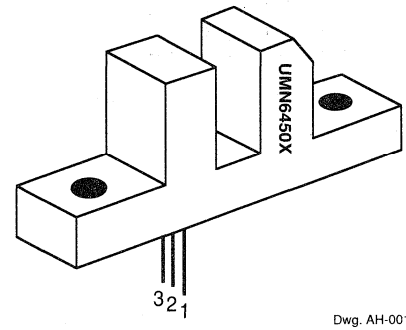
The Schmitt trigger provides hysteresis for turn-on and turn-off of the switch output for greater immunity to noise and imperfections in the vane. The on-chip regulator allows operation from supplies of 4.5 to 24 V. The switch output can sink up to 20 mA. The output can directly interface with bipolar and MOS logic circuits.

The UMN6450X is rated for operation over the industry-standard temperature range of -20°C to +85°C.

The UMN6450X is packaged in a three-pin plastic housing with 0.050" (1.27 mm) lead spacing ready for circuit-board mounting.

FEATURES

- More Rugged Replacement for Optical Vane Switch
- Reliable and Repeatable—No Mechanical Contacts to Wear Out
- On-Chip Schmitt Trigger Provides Hysteresis
- Temperature-Compensated Switch Points
- Digital Output Compatible with All Logic Families
- 4.5 to 24 V Operation



Dwg. AH-001

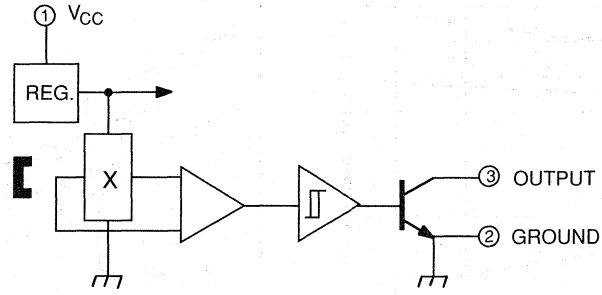
ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Supply Voltage, V_{CC} . . . . . **25 V**
Output OFF Voltage, V_{OUT} . . . . . **25 V**
Output ON Current, I_{OUT} . . . . . **25 mA**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +125°C**

Always order by complete part number: **UMN6450X** .

6450
DIGITAL VANE SWITCH

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-005-1

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5 V

Switching characteristics are determined using a 1030 steel vane with dimensions of 0.035" x 0.50" (0.89 x 12.7 mm). The vane is centered laterally between the vertical faces of the slot at a height of 0.080" (3.81 mm) from the bottom of the slot.

Switch Output Low-to-High, RRP, LRP ..... **0.015" ±0.030" (0.38 mm ±0.76 mm)[1]**
Switch Output High-to-Low, ROP, LOP ..... **0.030" ±0.030" (0.76 mm ±0.76 mm)[2]**
Hysteresis, LOP - LRP, ROP - RRP ..... **0.008" (0.2 mm) min.**
Repeatability ..... **±0.001" (0.025 mm) max.**
Symmetry [3]
- Output High, LOP - ROP ..... **±0.005" (0.13 mm) typ.**
- Output Low, LRP - RRP ..... **±0.005 " (0.13 mm) typ.**
- Hysteresis, (LOP - LRP) - (ROP - RRP) ..... **±0.002" (0.05 mm) max.**

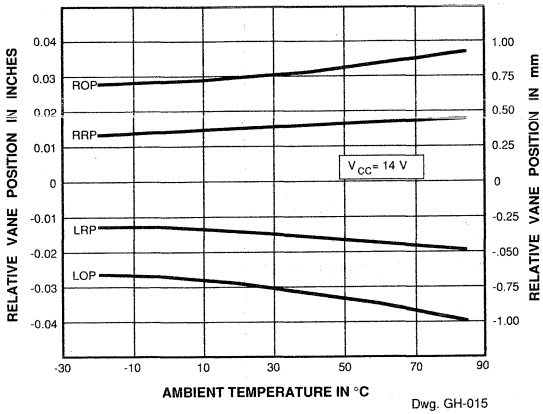
NOTES:
1. Measured relative to either vertical leading edge of the vane (depending on direction of motion) and the device center line.
2. Measured relative to either vertical trailing edge of the vane (depending on direction of motion) and the device center line.
3. The difference between the distances from the center line at which switch points occur as the vane travels through the slot from either direction.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted).

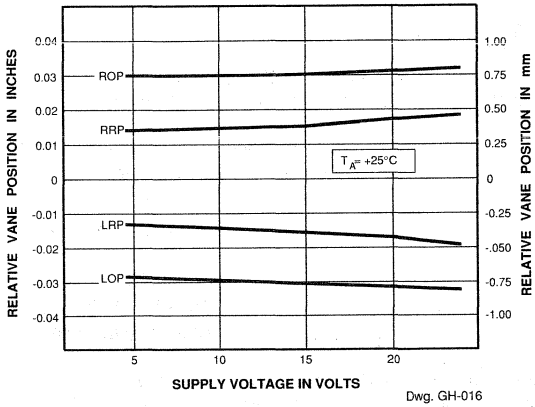
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{CC} = 24 V, I_{OUT} = 20 mA	—	150	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V	—	0.05	10	µA
Supply Current	I_{CC}	V_{CC} = 4.5 V, Output Open	—	4.7	8.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.04	2.0	µs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.18	2.0	µs

6450
DIGITAL VANE SWITCH

TYPICAL CHARACTERISTICS



Dwg. GH-015



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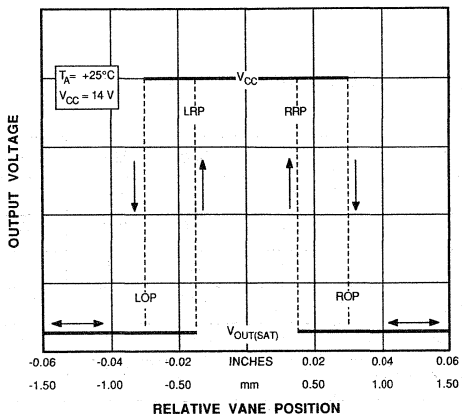
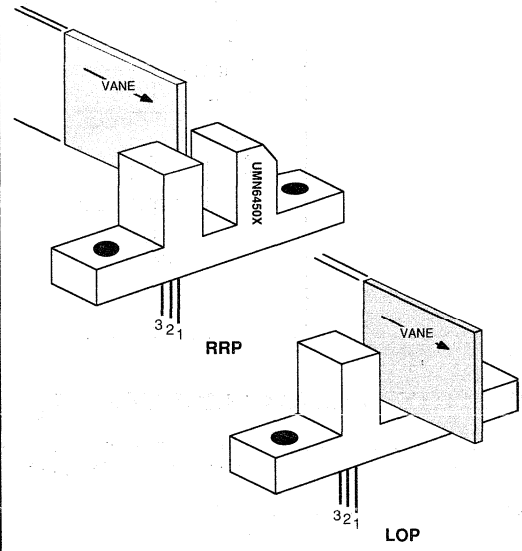
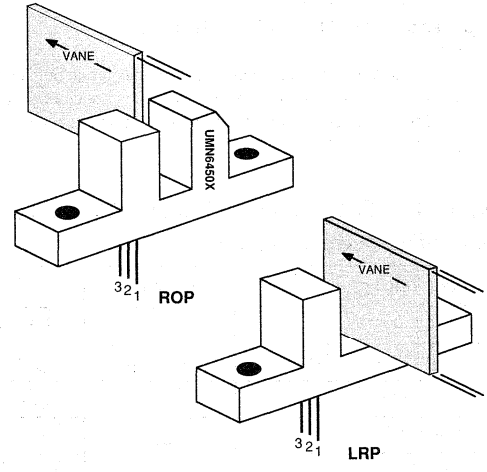


Dwg. GH-017

SWITCH POINT DEFINITIONS



Dwg. AH-002-1



Dwg. AH-002-2

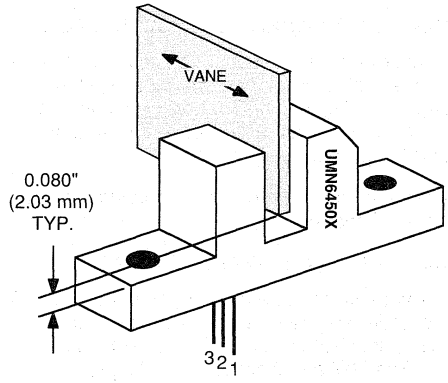
APPLICATIONS INFORMATION

VANE THICKNESS

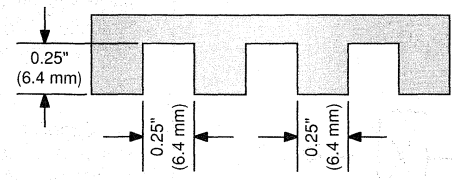
Increasing the thickness of the vane above 0.035" (0.89 mm) will move both switch points away from the center of the device. The increase in RRP and LRP will be larger than the increase in ROP and LOP which, in effect, reduces hysteresis. A vane thinner than 0.025" (0.64 mm) may be distorted by the force of the magnetic field and is therefore not recommended.

VANE DEPTH

The vane should be kept less than 0.120" (3.048 mm) from the bottom of the slot. The effect of depth on the switch points is minimal in this region. If the vane is more than 0.120" above the bottom of the slot, the switch points will move closer to the device center. If the distance is increased too much, the output will eventually fail to switch high.



Dwg. AH-002



Dwg. MH-006

VANE AND GAP WIDTH

The vane must be of sufficient width to shunt the magnetic field away from the sensor. The gap between successive vanes must allow the magnetic field to increase to the point where it will operate the Hall sensor. A minimum vane width of 0.25" (6.4 mm) and a minimum gap between vanes of 0.25" (6.4 mm) is recommended.

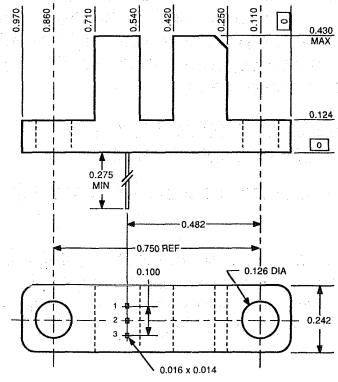
VANE LATERAL POSITION

Shifting the vane plane of travel laterally toward the magnet tower will move the switch points closer to the device center and will also increase hysteresis. Conversely, shifting the vane plane of travel laterally toward the sensor tower will move the switch points away from the device center and will also decrease hysteresis.

VANE MATERIAL

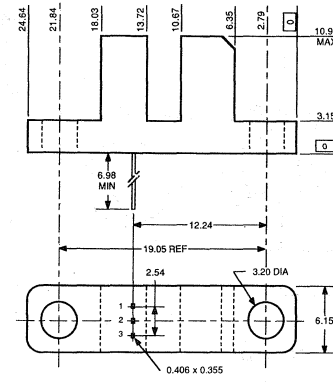
The vane material must have sufficient permeability to shunt the magnetic field away from the sensor. Low-carbon steel (1030 or lower), or other ferrous materials, are recommended.

DIMENSIONS IN INCHES



Dwg. MH-005 IN

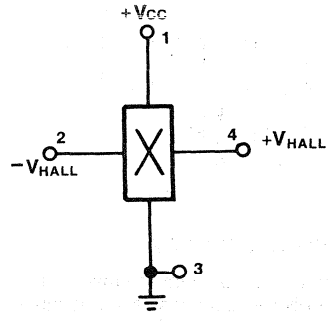
DIMENSIONS IN MILLIMETERS
(Based on 1" = 25.4 mm)



Dwg. MH-005 MM

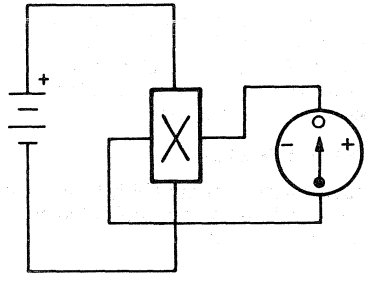
APPLICATIONS INFORMATION

HALL EFFECT IC APPLICATIONS GUIDE



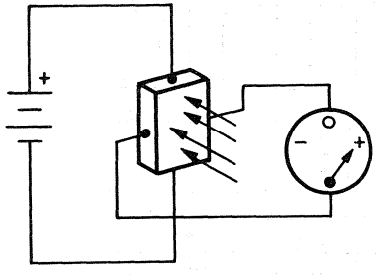
Dwg. No. 13,100

FIGURE 1



Dwg. No. 13,101

FIGURE 2



Dwg. No. 13,102

FIGURE 3

Allegro Microsystems uses the latest bipolar integrated circuit technology in combination with the century-old Hall effect to produce Hall effect ICs. These are contactless, magnetically activated switches and sensors with the potential to simplify and improve systems.

LOW-COST SIMPLIFIED SWITCHING

Simplified switching is a Hall sensor's strong point. Hall effect IC switches combine Hall voltage generators, signal amplifiers, Schmitt trigger circuits, and transistor output circuits on single integrated circuit chips. Output is clean, fast, and switched without bounce—an inherent problem with mechanical contact switches. A Hall effect switch typically operates at up to a 100 kHz repetition rate, and costs less than many common electromechanical switches.

EFFICIENT, EFFECTIVE, LOW-COST LINEAR SENSORS

The linear Hall effect sensor detects the motion, position, or change in field strength of an electromagnet, a permanent magnet, or a ferromagnetic material with an applied magnetic bias. Energy consumption is very low. The output is linear and temperature-stable. The sensor's frequency response is flat up to approximately 25 kHz.

A Hall effect sensor is more efficient and effective than inductive or optoelectronic sensors, and at a lower cost.

SENSITIVE CIRCUITS FOR RUGGED SERVICE

The Hall effect sensor is virtually immune to environmental contaminants and is suitable for use under severe service conditions. The circuit is very sensitive and provides reliable, repetitive operation in close tolerance applications. The Hall effect sensor can see precisely through dirt and darkness.

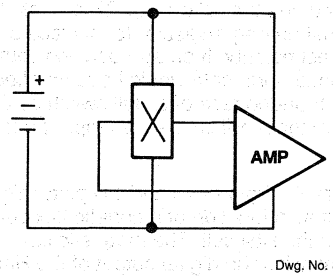
CURRENT APPLICATIONS

Current applications for Hall effect ICs include use in ignition systems, speed controls, security systems, alignment controls, micrometers, mechanical limit switches, computers, printers, disk drives, keyboards, machine tools, key-switches, and pushbutton switches. They are also used as tachometer pickups, current limit switches, position detectors, selector switches, current sensors, linear potentiometers and brushless dc motor commutators.

THE HALL EFFECT SENSOR: HOW DOES IT WORK?

The basic Hall sensor is a small sheet of semiconductor material represented by Figure 1.

A constant voltage source, as shown in Figure 2, will force a constant bias current to flow in the semiconductor sheet. The output will take the form of a voltage measured across the width of the sheet that will have negligible value in the absence of a magnetic field.



Dwg. No. 13,103

FIGURE 4

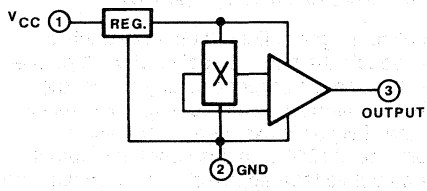


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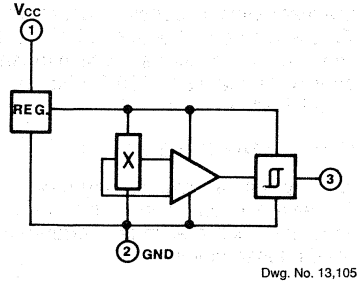
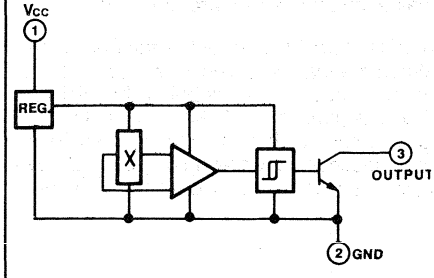
FIGURE 5



Dwg. No. 13,105

FIGURE 6



Dwg. No. 13,106

FIGURE 7

If the biased Hall sensor is placed in a magnetic field with flux lines at right angles to the Hall current (Figure 3), the voltage output is directly proportional to the strength of the magnetic field. This is the Hall effect, discovered by E. F. Hall in 1879.

LINEAR OUTPUT HALL EFFECT DEVICES.

The output voltage of the basic Hall effect sensor (Hall element) is quite small. This can present problems, especially in an electrically noisy environment. Addition of a stable high-quality dc amplifier and voltage regulator to the circuit (Figures 4 and 5) improves the transducer's output and allows it to operate over a wide range of supply voltages. The modified device provides an easy-to-use analog output that is linear and proportional to the applied magnetic flux density.

The UGN3501 is this type of linear output device. The UGN3503 and UGS3503 have improved sensitivity and temperature-stable characteristics. The output of the UGN/UGS3503 is ratiometric; that is, its output is proportional to its supply voltage.

DIGITAL OUTPUT HALL EFFECT SWITCHES

The addition of a Schmitt trigger threshold detector with built-in hysteresis, as shown in Figure 6, gives the Hall effect circuit digital output capabilities. When the applied magnetic flux density exceeds a certain limit, the trigger provides a clean transition from OFF to ON without contact bounce. Built-in hysteresis eliminates oscillation (spurious switching of the output) by introducing a magnetic dead zone in which switch action is disabled after the threshold value is passed.

An open-collector NPN output transistor added to the circuit (Figure 7) gives the switch digital logic compatibility. The transistor is a saturated switch that shorts the output terminal to ground wherever the applied flux density is higher than the ON trip point of the device. The switch is compatible with all digital families. The output transistor can sink enough current to directly drive many loads, including relays, triacs, SCRs, LEDs, and lamps.

The circuit elements in Figure 7, fabricated on a monolithic silicon chip and encapsulated in a small epoxy or ceramic package, are common to all Hall effect digital switches. Differences between device types are generally found in specifications such as magnetic parameters, operating temperature ranges, and temperature coefficients.

OPERATION

All Hall effect devices are activated by a magnetic field. A mount for the the devices, and electrical connections, must be provided; Parameters such as load current, environmental conditions, and supply voltage must fall within the specific limits shown in the appropriate documentation.

Magnetic fields have two important characteristics—flux density and polarity (or orientation). In the absence of any magnetic field, most Hall effect digital switches are designed to be OFF (open circuit at output). They will turn ON only if subjected to a magnetic field that has both sufficient density and the correct orientation.

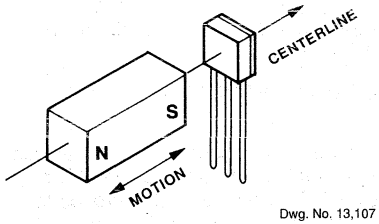


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FIGURE 8

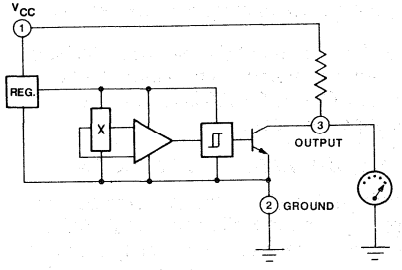

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FIGURE 9

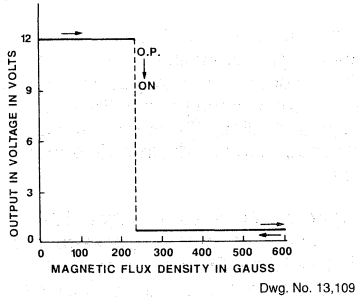

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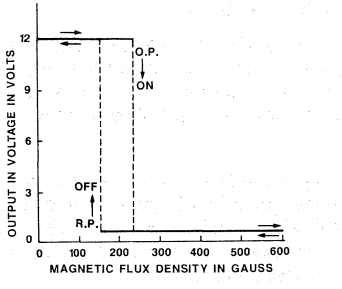
FIGURE 10



Dwg. No. 13,110

FIGURE 11

Hall switches have an active area that is closer to one face of the package (the face with the lettering, the branded face). To operate the switch, the magnetic flux lines must be perpendicular to this face of the package, and must have the correct polarity. If an approaching south pole would cause switching action, a north pole would have no effect. In practice, a close approach to the branded face of a Hall switch by the south pole of a small permanent magnet will cause the output transistor to turn ON (Figure 8).

A Transfer Characteristics Graph (Figures 10 and 11) plots this information. It is a graph of output as a function of magnetic flux density (measured in gauss) presented to the Hall cell. The magnetic flux density is shown on the horizontal axis. The digital output of the Hall switch is shown along the vertical axis.

To acquire data for this graph, add a power supply and a pull-up resistor that will limit current through the output transistor and enable the value of the output voltage to approach zero (Figure 9).

In the absence of an applied magnetic field (0 G), the switch is OFF, and the output voltage equals the power supply (12 V). A permanent magnet's south pole is then moved perpendicularly toward the active area of the device. As the magnet's south pole approaches the branded face of the switch, the Hall cell is exposed to increasing magnetic flux density. At some point (240 G in this case), the output transistor turns ON and the output voltage approaches zero (Figure 10). That value of flux density is called the operate point. If we continue to increase the field's strength, say to 600 G, nothing more happens. The switch turns ON once and stays ON.

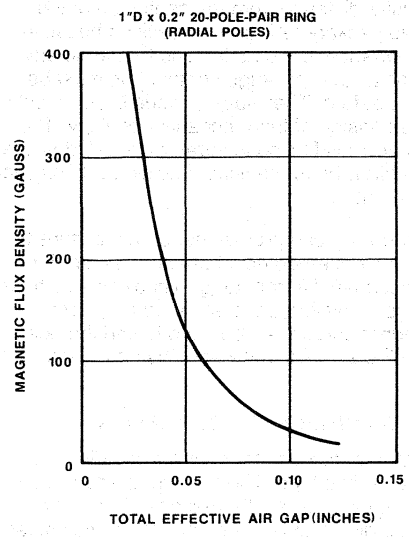
To turn the switch OFF, the magnetic flux density must fall to a value far lower than the 240 G "operate point" because of the built-in hysteresis. For this example we use 90 G hysteresis, which means the device turns OFF when flux density decreases to 150 G (Figure 11). That value of flux density is called the "release point".

CHARACTERISTICS AND TOLERANCES

The exact magnetic flux density values required to turn Hall switches ON and OFF differ for several reasons, including design criteria and manufacturing tolerances. Extremes in temperature will also somewhat affect the operate and release points.

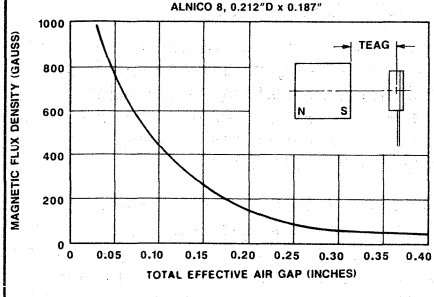
For each device type, worst-case magnetic characteristics for the operate value, the release value, and hysteresis are provided.

All switches are guaranteed to turn ON at or below the maximum operate point flux density. When the magnetic field is reduced, all devices will turn OFF before the flux density drops below the minimum release point value. Each device is guaranteed to have at least the minimum amount of hysteresis to ensure clean switching action. This hysteresis ensures that, even if mechanical vibration or electrical noise is present, the switch output is fast, clean, and occurs only once per threshold crossing.



Dwg. No. 13,126

FIGURE 12A



Dwg. No. 13,112

FIGURE 12B

GETTING STARTED

Since the electrical interface is usually straightforward, the design of a Hall effect system should begin with the physical aspects. In position-sensing or motion-sensing applications, the following questions should be answered:

How much and what type of motion is there?

What angular or positional accuracy is required?

How much space is available for mounting the sensing device and activating magnet?

How much play is there in the moving assembly?

How much mechanical wear can be expected over the lifetime of the machine?

Will the product be a mass-produced assembly, or a limited number of machines that can be individually adjusted and calibrated?

What temperature extremes are expected?

A careful analysis will pay big dividends in the long term.

THE ANALYSIS

The field strength of the magnet should be investigated. The strength of the field will be the greatest at the pole face, and will decrease with increasing distance from the magnet. The strength of the magnetic field can be measured with a gaussmeter or a calibrated linear Hall sensor, such as a UGN3503U (see Appendix II).

A plot of field strength (magnetic flux density) is a function of distance along the intended line of travel of the magnet. Hall device specifications (sensitivity in mV/G for a linear device, or operate and release points in gauss for a digital device) can be used to determine the critical distances for a particular magnet and type of motion. Note that these field strength plots are not linear, and that the shape of the flux density curve depends greatly upon magnet shape, the magnetic circuit, and the path traveled by the magnet.

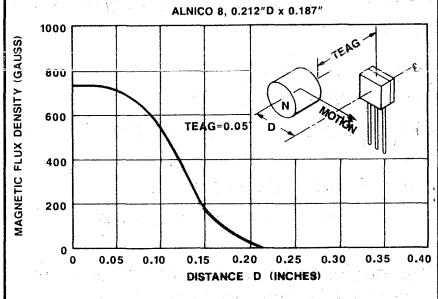
TOTAL EFFECTIVE AIR GAP (TEAG)

Total effective air gap, or TEAG, is the sum of active area depth and the distance between the package's surface and the magnet's surface. A graph of flux density as a function of total effective air gap (Figure 12A) illustrates the considerable increase in flux density at the sensor provided by a thinner package. The actual gain depends on the characteristic slope of flux density for a particular magnet.

MODES OF OPERATION

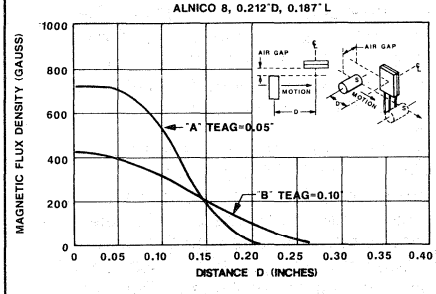
Even with a simple bar or rod magnet, there are several possible paths for motion. The magnetic pole could move perpendicularly straight at the active face of the Hall device. This is called the head-on mode of operation. The curve of Figure 12B illustrates typical flux density (in gauss) as a function of TEAG for a cylindrical magnet.

The head-on mode is simple, works well, and is relatively insensitive to lateral motion. The designer should be aware that overextension of the mechanism could cause physical damage to the epoxy package of the Hall device.



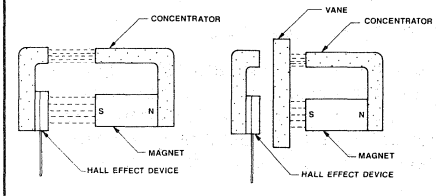
Dwg. No. 13,113

FIGURE 13



Dwg. No. 13,114

FIGURE 14



Dwg. No. 13,115

FIGURE 15

A second possibility would be to move the magnet in from the side of the Hall device in the slide-by mode of operation, as illustrated in Figure 13. Note that now the distance plotted is not total effective air gap, but rather the perpendicular distance from the centerline of the magnet to the centerline of the package. Air gap is specified because of its obvious mechanical importance, but bear in mind that to do any calculations involving flux density, the "package contribution must be added and the TEAG used, as before. The slide-by mode is commonly used to avoid contact if overextension of the mechanism is likely. The use of strong magnets and/or ferrous flux concentrators in well-designed slide-by magnetic circuits will allow better sensing precision with smaller magnet travel than the head-on mode.

Magnet manufacturers generally can provide head-on flux density curves for their magnets, but they often do not characterize them for slide-by operation, possibly because different air gap choices lead to an infinite number of these curves; however, once an air gap is chosen, the readily available head-on magnet curves can be used to find the peak flux density (a single point) in the slide-by application by noting the value at the total effective air gap.

STEEP SLOPES—HIGH FLUX DENSITIES

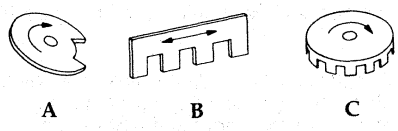
For linear Hall devices, greater flux changes for a given displacement give greater outputs, clearly an advantage. The same property is desirable for digital Hall devices, but for more subtle reasons. To achieve consistent switching action in a given application, the Hall device must switch ON and OFF at the same positions relative to the magnet.

To illustrate this concept, consider the flux density curves from two different magnet configurations in Figure 14. With an operate point flux density of 200 G, a digital Hall effect device would turn ON at a distance of approximately 0.14 inches in either case. If manufacturing tolerances or temperature effects shifted the operate point to 300 G, notice that for curve A (steep slope) there is very little change in the distance at which switching occurs. In the case of curve B, the change is considerable. The release point (not shown) would be affected in much the same way. The basic principles illustrated in this example can be modified to include mechanism and device specification tolerances and can be used for worse-case design analysis. Examples of this procedure are shown in later sections.

VANE INTERRUPTER SWITCHING

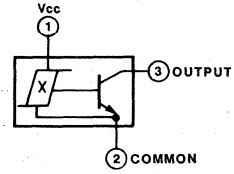
In this mode, the activating magnet and the Hall device are mounted on a single rigid assembly with a small air gap between them. In this position, the Hall device is held in the ON state by the activating magnet. If a ferromagnetic plate, or vane is placed between the magnet and the Hall device, as shown in Figure 15, the vane forms a magnetic shunt that distorts the flux field away from the Hall device.

Use of a movable vane is a practical way to switch a Hall device. The Hall device and magnet can be molded together as a unit, thereby eliminating alignment problems, to produce an extremely rugged switching assembly. The ferrous vane or vanes that interrupt the flux could have linear motion, or rotational motion, as in an automotive distributor. Ferrous vane assemblies, due to the steep flux density/distance curves that can be achieved, are often used where precision switching over a large temperature range is required.



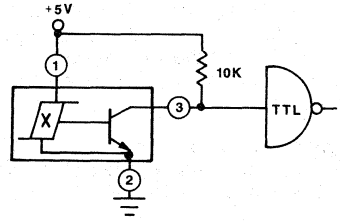
Dwg. No. 13,116

FIGURE 16



Dwg. No. 13,117

FIGURE 17



Dwg. No. 13,118

FIGURE 18A

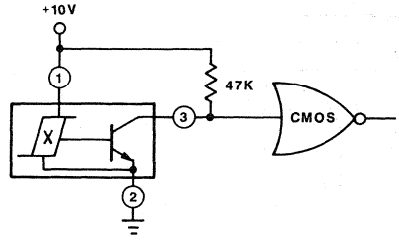


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FIGURE 18B

The ferrous vane can be made in many configurations, as shown in Figure 16. With a linear vane similar to that of Figure 16B, it is possible to repeatedly sense position within 0.002" over a 125°C temperature range.

ELECTRICAL INTERFACE FOR DIGITAL HALL DEVICES

The output stage of a digital Hall switch is simply an open-collector NPN transistor. The rules for use are the same as those for any similar switching transistor.

When the transistor is OFF, there is a small output leakage current (typically a few nanoamps) that usually can be ignored, and a maximum (breakdown) output voltage (usually 24 V), which must not be exceeded.

When the transistor is ON, the output is shorted to the circuit common. The current flowing through the switch must be externally limited to less than a maximum value (usually 20 mA) to prevent damage. The voltage drop across the switch ($V_{CE(sat)}$) will increase for higher values of output current. You must make certain this voltage is compatible with the OFF, or "logic zero," voltage of the circuit you wish to control.

Hall devices switch very rapidly, with typical rise and fall times in the 400 ns range. This is rarely significant, since switching times are almost universally controlled by much slower mechanical parts.

COMMON INTERFACE CIRCUITS

Figure 17 illustrates a simplified schematic symbol for Hall digital switches (Types 3113, 3119, 3120, 3130, 3140). It will make further explanation easier to follow.

Interface for digital logic integrated circuits usually requires only an appropriate power supply and pull-up resistor.

With current-sinking logic families, such as DTL or the popular 7400 TTL series (Figure 18A), the Hall switch has only to sink one unit-load of current to the circuit common when it turns ON (1.6 mA maximum for TTL). In the case of CMOS gates (Figure 18B), with the exception of switching transients, the only current that flows is through the pull-up resistor (about 0.2 mA in this case).

Loads that require sinking currents up to 20 mA can be driven directly by the Hall switch.

A good example is a light emitting diode (LED) indicator that requires only a resistor to limit current to an appropriate value. If the LED drops 1.4 V at a current of 20 mA, the resistor required for use with a 12 V power supply can be calculated as:

$$\frac{12\text{ V} - 1.4\text{ V}}{0.02\text{ A}} = 530\ \Omega$$

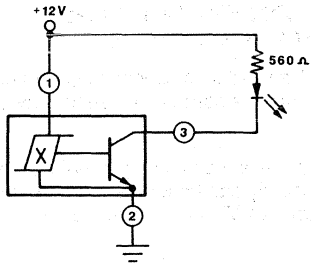

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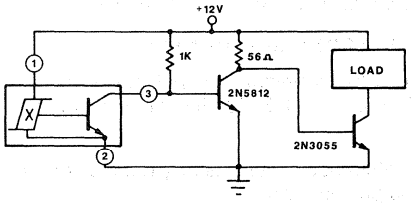
FIGURE 19



Dwg. No. 13,121

FIGURE 20

The nearest standard value is 560 Ω, resulting in the circuit of Figure 19.

Sinking more current than 20 mA requires a current amplifier. For example, if a certain load to be switched requires 4 A and must turn ON when the activating magnet approaches, the circuit shown in Figure 20 could be used.

When the Hall switch is OFF (insufficient magnetic flux to operate), about 12 mA of base current flows through the 1 kΩ resistor to the 2N5812 transistor, thereby saturating it and shorting the base of the 2N3055 to ground, which keeps the load OFF. When a magnet is brought near the Hall switch, it turns ON, shorting the base of the 2N5812 to ground and turning it OFF. This allows:

$$\frac{12\ V}{56\ \Omega} = 210\ mA$$

of base current to flow to the 2N3055, which is enough to saturate it for any load current of 4 A or less.

The Hall switch cannot source current to a load in its OFF state, but it is no problem to add a transistor that can. For example, consider using a 40669 triac to turn ON a 115 V or 230 V ac load. This triac would require about 80 mA of gate current to trigger it to the ON condition. This could be done with a 2N5811 PNP transistor, as shown below in Figure 21.

When the Hall switch is turned ON, 9 mA of base current flows into the 2N5811, thereby saturating it and allowing it to supply 80 mA of current to trigger the triac. When the Hall switch is OFF, no base current flows in the 2N5811, which turns it OFF and allows no gate current to pass to the triac. The 4.7 kΩ and the 1 kΩ resistors were added as a safeguard against accidental turn-on by leakage currents, particularly at elevated temperatures.

Note that the +12 V supply common is connected to the low side of the ac line, and in the event of a mixup, the Hall switch and associated low-voltage circuitry would be 115 V above ground. *Be careful!*

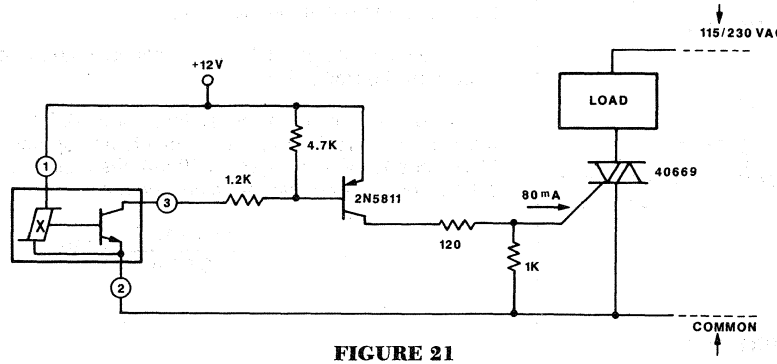


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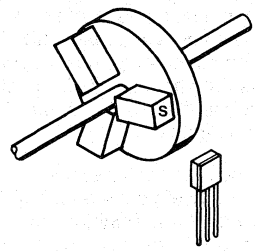
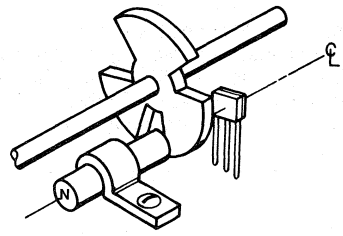
FIGURE 21

A. MAGNETIC ROTOR



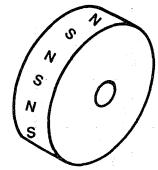
B. FERROUS VANE ROTOR



Dwg. No. 13,123

FIGURE 22

A. RADIAL



B. AXIAL

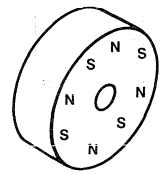


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FIGURE 23

ROTARY ACTIVATORS FOR HALL SWITCHES

A frequent application involves the use of Hall switches to generate a digital output proportional to velocity, displacement, or position of a rotating shaft. The activating magnetic field for rotary applications can be supplied in either of two ways:

MAGNETIC ROTOR ASSEMBLY

The activating magnet(s) are fixed on the shaft and the stationary Hall switch is activated with each pass of a magnetic south pole (Figure 22A). If several activations per revolution are required, rotors can sometimes be made inexpensively by molding or cutting plastic or rubber magnetic material. Ring magnets can also be used. Ring magnets are commercially available disc-shaped magnets with poles spaced around the circumference. They will operate Hall switches dependably and at reasonable costs.

Ring magnets do have limitations:

The accuracy of pole placement (usually within 2 or 3 degrees).

Uniformity of pole strength (±5%, or worse).

These limitations must be considered in applications requiring precision switching.

FERROUS VANE ROTOR ASSEMBLY

Both the Hall switch and the magnet are stationary (Figure 22B); the rotor interrupts and shunts the flux with the passing of each ferrous vane.

Vane switches tend to be a little more expensive than ring magnets, but because the dimensions and configuration of the ferrous vanes can be carefully controlled, they are often used in applications requiring precise switching or duty cycle control.

Properly designed vane switches can have very steep flux density curves, yielding precise and stable switching action over a wide temperature range.

RING MAGNETS FOR HALL SWITCH APPLICATIONS

Ring magnets suitable for use with Hall switches are readily available from magnet vendors in a variety of different materials and configurations. The poles may be oriented either radially (Figure 23A) or axially (Figure 23B) with up to 20 pole-pairs on a one-inch diameter ring. For a given size and pole count, ring magnets with axial poles have somewhat higher flux densities.

Materials most commonly used are various Alnicos, Ceramic 1, and barium ferrite in a rubber or plastic matrix material. Manufacturers usually have stock sizes with a choice of the number of pole pairs. Custom configurations are also available at a higher cost.

Alnico is a name given to a number of aluminum nickel-cobalt alloys that have a fairly wide range of magnetic properties. In general, Alnico ring magnets have the highest flux densities, the smallest changes in field strength with changes in temperature, and the highest cost. They are generally too hard to shape except by grinding and are fairly brittle, which complicates the mounting of bearings or arbor.

Ceramic 1 ring magnets (trade names Indox, Lodex) have somewhat lower flux densities (field strength) than the Alnicos, and their field strength changes more with temperature; however, they are considerably lower in cost and are highly resistant to demagnetization by external magnetic fields. The ceramic material is resistant to most chemicals and has high electrical resistivity. Like Alnico, they can withstand temperatures well above that of Hall switches and other semiconductors, and must be ground if reshaping or trimming is necessary. They may require a support arbor to reduce mechanical stress.

The rubber and plastic barium ferrite ring magnets are roughly comparable to Ceramic 1 in cost, flux density, and temperature coefficient, but are soft enough to shape using conventional methods. It is also possible to mold or press them onto a shaft for some applications. They do have temperature limitations ranging from 70°C to 150°C, depending on the particular material, and their field strength changes more with temperature than Alnico or Ceramic 1.

Regardless of material, ring magnets have limitations on the accuracy of pole placement and uniformity of pole strength which, in turn, limit the precision of the output waveform. Evaluations have shown that pole placement in rubber, plastic, and ceramic magnets usually falls within 2° or 3° of target, but 5° errors have been measured. Variations of flux density from pole to pole will commonly be ±5%, although variations of up to ±30% have been observed.

Figure 24 is a graph of magnetic flux density as a function of angular position for a typical 4 pole-pair ceramic ring magnet, one inch in diameter, with a total effective air gap of 0.065" (0.050" clearance plus 0.015" package contribution). It shows quite clearly both the errors in pole placement and variations of strength from pole to pole.

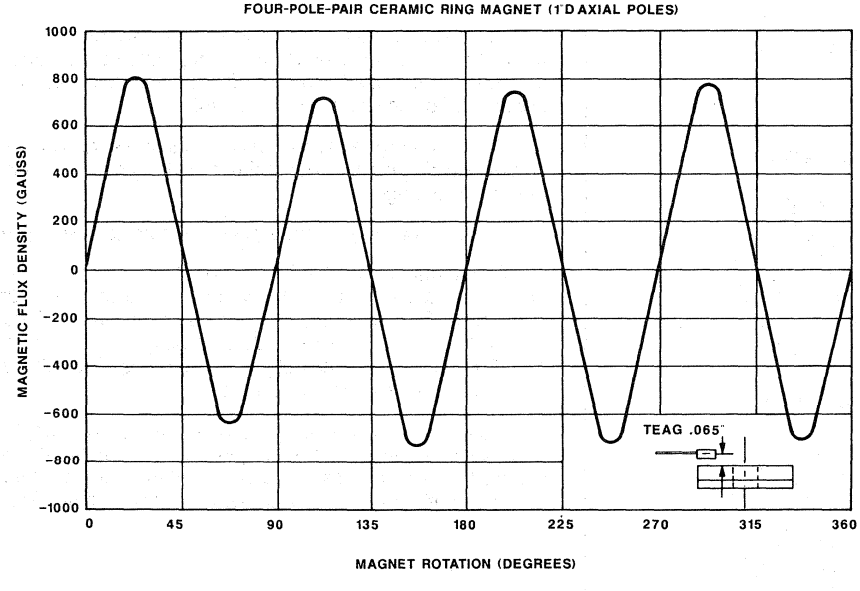

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FIGURE 24

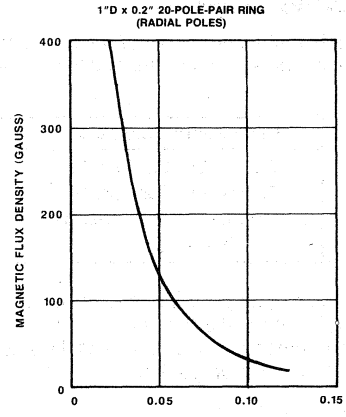

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FIGURE 25

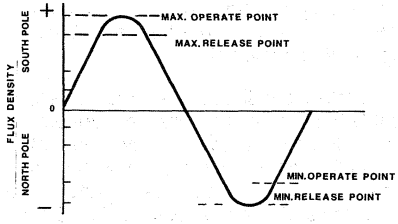

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FIGURE 26A

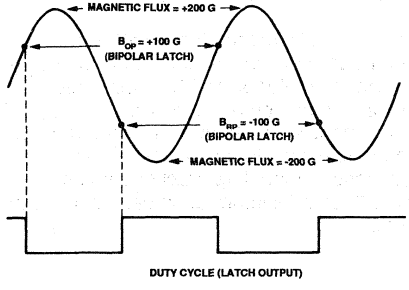

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FIGURE 26B

A frequent concern with ring magnets is ensuring sufficient flux density for reliable switching. There is a trade-off between the number of pole-pairs and the flux density for rings of a given size. Thus, rings with large numbers of poles have lower flux densities. It is important that the total effective air gap (TEAG) is kept to a minimum, since flux density at the Hall active area decreases by 5 G or 6 G per 0.001" for many common ring magnets. This is clearly shown in Figure 25, a graph of flux density at a pole as a function of TEAG for a typical 20-pole-pair plastic ring magnet. Also shown in Figure 25 is the effect of "package contribution" to the TEAG. The standard "U" package contributes about 0.016". The other factor contributing to TEAG is mechanical clearance, which should be as small as possible, consistent with dimensional tolerances of the magnet, bearing tolerances, bearing wear, and temperature effects on the Hall switch mounting bracket.

WHAT IS A BIPOLAR SWITCH?

A bipolar switch, the UGN/UGS3130, has a maximum operate point of +150 G, a minimum release point of -150 G, and a minimum hysteresis of 20 G at + 25°C; however, the operate point could be as low as -130 G (-150 G minimum release, 20 G minimum hysteresis) and the release could be as high as +130 G (+150 G maximum operate, 20 G minimum hysteresis). Figure 26A shows two cases of operate and release with one device operating at the maximum operate and release points, and the other with minimum operate and release points.

In applications previously discussed, the Hall switch was operated (turned ON) by the approach of a magnetic south pole (positive flux). When the south pole was removed (flux approaches zero), the Hall switch had to release (turn OFF). On ring magnets, both south and north poles are present in an alternating pattern. The release point flux density becomes less important, for if the Hall switch has not turned OFF when the flux density goes to zero (south pole has passed), it will certainly turn OFF when the following north pole causes flux density to go negative. Bipolar Hall switches take advantage of this extra margin in release point flux values to achieve lower operate point flux densities, a definite advantage in ring magnet applications.

THE BIPOLAR LATCH

Unlike the Type 3130 bipolar switch, which may operate and release with a south pole or north pole, the bipolar latch offers a more precise control of the operate and release parameters. This Hall integrated circuit has been designed to operate (turn ON) with a south pole only; it will then remain ON when the south pole has been removed. In order to have the bipolar latch release (turn OFF), it must be presented with a north magnetic pole. This alternating south pole-north pole operation, when properly designed, will produce a duty cycle approaching 50%.

The UGN3175 was designed specifically for applications requiring a tightly controlled duty cycle, such as in brushless dc motor commutation. This was accomplished with the introduction of the bipolar latch in 1982. The 3175 has become very popular as a brushless dc motor commutator, shaft encoder, speedometer element, and tachometer sensor.

Duty cycle is controlled with an alternating magnetic field, as shown in Figure 26B.

DESIGN EXAMPLE

Given:

Operating temperature range of -20° to +85°C.

Bipolar Hall switch UGN3130U in standard "U" package:

Maximum operate point +200 G from -20° to + 85°C.

Minimum release point -200 G from -20°C to + 85°C.

Air gap package contribution 0.016".

Necessary mechanical clearance 0.030".

First, find the total effective air gap:

TEAG = clearance + package contribution

TEAG = 0.030" + 0.016" = 0.046"

Now, determine the necessary flux density sufficient to operate the Hall switch, plus 40%.

To operate the Hall switch, the magnet must supply a minimum of ±200 G at a distance of 0.046" over the entire temperature range. Good design practice requires the addition of extra flux to provide some margin for aging, mechanical wear, and other imponderables. If we add a pad of 100 G, a reasonable number, the magnet required must supply ±300 G at a distance of 0.046" over the temperature range.

TEMPERATURE EFFECTS

Unfortunately, magnet strength is affected by temperature to some degree. Temperature coefficients of some common magnetic materials are given below:

Material	Temperature Coefficient
Rubber/Plastic	-0.2% to -0.3% per °C
Ceramic 1	-0.15% to -0.2% per °C
Alnico 2, 5	-0.02% to -0.03% per °C
Alnico 8	±0.01% per °C

If we are considering a ceramic ring magnet with a worst-case temperature coefficient of -0.2%/°C, we must add some extra flux density to the requirement at room temperature to ensure that we still have +300 G per south pole at +85°C. This amount is:

[(85°C - 25°C) x 0.2%/°C] 300 G = +36 G

Thus, the flux density that will ensure that the Hall switch will operate over temperature is 300 G + 36 G = 336 G per south pole at +25°C.

Follow the same procedure for the north pole requirements. If the magnet will supply +300 G per south pole and -300 G per north pole at +85°C, it will supply even more flux density per north pole at -20°C because of the negative temperature coefficient.

In applications where temperature conditions are more severe, Alnico magnets are considerably better than the ceramic magnets we considered. It is also possible to order custom Hall switches with specifications tailored to your application. For example, you can specify a range of operate and release points at a particular temperature, with temperature coefficients for operate and release points, if that is better suited to your application. On a custom basis, Hall switches are available with operate and release point temperature coefficients of less than 0.3 G/°C, and with operate flux densities of less than 100 G.

If you intend to use a low-cost, low flux density ring magnet, then the UGN3130U device in the 0.060" package would be a good choice. The package contribution is 0.016", which results in a significant improvement in peak flux density from a magnet, as shown in Figure 25.

If the rotor drive can withstand an increased torque requirement, consider a ferrous flux concentrator. Flux density can be increased by 10% to 40% in this manner. A concentrator of 0.03125" mild steel having the same dimensions as, and cemented to, the back surface of the Hall switch, will increase flux density by about 10%. A return path of mild steel from the back side of the device to the adjacent poles can add even more. Often the functions of mounting bracket and flux concentrator can be combined. Additional information can be found in the section on flux concentrators.

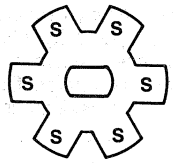

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FIGURE 27

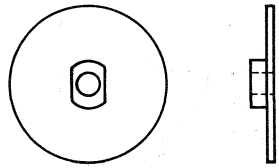

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FIGURE 28

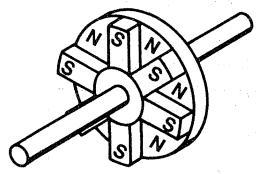

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FIGURE 29

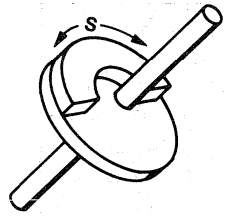

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FIGURE 30

RING MAGNETS —DETAILED DISCUSSION

AN INEXPENSIVE ALTERNATIVE

Innovative design can produce surprisingly good results. Rubber and plastic magnet stock comes in sheets. One side of the sheet is magnetic north; the other side is south. This material is relatively inexpensive and can easily be stamped or die-cut into various shapes.

These properties prompted one designer to fabricate an inexpensive magnetic rotor assembly that worked very well. The rubber magnet stock was die-cut into a star-shaped rotor form, as shown in Figure 27. A nylon bushing formed a bearing, as shown in Figure 28.

Finally, a thin mild steel backing plate was mounted to the back of the assembly to give mechanical strength and to help conduct the flux back from the north poles on the opposite side. This actually served to form apparent north poles between the teeth; the measured flux between south pole teeth is negative. Figure 29 shows the completed magnetic rotor assembly, essentially a ring magnet with axial poles.

The Hall switch was mounted with its active surface close to the top of the rotor assembly, facing the marked poles. There is some versatility in this approach, as asymmetrical poles can be used to fabricate a rotor that wll allow trimmable ON time and, thus, work as a timing cam. Figure 30 illustrates a cam timer adjusted to 180° ON and 180° OFF.

RING MAGNET SELECTION

When you discuss your application with a magnet vendor, the following items should be considered:

Mechanical Factors

- Dimensions and tolerances
- Mounting hole type and maximum eccentricity
- Rotational speed
- Mechanical support required
- Coefficient of expansion

Magnetic Factors

- Poles: number, orientation, and placement accuracy
- Flux density at a given TEAG (remember to add the Hall switch package contribution to the clearance figure)
- Magnetic temperature coefficient

Environmental Factors

- Tolerance of the material to the working environment (temperature, chemical solvents, electric potentials)

Flux density curves from several typical ring magnets are included to present an idea of what can be expected from various sizes and materials. Figure 31 shows the curve for a ring similar in size and material to that of Figure 25, but with 10 pole-pairs instead of 20 (note increased flux density values). Figure 32 shows the curve from a one pole-pair Alnico 8 ring. Figure 33 shows the curve from a three-pole-pair Ceramic 1 ring. Figure 34 shows the curves from a four-pole-pair Ceramic 1 ring, with and without a ferrous flux concentrator.

Incoming inspection of ring magnets is always advisable. You can ensure the magnets are within the agreed upon magnetic specifications by making measurements with a commercial gaussmeter, or a calibrated linear Hall device mounted in a convenient test fixture. Calibrated UGN3503U Hall devices and technical assistance are available.

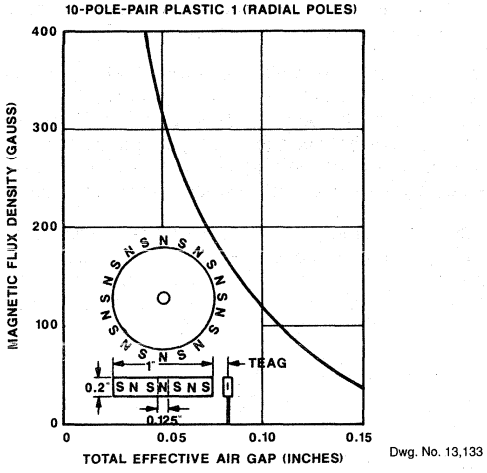

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FIGURE 31

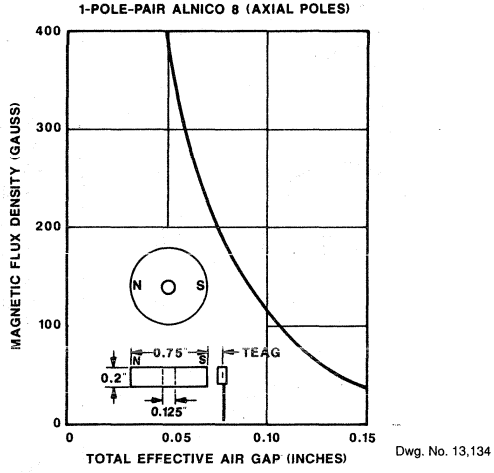

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FIGURE 32

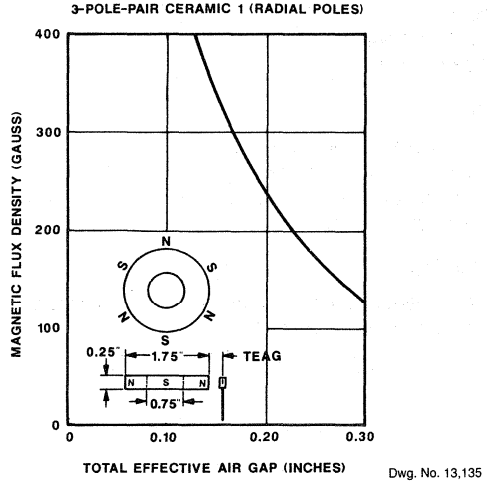

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FIGURE 33

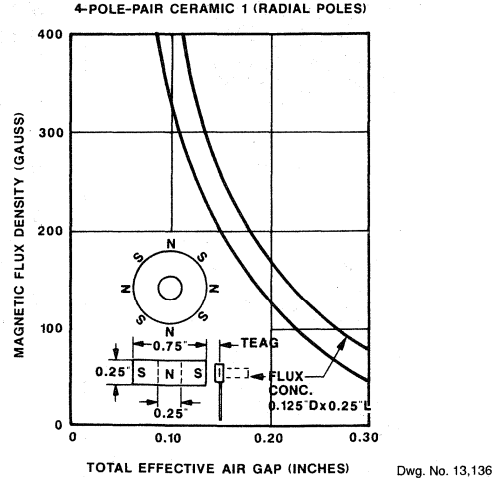

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FIGURE 34

FERROUS VANE ROTARY ACTIVATORS

A ferrous vane rotor assembly is the alternative to magnetic rotors for rotary Hall switch applications. As shown previously, a single magnet will hold a Hall switch ON except when one of the rotor vanes interrupts the flux path and shunts the flux path away from the Hall switch. The use of a single stationary magnet allows very precise switching by eliminating ring magnet variations, placement, and strength. Unlike the evenly spaced poles on ring magnets, the width of rotor vanes can easily be varied. It is possible to vary the Hall switch OFF and ON times, which gives the designer control over the duty cycle of the output waveform. Ferrous vane rotors are a good choice where precise switching is desired over a wide range of temperatures. As the vane passes between magnet and Hall switch, progressively more flux will be blocked or shunted. Small variations in lateral position have a very small effect on the transition point.

A FERROUS VANE IN OPERATION

Figure 35 combines top and front views of a ferrous vane magnet/Hall switch system with the graph of flux density as a function of vane travel produced by this system. Note that the drawings and the graph are vertically aligned along the horizontal axis. Position is measured from the leading edge of the vane to the centerline of the magnet/Hall device.

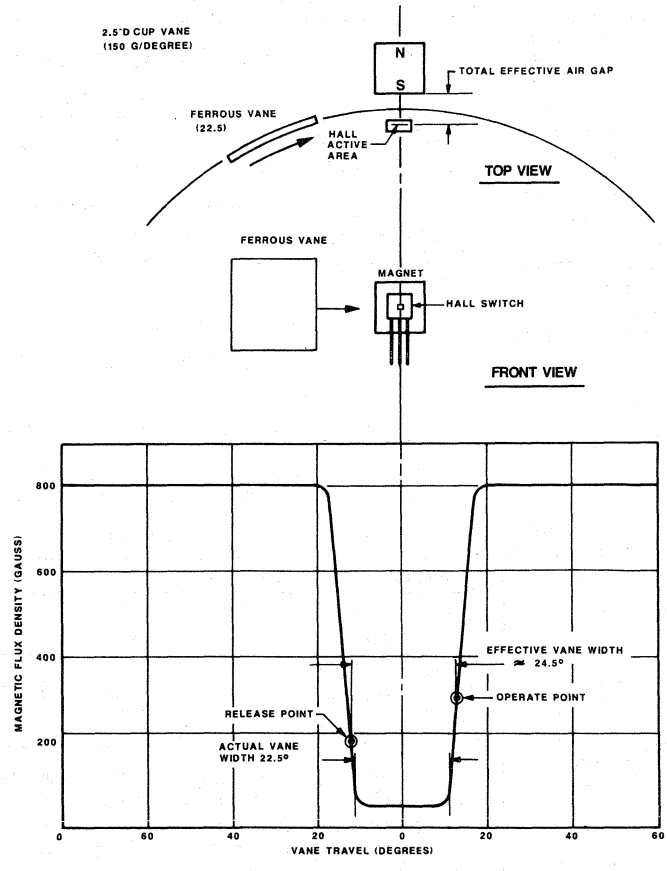

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FIGURE 35

Initially, when the vane is located entirely to the left of the magnet, the vane has no effect and the flux density at the sensor is at a maximum of 800 G. As the leading edge of the vane nears the magnet, the shunting effect of the vane causes the flux density to decrease in a nearly linear fashion. There, the magnet is covered by the vane and flux density is at a minimum. As the vane travels on it starts to uncover the magnet. This allows the flux to increase to its original value. After that, additional vane travel has no further influence on flux density at the sensor.

A Hall switch located in the position of the sensor would initially be ON because of the presence of the magnetic field. Somewhere in the linearly decreasing region, the flux would fall below the release point, and the Hall switch would turn OFF. It would remain OFF until the increasing flux reaches the operate point for that particular Hall switch. Recall that the operate point flux density is greater than the release point flux density by the amount of hysteresis for that particular Hall switch.

The interval during which the Hall switch remains OFF is determined by the actual width of the vane and the steepness of the magnetic slope, as well as by the operate and release point flux density values for the Hall switch. This interval is called the effective vane width, and it is always somewhat greater than the physical vane width.

ROTOR DESIGN

Two commonly used rotor configurations are the disk and the cup, as shown in Figure 36.

The disk is easily fabricated and, hence, is often used for low-volume applications such as machine control. Axial movement of the rotor must be considered. Vane activated switches tolerate this quite well, but the rotor must not hit the magnet or the Hall switch.

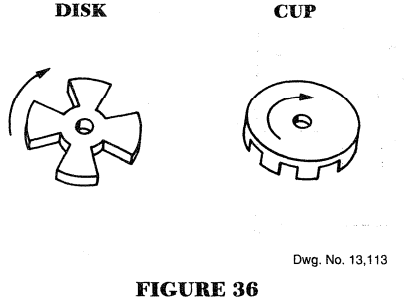

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FIGURE 36

Cup rotors are somewhat more difficult to fabricate and so are more expensive, but dealing with a single radial distance simplifies calculations and allows precise control of the output waveforms. For cup rotors, radial bearing wear or play is the significant factor in determining the clearances, while axial play is relatively unimportant. Cup rotors have been used very successfully in automotive ignition systems. The dwell range is determined by the ratio of the vane-to-window widths when the rotor is designed. Firing point stability may be held to ±0.005 distributor degrees per degree Celsius in a well-designed system.

MATERIAL

Vanes are made of a low carbon steel to minimize the residual magnetism and to give good shunting action. The vane thickness is chosen to avoid magnetic saturation for the value of flux density it must shunt. Vanes usually are between 0.03" and 0.06" thick.

VANE/WINDOW WIDTHS, ROTOR SIZE

Generally, the smallest vanes and window on a rotor should be at least one and one-half times the width of the magnet pole to provide adequate shunting action and to maintain sufficient differential between the OFF and ON values of flux density.

In Table 1, the maximum flux density (obtained with window centered over the magnet, the minimum flux density (vane centered over the magnet), and the difference between the two values are tabulated for three cases:

1. Vane and window width the same as magnet pole width.
2. Vane and window width one and one-half times magnet pole width.
3. Vane and window width two times the magnet pole width.

In each case the magnet is 0.25" x 0.25" x 0.125" samarium cobalt; the air gap is 0.1"; the rotor vanes are made of 0.04" mild steel stock.

TABLE 1

Window Vane Width Factor	1.0	1.5	2.0
Flux Density with Window Centered	630 G	713 G	726 G
Flux Density with Vane Centered	180 G	100 G	80 G
Flux Change Density	450 G	613 G	646 G

If a small rotor with many windows and vanes is required, a miniature rare earth magnet must be used to ensure sufficient flux density for reliable operation. For example, a 0.1" cubical samarium cobalt magnet makes it practical to fabricate a 1.25" diameter rotor with as many as 10 windows and vanes. With fewer vanes, even further size reduction is possible.

TABLE 2

Curve	Magnet	Air Gap	Slope G/mil	*Concentrator
A	0.25"D, 0.25"L Samarium Cobalt	0.1"	14	Yes
B	0.25"D, 0.25"L Samarium Cobalt	0.1"	9.85	No
C	0.25"D, 0.125"L Samarium Cobalt	0.1"	9.0	Yes
D	0.25"D, 0.125"L Samarium Cobalt	0.125"	8.7	Yes
E	0.25"D, 0.125"L Samarium Cobalt	0.1"	7.8	No
F	0.25"D, 0.125"L Samarium Cobalt	0.125"	6.3	No
G	0.25"D, 0.125"L Samarium Cobalt	0.125"	5.6	Yes
H	0.25"D, 0.125"L Samarium Cobalt	0.125"	4.5	No

NOTE: The "U" package is used for all measurements.*

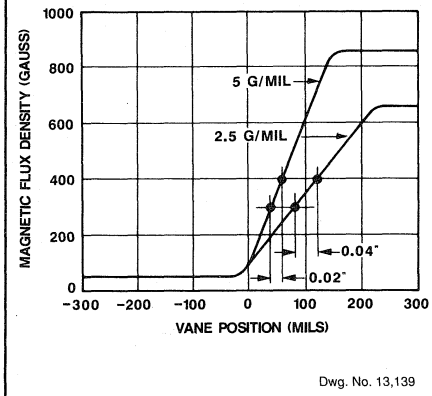

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FIGURE 37

STEEP MAGNETIC SLOPES FOR CONSISTENT SWITCHING

The flux density vane travel graph for most common vane configurations (Figure 35), is very nearly linear in the transition regions. The Hall switch operate and release points fall in these linear transition regions, and it is easily seen that if these values change, the position of the vane which causes the switching must change also. Figure 37 shows the flux density as a function of vane position for two different magnetic circuits. In one case, the magnetic slope is 2.5 G/mil. In the second case, it is 5.0 G/mil.

If the 2.5 G/mil system is used with a Hall switch known to have an operate point flux density of 300 G at + 25°C, the device would switch ON when the vane is 85 mils past the center of the window at this temperature. If the Hall switch operate point went up to 400 G at a temperature of +125°C (this represents Hall switch temperature coefficient of 1 G/°C), the vane must move to 120 mils past center, a change in switching position of 45 mils. If the same Hall switch is used in the second system having the 5 mil/G slope, the operate point would shift only 20 mils, or half as much, since the slope is twice as steep.

Slopes in typical vane systems range from 1 G/mil to 15 G/mil, and are affected by magnet type and size, the magnetic circuit, and the total effective air gap. It is interesting to note that, although slide-by operation can give very steep slopes, the transition point is much affected by lateral motion (change in air gap); therefore, vanes are often preferred for applications involving play or bearing wear.

SMALL AIR GAPS FOR STEEP SLOPES

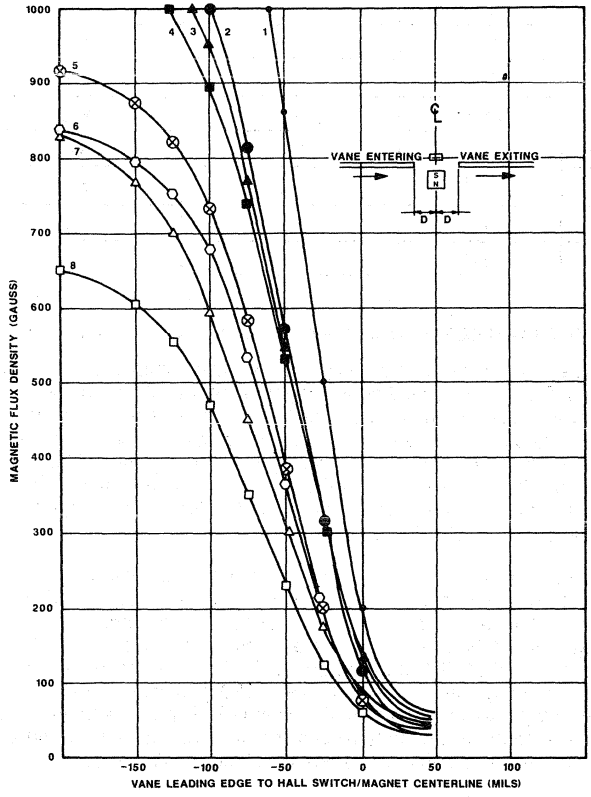
The air gap should be as small as the mechanical system allows. Factors to be considered are:

Vane material thickness and vane radius.

Maximum eccentricity for cup vanes.

Bearing tolerance and wear.

Change in air gap with temperature due to mounting considerations.



SYMBOL	MAGNET	AIR GAP	SLOPE(G/MIL)	*CONC.
1 ●	0.25"D,0.25"L SAM.CO.	0.1"	14	YES
2 ◉	0.25"D,0.25"L SAM.CO.	0.1"	9.85	NO
3 ▲	0.25"D,0.125"L SAM.CO.	0.1"	9.0	YES
4 ■	0.25"D,0.25"L SAM.CO.	0.125"	8.7	YES
5 ⊗	0.25"D,0.125"L SAM.CO.	0.1"	7.8	NO
6 ○	0.25"D,0.25"L SAM.CO.	0.125"	6.3	NO
7 △	0.25"D,0.125"L SAM.CO.	0.125"	5.6	YES
8 □	0.25"D,0.125"L SAM.CO.	0.125"	4.5	NO

NOTE - THE "U" PACKAGE IS USED FOR ALL MEASUREMENTS

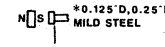


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FIGURE 38

In Figure 38, two different samarium cobalt magnets are used in a vane system to illustrate the effects of changes in air gap and magnet size. Note that only the falling transition region is shown (transition regions are symmetrical). The distances on the horizontal axis have been measured from the leading edge of the vane.

The term "air gap" as used in Figure 38 is not the total effective air gap; but is simply the distance from the face of the magnet to the surface of the Hall switch. It does not include the package contribution. The "U" package is often used in ferrous vane applications because it has a shallow active area depth.

FLUX CONCENTRATORS PAY DIVIDENDS

What if economic or size considerations dictated the smaller magnet used in Figure 38, and mechanical considerations dictated the larger (0.125") air gap, but the resulting flux density and slope (Curve 8) were not good enough? Curve 7 in Figure 38 shows the very substantial improvement that can be achieved by adding simple flux concentrators. Those used in the example were 0.125" in diameter by 0.250" long, and were fastened behind the Hall switch.

DESIGN EXAMPLE

The magnet/concentrator configuration we just considered (Curve 7, Figure 38) seems to offer a high performance/cost ratio. Following is an evaluation of its use in an automotive ignition system using a 2.5" diameter cup rotor.

The initial timing and wide operating temperature range requirements for this application have generally led designers to specify custom Hall switches in terms of the minimum and maximum operate or release point at +25°C, plus a maximum temperature coefficient on these parameters over the operating temperature range. Representative specifications might be:

+25°C Operate Point, Minimum ..... 300 G

+25°C Operate Point, Maximum ..... 450 G

+25°C Release Point, Minimum ..... 200 G

Temperature Coefficients:

Δ O.P./Δ T, maximum = +0.7 G/°C

Δ R.P./Δ T, maximum = +1.0 G/°C

Solid-state Hall effect ignition systems can be designed to fire either on operate or release of the Hall switch. We have arbitrarily chosen to have the system in this example fire when the switch operates and, thus, the operate point specifications of the Hall switch (between 300 and 450 G at +125°C) will determine the amount of uncertainty in the initial timing of the spark. It is possible that the mechanical system would also make a contribution, but that is not considered here.

Figure 39 shows the measured flux density at the position of the sensor as a function of the vane travel. The shape of the curve requires explanation: Because the flat minimum and maximum flux regions are irrelevant, it is convenient to measure from the vane's leading edge to

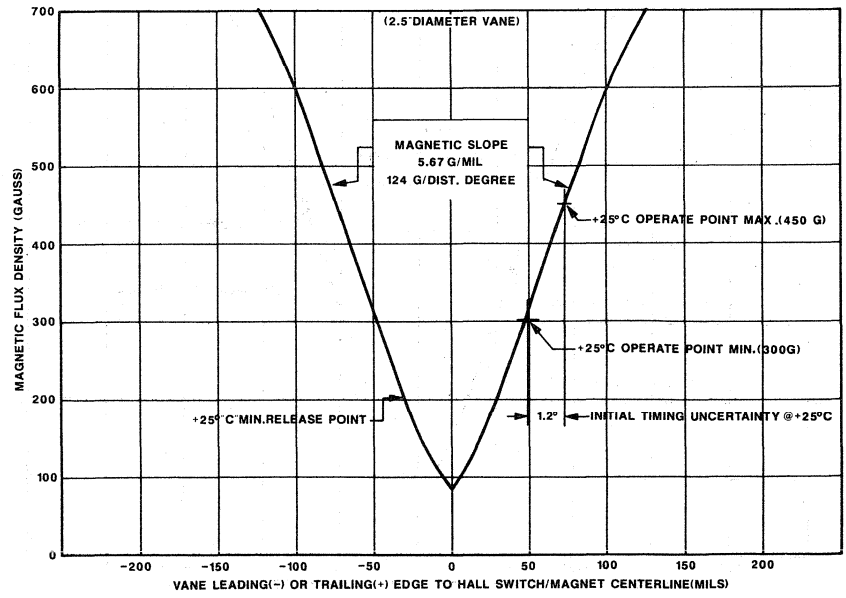

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FIGURE 39

edge of the vane to the magnet centerline while plotting data for the rising transition. (The same presentation would result if all data were plotted while a vane passed the magnet, the center low flux areas were snipped out, and the ends containing the linear transitions were pulled together.) From this graph, we can identify the magnetic slope of the transition regions for our system—approximately 5.67 G per 0.001" of vane travel.

Calculations based on the rotor diameter (2.5") show we have 22 mils of vane travel per distributor degree. The 5.67 G/mil slope obtained from Figure 39 is equivalent to 125 G per distributor degree. From the specifications, it is known that the Hall switch will operate when flux is between 300 and 450 G, leaving a 150 G window of uncertainty. At +25°C, this will be:

$$150\ \text{G} \times \frac{\text{Distributor Degree}}{125\ \text{G}} =$$

1.2 Distributor Degrees

Additional contributions to the initial timing uncertainty will result if the total effective air gap is changed, as that would affect the shape or slopes of the magnetic flux density/vane travel curve of Figure 39. Factors to be considered are the magnet peak energy product tolerances, as well as manufacturing tolerances in the final Hall switch/magnet assembly.

TEMPERATURE STABILITY OF OPERATE POINT

The Hall switch operate point temperature coefficient is approximately 0.2 G/°C for a UGN/UGS3130. To translate this into distributor degrees per degree Celsius, we take:

$$\frac{0.2\ \text{G}}{1°\text{C}} \times \frac{\text{Distributor Degrees}}{125\ \text{G}} =$$

0.0016 Distributor Degrees/°C

The distributor timing would, therefore, change 0.16 degrees for a temperature change of 100°C.

A typical samarium cobalt magnet temperature coefficient is -0.04%/°C. A magnetic field of 375 G at +25°C would decrease to 360 G at +125°C. For Figure 40, our system has a magnetic slope of 5.67 G/mil, giving an additional vane travel requirement at +125°C of:

$$(375\ \text{G}-360\ \text{G}) \times \frac{1\ \text{mil}}{5.67\ \text{G}} = 2.7\ \text{mils}$$

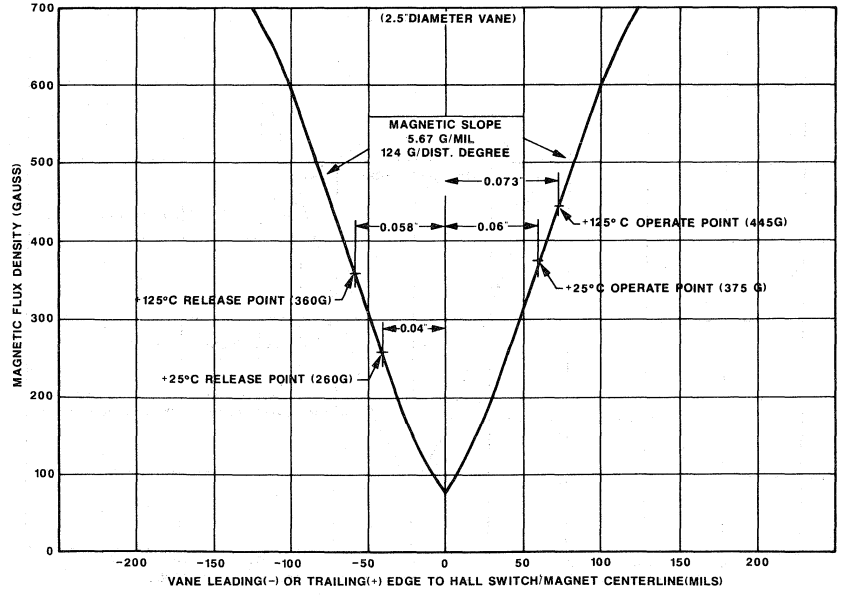

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FIGURE 40

This translates to timing change of:

$$2.7 \text{ mils} \times \frac{\text{Distributor Degree}}{22 \text{ mils}} =$$

0.12 Distributor Degrees

for a temperature change of 100°C.

CALCULATING DWELL ANGLE AND DUTY CYCLE VARIATIONS

The dwell angle in a conventional system is the number of distributor degrees during which the points are closed, which corresponds to the amount of time current can flow in the coil's primary winding. In our example, current flows in the coil primary from the time the Hall switch releases until it operates, which is called the effective vane width. For nostalgic reasons we will assume an eight-cylinder engine, which requires a distributor rotor with eight windows and eight vanes of equal size. One window-vane segment thus occupies 45 distributor degrees and will fire one cylinder. Let us further assume a typical Hall switch operate point of 375 G at +25°C (A), and a +25°C release point of 260 G (B). From Figure 40 we find that the points will close 40 mils before the vane's leading edge passes the magnet centerline; they open 60 mils after the vane's trailing edge passes the magnet centerline. The effective vane width is greater than the mechanical vane width by an amount:

$$(60 \text{ mils} + 40 \text{ mils}) \times \frac{\text{Distributor Degree}}{22 \text{ mils}} =$$

4.54 Distributor Degrees

This gives a dwell angle of (45° + 4.54°) = 49.54 distributor degrees at +25°C. The duty cycle is:

$$\frac{49.54°}{90°} = 55.0\% \text{ at } +25°C.$$

Using the specified worst-case temperature coefficients, we calculate the new operate and release points at +125°C to be 445 G (C) and 360 G (D), also shown in Figure 40. The dwell angle at +125°C would then be:

$$45° + \left[(73 \text{ mils} + 58 \text{ mils}) \times \frac{\text{Distributor Degree}}{22 \text{ mils}}\right] =$$

50.9 Distribution Degrees

The duty cycle is then:

$$\frac{50.9°}{90°} = 56.6\%$$

EFFECTS OF BEARING WEAR

A ±10 mil radial movement of the vane, with its position adjusted to the approximate operate point of the Hall switch, gave a measured change of ±6 G. This translates into a change of:

$$6 \text{ G} \times \frac{\text{Distributor Degrees}}{125 \text{ G}} =$$

0.048 Distributor Degrees,

which is equivalent to 0.097 crankshaft degrees.

MOUNTING ALSO AFFECTS STABILITY

In the example above, it was assumed that the physical relationship between the Hall switch and the magnet was absolutely stable. In practice, it is necessary to design the mountings with some care if this is to be true. It has been found that supporting the magnet or Hall switch with formed brackets of aluminum or brass will often contribute a significant temperature-related error to the system. Use of molded plastic housings has proven to be one of the better mounting techniques.

INDIVIDUAL CALIBRATION TECHNIQUES

In some applications, it may be desirable to have the vane switch assemblies operate within a narrower range of vane edge positions than is possible with a practical operate point specification for the Hall switch; for example, if it were necessary to reduce the initial timing window in the previous case. One solution would be individual calibration. Possible techniques include:

1) Adjusting the air gap by changing the magnet position.
2) Adjusting the position of a flux concentrator behind the Hall switch.
3) Adjusting the position of a small bias magnet mounted behind the Hall switch.
4) Demagnetizing the magnet in small increments that would decrease the magnetic slope and, thus, increase the temperature effects.
5) Adjusting the position of the Hall switch-magnet assembly relative to the rotor in a manner similar to rotating an automotive distributor to change the timing.

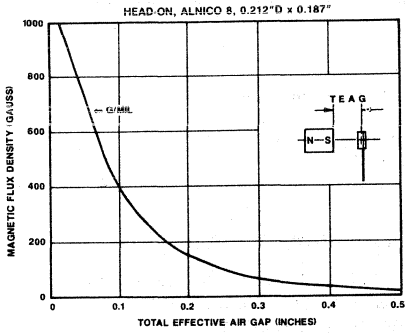

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FIGURE 41

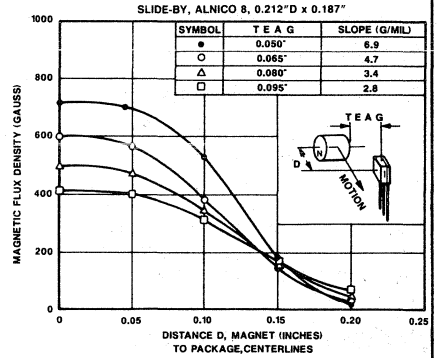

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FIGURE 42

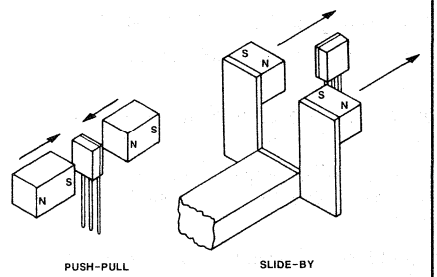

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FIGURE 43

OPERATING MODES

HEAD-ON AND SLIDE-BY MODES

The most common operating modes are head-on and slide-by. The head-on mode is simple and relatively insensitive to lateral motion, but cannot be used where overextension of the mechanism might damage the Hall switch. The flux density plot for a typical head-on operation (Figure 41) shows that the magnetic slope is quite shallow for low values of flux density, a disadvantage that generally requires extreme mechanism travel and extreme sensitivity to flux changes in operate and release points of the Hall switch. This problem can be overcome by selecting Hall switches with higher operate and release properties.

The slide-by mode is also simple, can have reasonably steep slopes (to about 10 G/mil) and has no problem with mechanism overtravel. It is, however, very sensitive to lateral play, as the flux density varies dramatically with changes in the air gap. This can be seen clearly in the curves of Figure 42, in which the flux density curves are plotted for actual slide-by operation with various air gaps. It is apparent that the operating mechanism can have little side play if precise switching is required.

OPERATING MODE ENHANCEMENTS —COMPOUND MAGNETS

PUSH-PULL

Because the active area of a Hall switch is close to the branded face of the package, it is usually operated by approaching this face with a magnetic south pole. It is also possible to operate a Hall switch by applying a magnetic north pole to the back side of the package. While a north pole alone is seldom used, the push-pull configuration (simultaneous application of a south pole to the branded side and a north pole to the back side) can give much greater field strengths than are possible with any single magnet (Figure 43). Perhaps more important, push-pull arrangements are quite insensitive to lateral motion and are worth considering if a loosely fitting mechanism is involved.

Figure 44 shows the flux density curve for an actual push-pull slide-by configuration that achieves a magnetic slope of about 8 G/mil.

PUSH-PUSH

Another possibility, a bipolar field with a fairly steep slope (which is also linear), can be created by using a push-push configuration in the head-on mode. (Figure 45)

In the push-push mode, head-on configuration as shown in Figure 45, the magnetic fields cancel each other when the mechanism is centered, giving zero flux density at that position. Figure 46 shows the flux density plot of such a configuration. The curve is linear and moderately steep at better than 8 G/mil. The mechanism is fairly insensitive to lateral motion.

BIASED OPERATION

It is also possible to bias the Hall switch by placing a stationary north or south pole behind it to alter the operate and release points. For example, a north pole attached to the reverse face would turn the device normally ON until a north pole providing a stronger field in the opposite direction approached the opposite face. (Figure 47)

Figures 48-51 demonstrate four additional slide-by techniques. Compound magnets are used in push-pull, slide-by, edgewise configurations to achieve a magnetic slope of 17.4 G/mil. Rare earth magnets may be used to obtain substantially steeper slopes. A flux density curve of up to 100 G/mil is obtainable.

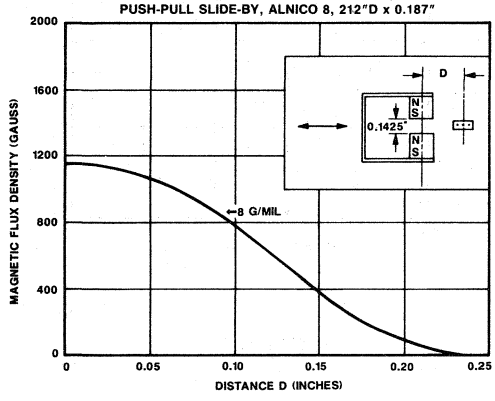

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FIGURE 44

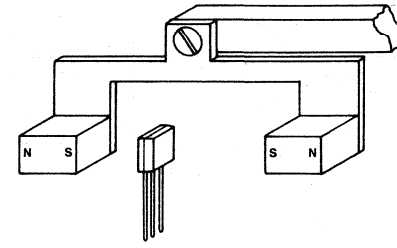

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FIGURE 45

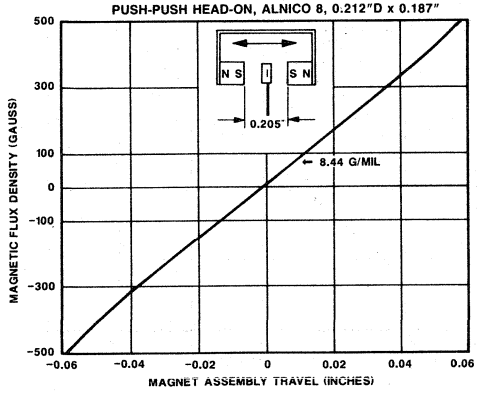

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FIGURE 46

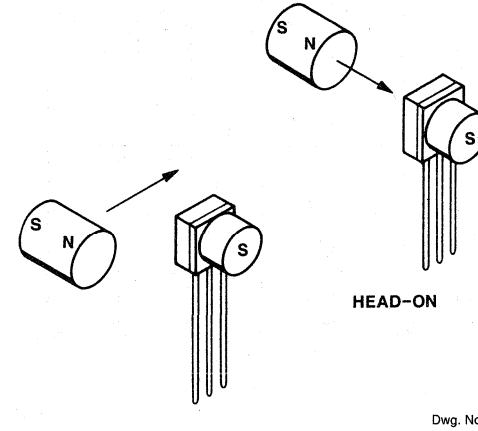

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FIGURE 47

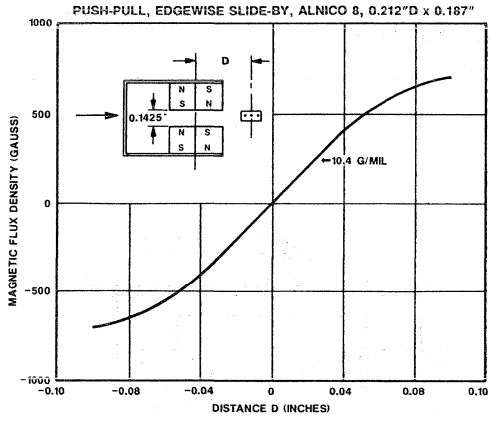

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FIGURE 48

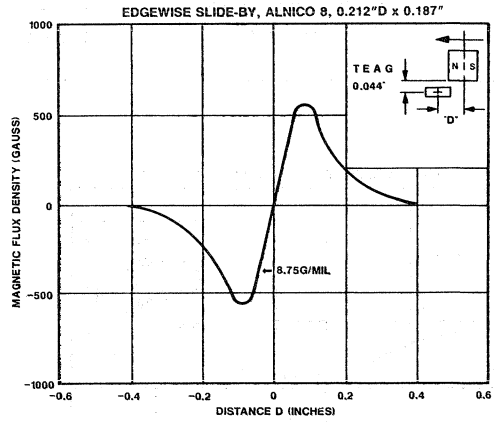

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FIGURE 49

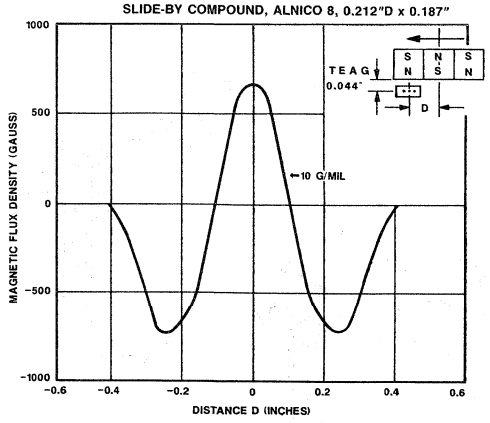

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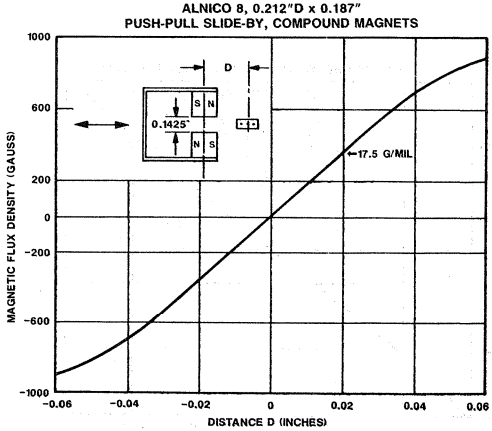
FIGURE 50



Dwg. No. 13,153

FIGURE 51

INCREASING FLUX DENSITY BY IMPROVING THE MAGNETIC CIRCUIT

Magnetic flux can travel through air, plastic, and most other materials only with great difficulty. Since there is no incentive for flux from the activating magnet to flow through the (plastic and silicon) Hall device, only a portion of it actually does. The balance flows around the device and back to the other pole by whatever path offers the least resistance. (Figure 52)

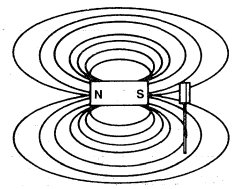


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FIGURE 52

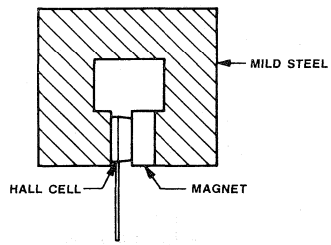

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FIGURE 53

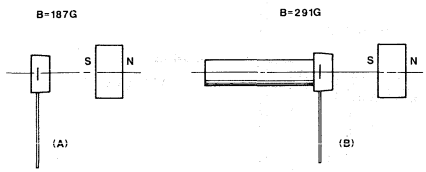

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FIGURE 54

However, magnetic flux easily flows through a ferromagnetic material such as mild steel. The reluctance of air is greater by a factor of several thousand than that of mild steel.

In a Hall device application, the goal is to minimize the reluctance of the flux path from the magnetic south pole, through the Hall device, and back to the north pole. The best possible magnetic circuit for a Hall device would provide a ferrous path for the flux, as shown in Figure 53, with the only "air gap" being the Hall device itself.

While a complete ferrous flux path is usually impractical, unnecessary, and even impossible in applications requiring an undistorted or undisturbed flux field, it is a useful concept that points the way to a number of very practical compromises for improving flux density.

FLUX CONCENTRATORS

Flux concentrators are low carbon (cold-rolled) steel magnetic conductors. They are used to provide a low reluctance path from a magnet's south pole, through the Hall sensor, and back to the north pole. Flux concentrators can take many forms and will often allow use of smaller or less expensive magnets (or less expensive, less sensitive Hall devices) in applications where small size or economy are important. They are of value whenever it is necessary or desirable to increase flux density at the Hall device. Increases of up to 100% are possible.

An example of the effectiveness of a concentrator is illustrated in Figures 54(A) and 54(B).

(A) The south pole of a samarium cobalt magnet 0.25" square and 0.125" long, is spaced 0.25" from the Hall switch. There is a flux density of 187 G at the active area.

(B) With a concentrator 0.125" in diameter and 0.5" long, the flux density increases to 291 G.

SIZE OF THE CONCENTRATOR

The active area of the Hall device is typically 0.01" square. Best results are obtained by tapering the end of the concentrator to approximately the same dimensions. With the "U" package, however, there is 0.044" from the active area to the rear surface of the package. Due to this 0.044" distance, a slightly larger end to the concentrator results in higher values of flux density at the active area. If the end is too large, the flux is insufficiently concentrated. Figure 55(A), (B), and (C) illustrates these effects using cylindrical flux concentrators and a 0.25" gap.

The length of the concentrator also has an effect on the flux density. This is illustrated in Figure 56.

Cylindrical concentrators were used here for convenience, but the body of the concentrator has little effect. The important factors are the shape, position, and surface area of the magnet end nearest the Hall sensor.

The effectiveness of other concentrator configurations can be measured easily by using a calibrated linear Hall device, such as the UGN3503U, or a commercial gaussmeter.

MOUNTING THE MAGNET TO A FERROUS PLATE

Mounting the magnet to a ferrous plate will give an additional increase in flux density at the Hall element. Using the same configuration as in Figure 55(C), which produced 291 G, note the available flux attained in Figure 57(A) and (B) with the addition of the ferrous plate.

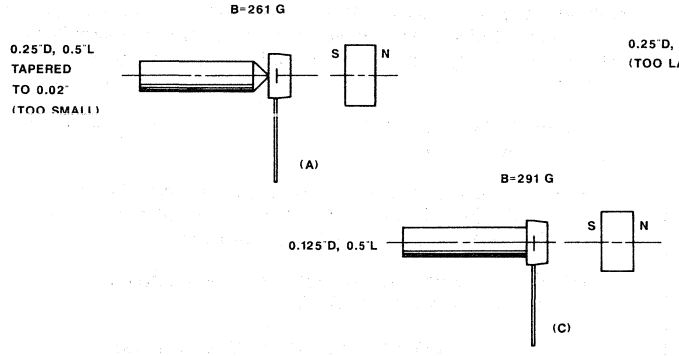
Figure 58 shows a possible concentrator for a ring magnet application. Using a flux concentrator that extends to both of the adjacent north poles, flux density increases from 265 G to 400 G (0.015" air gap). Note that the concentrator has a dimple, or mesa, centered on the Hall device. In most applications, the mesa will give a significant increase in flux density over a flat mounting surface.

ATTRACTIVE FORCE AND DISTORTED FLUX FIELD

Whenever a flux concentrator is used, an attractive force exists between magnet and concentrator. That may be undesirable.

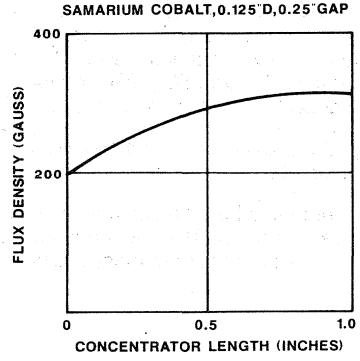
FEED-THROUGHS

An example of the use of a magnetic conductor to feed flux through a nonferrous housing is shown in Figure 59. A small electric motor has a 0.125" cube samarium cobalt magnet mounted in the end of its rotor, as shown. A 0.125" cube ferrous conductor extends through the alloy case with a 0.031" air gap between it and the magnet's south pole. The Hall switch is mounted at the other end with a flux concentrator behind it.



Dwg. No. 13,157

FIGURE 55



Dwg. No. 13,158

FIGURE 56

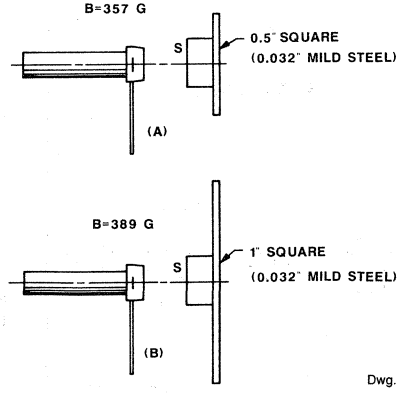


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FIGURE 57

In general, the feed-through should be of approximately the same cross-sectional area and shape as is the magnet pole.

This concept can be used to feed flux through any non-ferrous material, such as a pump case, pipe, or panel.

The two curves of Figure 60 illustrate the effects on flux density of increasing the length of the feed-through, as well as the contribution by the flux concentrator behind the Hall switch. Values for curve A were obtained with the flux concentrator in place, those for curve B without it. In both cases, the highest flux densities were achieved with the shortest feed-through dimension L, which was 0.125". Peak flux density was 350 G with flux concentrator in place, 240 G without it.

MAGNET SELECTION

A magnet must operate reliably with the total effective air gap in the working environment. It must fit the available space. It must be mountable, affordable, and available.

FIGURES OF MERIT

The figures of merit commonly applied to magnetic materials are:

Residual Induction (B_r) in gauss: How strong is the magnetic field?

Coercive Force (H_c) in oersteds: How well will the magnet resist external demagnetizing forces?

Maximum Energy Product (BH_{max}) in gauss-oersteds times 10^6. A strong magnet that is also very resistant to demagnetizing forces has a high maximum energy product. Generally, the larger the energy product, the better, stronger, and more expensive the magnet.

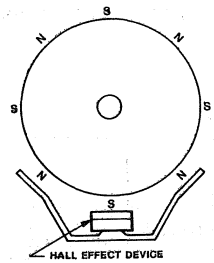

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FIGURE 58

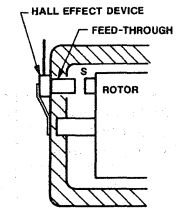

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FIGURE 59

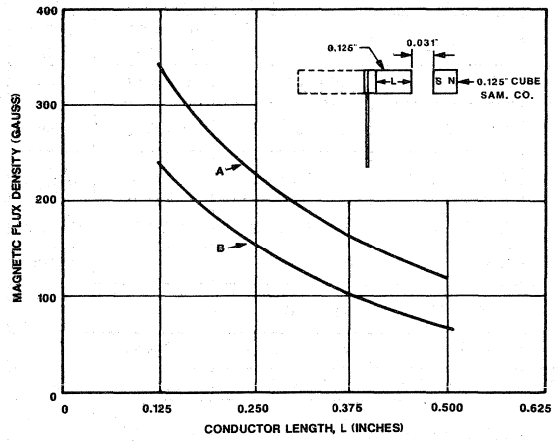

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FIGURE 60

Temperature Coefficient: The rate of change of the operate or release point over temperature, measured in gauss per degree Celsius. How much will the strength of the magnet change as temperature changes?

MAGNETIC MATERIALS

Neodymium (Ne-Fe B)—The new neodymium-iron-boron alloys fill the need for a high maximum-energy product, moderately priced magnet material. The magnets are produced by either a powdered-metal technique called orient-press-sinter or a new process incorporating jet casting and conventional forming techniques. Current work is being directed toward reducing production costs, increasing operating temperature ranges and decreasing temperature coefficients. Problems relating to oxidation of the material can be overcome through the use of modern coatings technology. Maximum energy products range from 7.0 to 15.0 MGOe depending on the process used to produce the material.

Rare Earth—Cobalt is an alloy of a rare earth metal, such as samarium, with cobalt (abbreviated RE cobalt). These magnets are the best in all categories, but are also the most expensive by about the same margins. Too hard for machining, they must be ground if shaping is necessary. Maximum energy product, perhaps the best single measure of magnet quality, is approximately 16×10^6.

Alnico is a class of alloys containing aluminum, nickel, cobalt, iron, and additives that can be varied to give a wide range of properties. These magnets are strong and fairly expensive, but less so than RE cobalt. Alnico magnets can be cast, or sintered by pressing metal powders in a die and heating them. Sintered Alnico is well suited to mass production of small, intricately shaped magnets. It has more uniform flux density, and is mechanically superior. Cast Alnico magnets are generally somewhat stronger. The non-oriented or isotropic Alnico alloys (1, 2, 3, 4) are less expensive and magnetically weaker than the oriented alloys (5, 6, 5-7, 8, 9). Alnico is too hard and brittle to be shaped except by grinding. Maximum energy product ranges from 1.3×10^6 to 10×10^6.

Ceramic magnets contain barium or strontium ferrite (or another element from that group) in a matrix of ceramic material that is compacted and sintered. They are poor conductors of heat and electricity,

TABLE 4
Properties of Magnetic Materials

Material	Maximum Energy Product (Gauss-Oersted)	Residual Induction (Gauss)	Coercive Force (Oersteds)	Temperature Coefficient	Cost	Comments
R.E. Cobalt	16×10^6	8.1×10^3	7.9×10^3	-0.05%/°C	Highest	Strongest, smallest, resists demagnetizing best
Alnico 1, 2, 3, 4	$1.3 - 1.7 \times 10^6$	$5.5 - 7.5 \times 10^3$	$0.42 - 0.72 \times 10^3$	-0.02%/°C to -0.03%/°C	Medium	Non-oriented
Alnico 5, 6, 5-7	$4.0 - 7.5 \times 10^6$	$10.5 - 13.5 \times 10^3$	$0.64 - 0.78 \times 10^3$	-0.02%/°C to -0.03%/°C	Medium-High	Oriented
Alnico 8	$5.0 - 6.0 \times 10^6$	$7 - 9.2 \times 10^3$	$1.5 - 1.9 \times 10^3$	-0.01%/°C to +0.01%/°C	Medium-High	Oriented, high coercive force, best temperature coefficient
Alnico 9	10×10^6	10.5×10^3	1.6×10^3	-0.02%/°C	High	Oriented, highest energy product
Ceramic 1	1.0×10^6	2.2×10^3	1.8×10^3	-0.2%/°C	Low	Non-oriented, high coercive force, hard, brittle, non-conductor
Ceramic 2, 3, 4, 6	$1.8 - 2.6 \times 10^6$	$2.9 - 3.3 \times 10^3$	$2.3 - 2.8 \times 10^3$	-0.2%/°C	Low-Medium	Partially oriented, very high coercive force, hard, brittle, non-conductor
Ceramic 5, 7, 8	$2.8 - 3.5 \times 10^6$	$3.5 - 3.8 \times 10^3$	$2.5 - 3.3 \times 10^3$	-0.2%/°C	Medium	Fully oriented, very high coercive force, hard, brittle, non-conductor
Cunife	1.4×10^6	5.5×10^3	0.53×10^3	—	Medium	Ductile, can cold form and machine
Fe-Cr	5.25×10^6	13.5×10^3	0.60×10^3	—	Medium-High	Can machine prior to final aging treatment
Plastic	$0.2 - 1.2 \times 10^3$	$1.4 - 3 \times 10^3$	$0.45 - 1.4 \times 10^3$	-02%/°C	Lowest	Can be molded, stamped, machined
Rubber	$0.35 - 1.1 \times 10^6$	$1.3 - 2.3 \times 10^3$	$1 - 1.8 \times 10^3$	-0.2%/°C	Lowest	Flexible
Neodymium	$7 - 15 \times 10^6$	$6.4\ 11.75 \times 10^3$	$5.3 - 6.5 \times 10^3$	-.157%/°C to -.192%/°C	Medium-High	Non-oriented

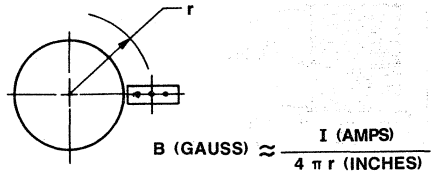

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FIGURE 61

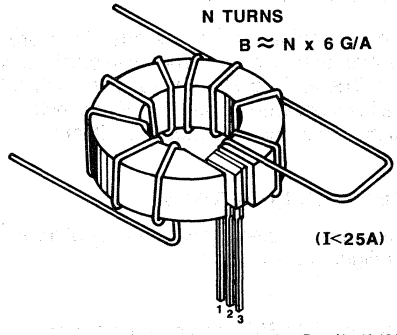

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FIGURE 62(A)

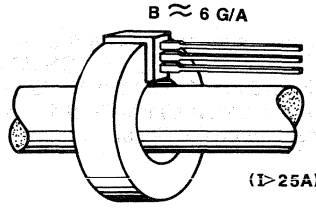

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FIGURE 62(B)

are chemically inert, and have-high values of coercive force. As with Alnico, ceramic magnets can be fabricated with partial or complete orientation for additional magnetic strength. Less expensive than Alnico, they also are too hard and brittle to shape except by grinding. Maximum-energy product ranges from 1 x 10^6 to 3.5 x 10^6.

Cunife is a ductile copper base alloy with nickel and iron. It can be stamped, swaged, drawn, or rolled into final shape. Maximum energy product is approximately 1.4 x 10^6.

Iron-Chromium magnets have magnetic properties similar to Alnico 5, but are soft enough to undergo machining operations before the final aging treatment hardens them. Maximum energy product is approximately 5.25 x 10^6.

Plastic and rubber magnets consist of barium or strontium ferrite in a plastic matrix material. They are very inexpensive and can be formed in numerous ways including stamping, molding, and machining, depending upon the particular matrix material. Since the rubber used is synthetic, and synthetic rubber is also plastic, the distinction between the two materials is imprecise. In common practice, if a plastic magnet is flexible, it is called a rubber magnet. Maximum energy product ranges from 0.2 x 10^6 to 1.2 x 10^6.

CHOOSING MAGNET STRENGTH

A magnet must have sufficient flux density to reach the Hall switch maximum operate point specification at the required air gap. Good design practice suggests the addition of another 50 G to 100 G for insurance and a check for sufficient flux at the expected temperature extremes.

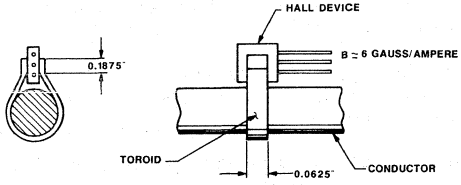
The data sheet on the UGN3120U Hall switch specifies a 350 G maximum operate point at +25°C. After adding a pad of 100 G, we have 450 G at +25°C. If operation to +70°C is needed, the requirement is 450 G + 45 G = 495 G. (For calculations, we use 0.7 G/°C operate point coefficient and 1 G/°C release point coefficient.) Since the temperature coefficient of most magnets is negative, this factor would also require some extra flux at room temperature to guarantee high-temperature operation.

COERCIVE FORCE

Coercive force becomes important if the operating environment will subject the magnet to a strong demagnetizing field, such as that encountered near the rotor of an ac motor. For such applications, a permanent magnet with high coercive force (ceramic, Alnico 8, or, best of all, RE cobalt) is clearly indicated.

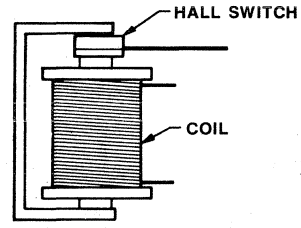
PRICE AND PEAK ENERGY PRODUCT

The common permanent magnet materials and their magnetic properties are summarized in Table 4. The cost column shows the relationship between the price paid for a magnet and its peak energy product.



Dwg. No. 13,166

FIGURE 63



Dwg. No. 13,167

FIGURE 64

CURRENT LIMITING AND MEASURING

CURRENT SENSORS

Hall effect devices are excellent current-limiting or measuring sensors. Their response ranges from dc to the kHz region. The conductor need not be interrupted in high-current applications.

The magnetic field about a conductor is normally not intense enough to operate a Hall effect device (Figure 61).

The radius, r, is measured from the center of the conductor to the active area of the Hall device. With a radius of 0.5" and a current of 1,000 A, there would be a magnetic flux density of 159 G at the Hall device. At lower current, use a toroid or closed magnetic circuit to increase the flux density, as illustrated in Figure 62(A) and (B).

With a 0.06" air gap for the "U" package, there would be 6 G/A per turn for Figure 62(A), and 6 G/A for Figure 62(B).

The core material can be of either ferrite or mild steel (C-1010) for low-frequency applications, and ferrite for high-frequency measurements.

The main concerns are:

That the core retains minimal field when the current is reduced to zero.

That the flux density in the air gap is a linear function of the current.

And that the air gap is stable over the operating temperature range.

The cross-sectional dimensions of the core are at least twice the air gap dimension to ensure a reasonably homogeneous field in the gap. For example, a toroid with a 0.06" gap would have at least a 0.12" x 0.12" cross-section.

Another simple and inexpensive application is illustrated in Figure 63. A toroid of the appropriate diameter is formed from mild steel stock, 0.0625" thick and 0.1875" wide. The ends are formed to fit on each side of the central portion of the Hall device. One advantage of this technique is that the toroid can be placed around a conductor without disconnecting the conductor.

MULTI-TURN APPLICATIONS

There are several considerations in selecting the number of turns for a toroid such as the one in Figure 62(A):

Hall Switches

Keep the flux density in the 200 G to 300 G range for a trip point. Devices can be supplied with a narrow distribution of magnetic parameters within this range. If, for example, you want the Hall switch to turn ON at 10 A:

$$N = \frac{300\ G}{6\ G/A \times 10\ A} = 5\ \text{turns}$$

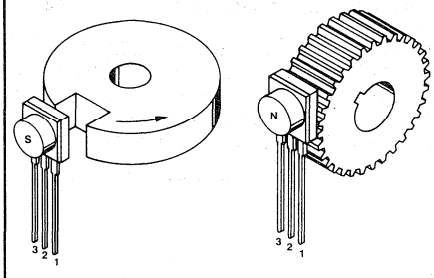
It is possible to supply parts having a ±20% operating point window in this range.

Hall Linears

It is desirable to have flux density in the 200 G to 300 G range to maximize the output signal/zero drift ratio. In using the UGN3501, for example, the zero drift is typically 0.15 mV/°C, so from 0°C to +70°C there would be typically a ±7 mV zero drift. A sensitivity of 1.4 mV/G and a 300 G field would give a 420 mV output signal.

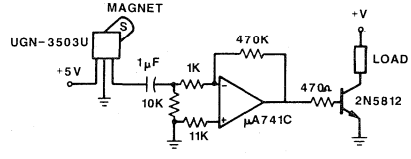
The UGN3501 also has a -0.3%/°C sensitivity coefficient. For example, a 420 mV output signal at 0°C would drop to 330 mV at +70°C.

For low-current applications in which many turns are required, one can wind a bobbin, slip it over a core, and complete the magnetic circuit through the Hall device with a bracket-shaped pole piece, as shown in Figure 64.



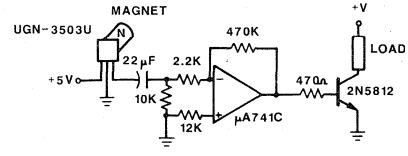
Dwg. No. 13,168

FIGURE 65



Dwg. No. 13,169

FIGURE 66



Dwg. No. 13,170

FIGURE 67

With this bobbin-bracket configuration, it is possible to measure currents in the low milliampere range or to replace a relay using a Hall switch. To activate a Hall switch at 10 mA (±20%), using a device with a 200 G (±40 G) operate point, bobbin windings require:

$$N = \frac{200\ G}{6\ G/A \times 0.01\ A} = 3333\ turns$$

It would be practical to tweak the air gap for final, more precise calibration. In all cases, *be careful not to stress the package.*

OTHER APPLICATIONS FOR LINEAR SENSORS

Type UGN3503U and UGS3503U Hall Effect linear sensors are used primarily to sense relatively small changes in magnetic field—changes too small to operate a Hall Effect switching device. They are customarily capacitively coupled to an amplifier, which boosts the output to a higher level.

As motion detectors, gear tooth sensors, and proximity detectors (Figure 65), they are magnetically driven mirrors of mechanical events. As sensitive monitors of electromagnets, they can effectively measure a system's performance with negligible system loading while providing isolation from contaminated and electrically noisy environments.

Each Hall effect integrated circuit includes a Hall sensing element, linear amplifier, and emitter-follower output stage. Problems associated with handling tiny analog signals are minimized by having the Hall cell and amplifier on a single chip.

The output null voltage of Type 3503 is nominally one-half the supply voltage. A south magnetic pole presented to the branded face of the Hall effect sensor will drive the output higher than the null voltage level. A north magnetic pole will drive the output below the null level.

In operation, instantaneous and proportional output-voltage levels are dependent on magnetic flux density at the most sensitive area of the device. Greatest sensitivity is obtained with a supply voltage of 6 V, but at the cost of increased supply current and a slight loss of output symmetry. The sensor's output is usually capacitively coupled to an amplifier that boosts the output above the millivolt level.

In the two applications shown in Figures 66 and 67, permanent bias magnets are attached with epoxy glue to the back of the epoxy packages. The presence of ferrous material at the face of the package then acts as a flux concentrator.

The south pole of a magnet is attached to the back of the package if the Hall effect IC is to sense the presence of ferrous material. The north pole of a magnet is attached to the back surface if the integrated circuit is to sense the absence of ferrous material.

Calibrated linear Hall devices, which can be used to determine the actual flux density presented to the Type 3503 sensor in a particular application, are available.

FERROUS METAL DETECTORS

Two similar detector designs are illustrated in Figures 68 and 69. The first senses the presence of a ferrous metal; the other senses an absence of the metal. The two sensing modes are accomplished simply by reversing the magnet poles relative to the UGN3501. The pole of the magnet is affixed to the unbranded side of the UGN3501 in both cases.

Frequency response characteristics of this circuit are easily controlled by changing the value of the input decoupling capacitor for the low-frequency break-point. If high-frequency attenuation is desired, a capacitor can be used to shunt the feedback resistor.

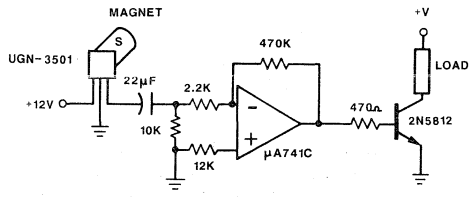
METAL SENSOR

The north pole of the magnet is affixed to the back side of a UGN3501. The sensor is in contact with the bottom of a 0.09375" epoxy board. A 20 mV output change (decrease) is produced as a 1" steel ball rolls over the sensor. This signal is amplified and inverted by the μA 741C operational amplifier and drives the 2N8512 ON.

NOTCH SENSOR

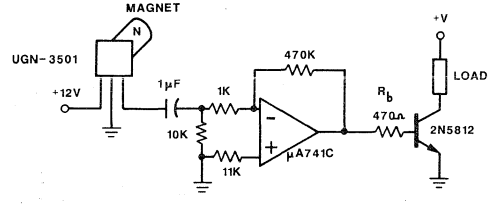
The south pole of the magnet is fixed to the backside of a UGN3501. The sensor is 0.03125" from the edge of a steel rotor. A 0.0625" wide by 0.125' deep slot in the rotor edge passing the sensor causes a 10 mV peak output change (decrease). This signal is amplified and inverted by the μA 741C op amp and drives the 2N5812 ON.

Note that, in both examples, the branded side of the UGN3501 faces the material (or lack of material) to be sensed. In both cases, the presence (or absence) of the ferrous metal changes the flux density at the Hall Effect sensor so as to produce a negative going output pulse. The pulse is inverted by the amplifier to drive the transistor ON.



Dwg. No. 13,171

FIGURE 68



Dwg. No. 13,172

FIGURE 69

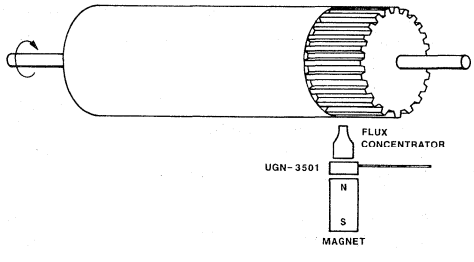


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FIGURE 70

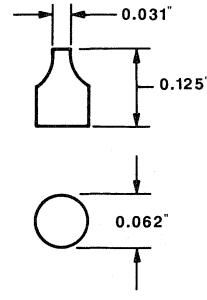

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FIGURE 71

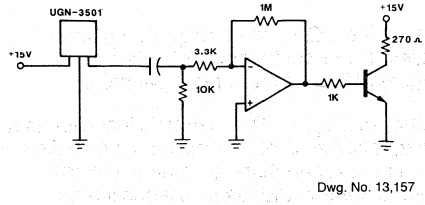

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FIGURE 72

PRINTER APPLICATION

The device in Figure 70 senses lobes on a character drum. Lobes are spaces 0.1875" apart around the circumference, are 0.25" long and rise 10 to 15 mils from the surface of the drum.

A UGN3501 Hall effect linear IC sensor is used with an Indiana General Magnet Products Company SR8522 magnet. The north pole is affixed to the reverse side of the package. A flux concentrator is affixed to the branded face. Though it does not provide a flux return path, a concentrator will focus the magnetic field through the switch.

The concentrator blade, shown in Figure 71, is aligned with the drum lobe at an air gap distance of 0.01". The output change is 10 mV peak, amplified as shown to develop a +3 V output from the operational amplifier, driving the transistor ON, as illustrated in Figure 72.

Sensitivity is so great in this configuration that the UGN3501 output signal's baseline quite closely tracks eccentricities in the drum. This affects lobe resolution, but lobe position can still be measured.

USING CALIBRATED DEVICES

UGN3503U

The calibrated Type 3503 is an accurate, easy-to-use tool for measuring magnetic flux densities. Each device is individually calibrated and furnished with a calibration curve and sensitivity coefficient. Although calibration is performed in a south and north 500 G field, the UGN3503 is useful for measuring fields in both polarities to 1000 G.

A closely regulated 5 V (±10 mV) power supply is necessary to preserve accuracy in calibrated UGN3503 flux measurements. An ambient temperature range of 21°C to 25°C must also be maintained.

Connect Pin 1 to voltage V_{CC}, Pin 2 to ground, and Pin 3 to a high-impedance voltmeter. Before use, the device should be powered-up and allowed to stabilize for one minute.

The calibration curve affords the most convenient method of flux measurement. Subject the device to the field in question. Read the output voltage from the voltmeter and find that value on the chart X axis. Locate the intersection of the output level with the calibration trace and read the corresponding flux density on the chart's Y axis.

The sensitivity coefficient can be used to calculate flux densities somewhat more precisely. First, determine the null output voltage of the device under 0 G or null field condition. Then, read the output of the device under an applied field condition by subjecting it to the flux in question. Magnetic flux density at the device may be calculated by:

$$B = \Delta V_{OUT(B)} - V_{OUT(0)} * 1000/S$$

where

$\Delta V_{OUT(B)}$ = Output voltage under applied field in volts.

$V_{OUT(0)}$ = Output null voltage in volts.

S = Sensitivity coefficient in mV/G.

B = Magnetic flux density at the device in gauss.

GLOSSARY

Active Area — The site of the Hall element on the encapsulated IC chip.

Air Gap — The distance from the face of the magnetic pole to the face of the sensor.

Ampere-turn (NI) — The mks unit of magnetomotive force.

Ampere-turns/meter (NI/m) — The mks unit of magnetizing force. One ampere turn per meter equals 79.6 oersteds.

Bipolar — A method of operating a Hall sensor using both north and south magnetic poles.

Coercive Force (H_c) — The demagnetizing force that must be applied to reduce the magnetic flux density in a magnetic material to zero. Measured in oersteds.

Concentrator — Any ferrous metal used to attract magnetic lines of force.

Gauss (G) — The CGS unit of magnetic flux density. Equivalent to one maxwell per square centimeter (Mx/cm^2). One gauss equals 10^{-4} tesla.

Gilbert — The CGS unit of magnetomotive force.

Head-On — A method by which the Hall sensor is actuated. The magnetic field is increased and decreased by moving the magnetic pole toward and away from the sensor face.

Maximum Energy Product (BH_{max}) — The highest product of B and H from the demagnetization curve of a magnetic material. Given in gauss-oersteds x 10^6 (MGOe).

Maxwell (Mx) — The CGS unit of total magnetic flux. One maxwell equals 10^{-8} webers.

Oersteds (Oe) — The CGS unit of magnetizing force. Equivalent to gilberts per centimeter (Gilberts/cm). One oersted equals 125.7 ampere-turns per meter.

Remanent Induction (B_d) — The magnetic induction that remains in a magnetic circuit after removal of an applied magnetomotive force. When there is no air gap in the magnetic circuit, remanent and residual induction are equal. With an air gap, remanence will be less than residual induction. Measured in gauss.

Residual Induction (B_r) — The flux density remaining in a closed magnetic circuit of magnetic material when the magnetizing force adequate to saturate the material is reduced to zero. Measured in gauss.

Slide-by — A method which a Hall sensor is actuated. The magnetic field is increased and decreased as a permanent magnet is moved laterally past the sensor face.

Tesla (T) — The mks unit of magnetic flux density. Equivalent to one weber per square meter (Wb/m^2). One tesla equals 10^4 gauss.

Toroid — A doughnut-shaped ring often composed of iron, steel or ferrite.

Total Effective Air Gap (TEAG) — The distance from the face of a magnetic pole to the active area of a Hall Effect sensor.

Unipolar — A method of operating a Hall sensor using a single magnetic pole, usually the south pole.

Vane — Any ferrous metal used to shunt a magnetic field away from the Hall sensor (at least 1.5 times the width of an associated magnet).

Window — An opening in a vane at least 1.5 times the width of an associated magnet.

SOURCES FOR FERRITE TOROIDS AND MAGNETS

As a convenience, some sources for ferrite toroids and magnets are listed below.
Addresses and telephone numbers are correct to the best of our knowledge at time of printing.

TOROID SUPPLIERS

J.W. Miller Co.
Division of Bell Industries
19070 Reyes Avenue
P.O. Box 5825
Rancho Dominguez, CA 90224
213/537-5200

Fair-Rite Products Corp.
P.O. Box J
Wallkill, NY 12589-0288
914/895-2055

Magnetics
900 East Butler Road
P.O. Box 391
Butler, PA 16001
412/282-8282

Dexter Magnetic Materials Division
10 Fortune Drive
Billerica, MA 01865
508/663-7500

Neosid Inc.
28 Main Street
Eatontown, NJ 07724
201/389-4411

Ferrox/Division of Amperex Corp.
5083 Kings Highway
Saugerties, NY 12477
914/246-2811

MAGNET SUPPLIERS

	Types
Arnold Engineering P.O. Box G Marengo, IL 60152 815/568-2000	Alnico, Ceramic, Multipole Ring
Bunting Magnetics Company 1165 Howard St. Elk Grove Village, IL 60007 312/593-2060	Alnico, Ceramic, Plastic
Ceramic Magnetics, Inc. 87 Fairfield Road Fairfield, NJ 07006 201/227-4222	Ceramic, Multipole Ring
Crucible Magnetics 101 Magnet Dr. Elizabethtown, NJ 42701 502/769-1333	Alnico, Rare Earth
Hitachi Magnetics 7800 Neff Road Edmore, MI 48829 517/427-5151	Alnico, Ceramic, Rare Earth
IG Technolog 405 Elm Street Valparaiso, IN 46383 219/462-3131	Alnico, Ceramic, Multipole Ring, Rare Earth
Ogallala Electronics P.O. Box 59 Ogallala, NE 69153 308/284-4093	Ceramic, Multipole Ring
Dexter Magnetic Materials Division 400 Karin Lane Hicksville, NY 11801 516/822-3311	Representatives of various manufacturers. Dexter Magnetic also does custom grinding.
Recoma, inc. 2 Stewart Place Fairfield, NJ 07006 201/575-6970	Rare Earth
Stackpole Carbon Co. Magnet Division 700 Elk Ave. Kane, PA 16735 814/837-7000	Ceramic, Flexible Plastic
TDK Corporation of America Head Office 1600 Feehanville Drive Mount Prospect, IL 60056 312/803-6100	Rare Earth
The Electrodyne Company 4188 Taylor Road Batavia, OH 45103 513/732-2822	Plastic
Xolox Corporation 6932 Gettysburg Pike Ft. Wayne, IN 46804 219/432-0661	Plastic, Multipole Ring
3-M Plastiform 3-M Center Industrial Electric Products Div. Building 225-4N St. Paul, MN 55144 Attn: James Fenwick 800/328-1373	Plastic
Magnaquench Div. of Gen. Motors 6435 S. Scatterfield Rd. Anderson, IN 46011 317/646-2763	Neodymium
Dynacast Co. 921 Albion Ave. Schaumburg, IL 60193 312/351-6100	

APPLICATIONS INFORMATION

THE HALL-EFFECT SENSOR

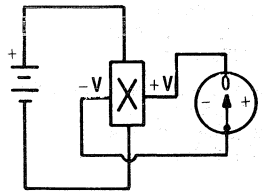

FIGURE 1

If no magnetic field is present, the voltage measured across the width of the semiconductor material of the Hall-effect sensor is zero.

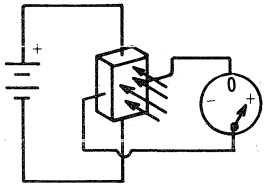

FIGURE 2

The output voltage of a Hall-effect sensor is directly proportional to the magnetic field present at right angles to the direction of current flow through the sensor.

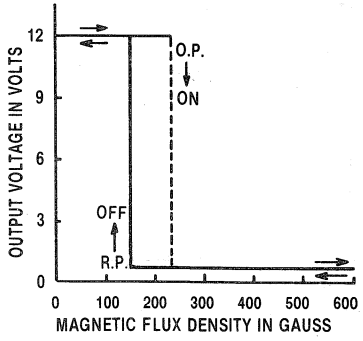

FIGURE 3

The transfer characteristic graph plots input on the horizontal axis vs output on the vertical axis. With no magnetic field present, the Hall-effect switch is off; as the field increases, the switch will turn on at a predesigned operating point. This particular device exhibits hysteresis of 90 gauss.

The basic Hall sensor is simply a small sheet of semiconductor material. A constant voltage source forces a constant bias current to flow in the semiconductor sheet. The output, a voltage measured across the width of the sheet, reads near zero if a magnetic field is not present (Figure 1).

If the biased Hall sensor is placed in a magnetic field oriented at right angles to the Hall current, the voltage output is in direct proportion to the strength of the magnetic field. This is the Hall effect, discovered by E. H. Hall in 1879 (Figure 2).

The basic Hall sensor is essentially a transducer that will respond with an output voltage if the applied magnetic field changes in any manner. Differences in the response of devices are generally related to tolerances and specifications, such as operate (turn on) and release (turn off) thresholds, as well as temperature range and temperature coefficients of these parameters. Also available are linear output sensors that differ in sensitivity or respond per gauss change.

A Hall sensor is activated by a magnetic field created by either electromagnets or permanent magnets. Magnetic fields have two important characteristics: magnitude and direction (or orientation). In the absence of any magnetic field, the most common Hall-effect digital switches are designed to be off (open circuit at output). They will turn on only if subjected to a magnetic field that has both sufficient strength and the correct polarity.

If the approach of the South pole of a magnet would cause switching action of a digital sensor, the approach of the North pole of a magnet would have no effect. In practice, a close approach by the South pole of a magnet will cause the output transistor to turn on.

The transfer characteristics graph (Figure 3) shows input vs output. The input variable, which is the strength of the activating magnetic field (magnetic flux density, measured in gauss), is plotted along the horizontal axis. The output variable, which is the digital (on, off) output from a Hall switch, is plotted along the vertical axis.

In the absence of any magnetic field (zero gauss), the Hall-effect switch is off and the output voltage equals the power supply (12 V). As the strength of the magnetic field increases, at some point (240 gauss in this case) the output transistor will turn on and the output voltage goes to zero. The output does not change even if the magnetic field's strength continues to increase.

The switch stays on until the magnetic field falls well below the 240 G operating point. This is a circuit design characteristic (hysteresis) that prevents oscillations. Our example uses a 90 gauss hysteresis (240-150), which will turn the device off at 150 gauss.

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FIGURES OF MERIT COMMONLY APPLIED TO MAGNETIC MATERIALS

- **Residual Induction (B_r) in Gauss.** How strong is the magnetic field? A magnet must have sufficient flux density to satisfy the Hall switch maximum operating point specification at the required air gap.
- **Coercive Force (H_c) in Oersteds.** How well will the magnet resist external demagnetizing forces? This property becomes important if the operating environment will subject the magnet to a strong demagnetizing field, such as might be encountered near the rotor of an A.C. motor. For such applications, a permanent magnet with this coercive force (ceramic, alnico-8, or, best of all, RE cobalt) is clearly indicated.
- **Maximum Energy Product [(B_d x H_d) Max x 10^6] in Gauss-Oersteds.** A strong magnet that is also very resistant to demagnetizing forces would have a high maximum energy product. Generally, the larger the energy product, the better, stronger, and more expensive the magnet.
- **Temperature Coefficient in Percent per Degree Celsius.** How much will the strength of the magnet change as the temperature changes?

All switches turn on at or below their maximum operating point flux density, and when the magnetic field is reduced, all devices turn off before the flux density drops below their minimum release point value. Additionally, each device has a minimum amount (typically, 20 gauss) hysteresis to ensure clean switching action. This hysteresis ensures that even if mechanical vibration or electrical noise is present, the switch output is fast, clean, and occurs only once per threshold crossing.

Linear Hall-effect sensors differ from digital Hall-effect sensors with respect to the output response from the sensor. The digital sensor has an off/on or high/low output; the linear sensor has an output proportional to the magnetic field subjected to the "active area." Hall-effect linear sensors are used primarily to sense relatively small changes in magnetic fields, changes too small to operate a Hall-effect digital switch.

The exact magnetic flux density values required to activate Hall sensors differ for several reasons, including design criteria and manufacturing tolerances. Extremes in temperature also affect the response characteristics of the sensors.

For each device type, worst-case magnetic specifications can be set out for the user by a Hall-effect sensor marketing or applications engineer, if it has been determined that a catalogue item will not meet required tolerances.

APPLICATIONS

With an understanding of how Hall-effect sensors work, it is possible to build devices around them. The physical aspects of their characteristics form the basis of Hall device applications.

Analysis. The field created by a magnet must be compatible with the characteristics of the Hall-effect device it is expected to operate. Measure the strength of the magnetic field, which is greatest at the magnet's pole face, with a gaussmeter or a calibrated linear Hall sensor. Then plot a graph of field strength (magnetic flux density) vs distance of the magnet from the device along the intended line of travel of the magnet. Then, by using the Hall device specifications sensitivity of mV/gauss for a linear device, or operate and release points in gauss for a digital device) one can find the critical distances for a particular magnet and type of motion. These field strength plots are not linear, and the shape of the plot depends greatly upon magnet shape, magnetic circuit (concentrators), and path traveled.

Total Effective Air Gap. Hall-effect switches are offered in many different packages, such as epoxy three-pin SIPs, ceramic substrate mounted chips, ceramic three-pin SIPs, and surface mount packages. The most critical difference between packages is the distance from the face of the package to the surface of the Hall cell: the active area depth, which effectively adds to the total effective air gap.

The total effective air gap (TEAG) is the sum of the active area depth and the distance between the package surface and the magnet's surface. For Hall device applications, the TEAG should be as small as possible, consistent with the limitations of the activating mechanical system. This will ensure that the magnetic flux will always be great

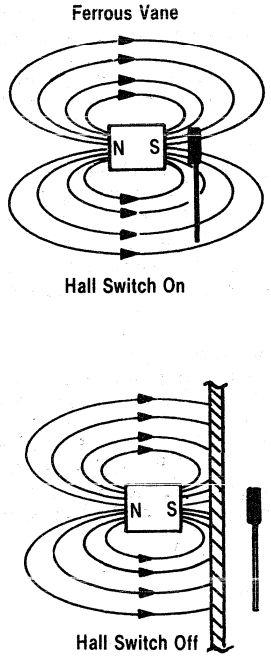

FIGURE 4

The ferromagnetic vane moves between the activating magnet and the Hall-effect switch shunting the flux field from the switch. These assemblies can be used for precision switching over large temperature ranges.

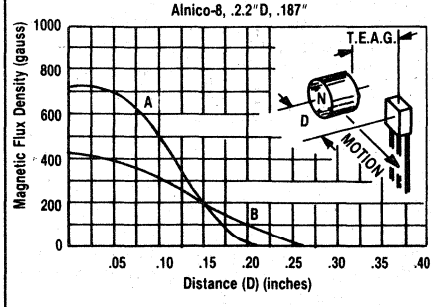

FIGURE 5

Hall devices must always switch on/off at the same point relative to the magnet. The effect of a change in flux density on switching distance is shown.

enough to switch the device. Remember, magnetic flux decreases very sharply as the total effective air gap increases.

Modes of Operation. There are many ways to operate a Hall sensor. For example, with a simple bar or rod magnet there are two possible paths for the magnet to travel—head-on and slide-by. In the head-on mode, the magnetic pole moves along a perpendicular path straight at the active face of the Hall device. The head-on mode is simple, works well, and is relatively insensitive to lateral motion; however, if the mechanism moving the magnet overshoots the mark, the sensor package could be damaged.

A second possible path is to move the magnet in from the side of the hall device in the slide-by mode of operation. The slide-by mode is commonly used to avoid contact with the sensor package. The use of strong magnets or ferrous flux concentrators in well-designed slide-by magnetic circuits allows better sensing precision with a shorter travel path than the head-on mode.

Magnet manufacturers generally can provide head-on flux density curves for their magnets, but they often do not characterize magnets for slide-by operation, possibly because different air gap choices lead to an infinite number of these curves. Once a TEAG is chosen, however, the head-on magnet curves can be used to find the peak flux density (a single point) for slide-by applications by noting the value of magnetic flux at the chosen TEAG.

A third mode of operation keeps the Hall-effect sensor and magnet a fixed distance from one another and switches the sensor with a movable ferromagnetic vane. The Hall device and magnet can be molded together as a unit in a single rigid assembly, separated by an air gap. This eliminates alignment problems and produces an extremely rugged switching assembly.

The Hall device is held in the on state by the activating magnet. Placing the vane between the magnet and the Hall device (Figure 4) forms a magnetic shunt that distorts the flux field away from the Hall device. The vane can be made in many configurations to repeatedly sense position within ±0.002 in. over a 125°C temperature range.

The ferrous vane or vanes that interrupt the flux could have linear motion or rotational motion (as for a shaft encoder). Ferrous vane assemblies, due to the steep flux density/distance curves that can be achieved, are often used where precision switching over a large temperature range is required.

Steep Slopes and High Flux Densities. For linear Hall devices, greater flux changes for a given displacement give greater outputs, clearly an advantage because the voltage output of the sensor will be much greater, reducing the possibility of instruments picking up electrical noise. The same property is desirable for digital Hall devices, but the reasons are more subtle. To achieve consistent switching action in a given application, the Hall device must always switch on and off at the same positions relative to the magnet.

Consider, for example, the flux density curves of the two different magnet configurations in Figure 5. With an operating point flux density of 200 gauss, a digital Hall-effect device would turn on at a distance of

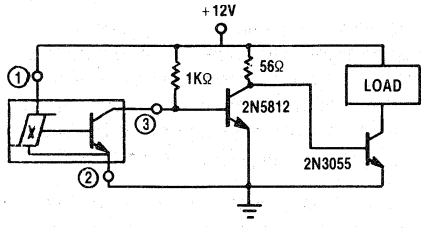

FIGURE 6

This circuit could be used if a load required a current of 4 A to switch.

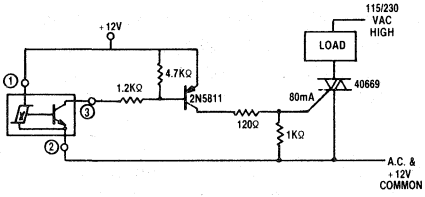

FIGURE 7

This circuit could be used to switch a 115 or 230 VAC load.

approximately 0.14 in. from either magnet. If manufacturing tolerance or temperature effects shifted the operating point of the sensor to 300 gauss, notice that in the curve for magnet "A" (steep slope) there is very little change in the distance at which switching occurs, while in the case of the curve of magnet "B", the change is considerable. The release point would be affected in much the same way.

The basic principles illustrated in this example can be modified to include mechanism and device specification tolerances and used for worst-case design analysis.

ELECTRICAL INTERFACE FOR DIGITAL HALL DEVICES

A typical application for a Hall-effect sensor is interfacing the sensor signal to a microporocessor. The output of the Hall element is quite small; therefore, Hall ICs have been developed that contain a voltage regulator to allow a wide range of operating voltages, a high-quality DC amplifier to boost the element signal to a more easily used signal, a Schmitt trigger threshold detector to produce digital logic, and output stages for universal interfaces capable of current sinking or sourcing. The output of the Hall-effect digital switch can be either linear (proportional to the magnetic field present) or clean-switching (no bounce) digital logic. Energy consumption is very low, and frequency responses are well over 100 kHz.

The output stage of a digital switch is simply an open collector npn transistor switch, and the rules for use are the same as those for any similar switching transistor. When the transistor is off, there is a small leakage current (typically a few nanoamps) that usually can be ignored and a maximum (breakdown) voltage specification that must not be exceeded. When the transistor is on, the device output is shorted to the circuit common, and the current flowing through the switch must be externally limited to less than the maximum specified value to prevent damage (usually 20 mA).

Hall devices switch very rapidly; typical rise and fall times are in the 400 nano-second range. This is rarely significant, since switching times are almost universally controlled by the much slower mechanical parts of the device.

Interfacing with digital logic integrated circuits usually requires only an appropriate power supply and pull-up resistor.

Loads that require sinking currents up to 20 mA can be driven directly by a Hall switch. A good example is a light emitting diode (LED) indicator that requires only a resistor to limit current to an appropriate value.

Sinking more current than 20 mA requires a current amplifier. For example, if a certain load to be switched requires 4 amperes and must turn on when the activating magnet approaches, the circuit shown in Figure 6 could be used. To turn on a 115 or 230 VAC load, consider Figure 7. Note, however, that the +12 V supply common is connected to the low side of the AC line, and in the event of a mixup, the Hall switch and associated low voltage circuitry would be 115 volts above ground.

THE HALL-EFFECT·SENSOR

Due to the magnetic field around any current-carrying conductor, Hall-effect devices can be used to measure and limit current by converting this magnetic field to an electrical signal. The sensor response ranges from DC to the kHz range, and the conductor need not be interrupted. In low current applications, the magnetic field about a conductor is not normally intense enough to operate a Hall-effect digital switch; therefore, it would be best to use a toroid or closed magnetic circuit to increase the flux density.

Hall-effect linear sensors are used primarily to sense relatively small changes in magnetic fields—changes that are too small to operate a Hall-effect switching device. They are customarily capacitively coupled to an amplifier that boosts the output to a higher level (Figure 7).

As motion detectors, gear tooth sensors, and proximity detectors, linear Hall-effect sensors produce an electrical output that is a magnetically driven mirror of mechanical events. As sensitive monitors of electromagnets, they can effectively measure a system's performance with negligible system loading while producing isolation from contaminated and electrically noisy environments.

Hall-effect sensors, both digital and linear, are used in the commutation of brushless DC motors, speed sensors, shaft encoders, current limiters and monitors, position sensors, and gear tooth sensors. Recent technology breakthroughs in Hall-effect devices have made available sensors for temperature ranges as high as 170°C. These sensors have been integrated into a vast array of innovative high-technology applications where reliability, efficiency, and cost competitiveness are a must.

MAGNETIC MATERIALS MOST COMMONLY USED

- **Rare Earth—Cobalt.** An alloy of rare earth metal, such as samarium, with cobalt (abbreviated RE cobalt). These magnets are the best in all categories but are also the most expensive. Too hard for machining, these magnets must be ground, if shaping is necessary. Maximum energy product, perhaps the best single measure of magnet quality, is approximately 16 x 10^6.

- **Alnico.** A class of alloys containing aluminum, nickel, cobalt, iron, and additives, which can be varied to give a wide range of properties. The magnets are strong and fairly expensive, but less so than RE cobalt. Alnico magnets can be cast or sintered by pressing metal powders into a die and heating. Sintered alnico is well suited to mass production of small, intricately shaped magnets, has a more uniform flux density, and is mechanically superior, but cast alnico magnets are generally magnetically stronger. The nonoriented or isotropic alnico alloys (alnico-1, alnico-2, alnico-3, alnico-4) are lessexpensive and magnetically weaker than the oriented alloys (alnico-5, alnico-6...alnico-9). Alnico is too hard and brittle to be shaped except by grinding. Maximum energy products range from 1.3 to 10 x 10^6.

- **Ceramic.** These magnets contain barium or strontium (or another element from that group) ferrite in a matrix of ceramic material that is compacted and sintered. They are poor conductors of heat and electricity, chemically inert, and have high values of coercive force. As with alnico, ceramic magnets can be fabricated with partial or complete orientation for additional magnetic strength. Less expensive than alnico, they are also too hard and brittle to shape except by grinding. Maximum energy products range from 1 to 1.3 x 10^6.

- **Cunife.** A ductile copper base alloy with nickel and iron, cunife can be stamped, swaged, drawn, or rolled into final stage. Maximum energy product is approximately 1.4 x 10^6.

- **Iron-Chromium.** These magnets have magnetic properties similar to alnico-5 but are soft enough to undergo machining operations before the final aging treatment hardens them. Maximum energy product is approximately 5.25 x 10^6.

- **Plastic and Rubber.** These magnets consist of barium and strontium ferrite in a plastic matrix material. They are very inexpensive and can be formed in numerous ways, including stamping, molding, and machining, depending on the particular matrix material. Since synthetic rubber is a plastic, the distinction between the two materials is not very precise. If a plastic magnet is flexible like rubber, it is generally called a rubber magnet. Maximum energy products range from 0.2 to 1.2 x 10^6.

APPLICATIONS INFORMATION

LIGHT SENSING USING OPTICAL INTEGRATED CIRCUITS

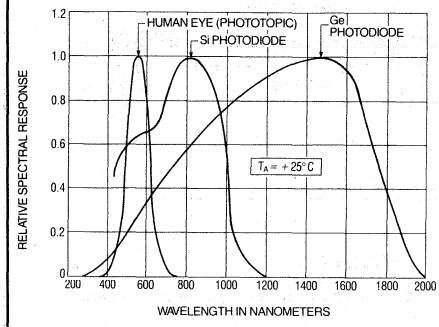

FIGURE 1

The CIE spectral response curve is overlaid on the spectral responsivity curves of silicon and germanium (1, 3).

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Light sensing has traditionally been used for a variety of transducing applications including absolute light measurement position encoding, rotary speed measurement, optical communications, and electrical isolation. Most of these applications use light emitters and detectors along with additional driving-sensing circuitry to enable the sensing of electrical or mechanical stimuli.

Light emitters come in several varieties: incandescent lamps (or light bulbs), light-emitting diodes (LEDs), and lasers. In most transducer applications, incandescent lamps are not used due to their slow response to electrical stimuli and the lack of focused light emission. LEDs are more popular because they respond to fast electrical impulses, emit focused light of a narrow bandwidth, and the intensity of emitted light can easily be changed by changing the current through the device. However, the maximum intensity of the light emitted by LEDs is severely limited. This problem has been overcome by lasers, which have more power than LEDs, but laser usage is constrained by the need for expensive driving electronics and the inability to easily change the intensity of the emitted light. Therefore, most electrical transducing applications use LEDs.

While there are several types of light detectors, the most popular detectors are semiconductor-based devices, which fall into two major categories: photoconductors and photodetectors. Photoconductors are devices whose resistance decreases with incident light. Cadmium sulfide and cadmium selenide are examples of photoconductors that are sensitive to visible light. These devices are relatively large, typically ranging in diameter from 5 to 25 mm.

Typical junction photodetectors, such as photodiodes, Schottky photodiodes, phototransistors, and avalanche photodetectors, work under the principle of carrier transport across material interface junctions. Photodiodes respond to optical radiation by generating electron-hole pairs, which are then transported across a p-n junction. Carrier transport in Schottky photodiodes takes place across a metal-semiconductor junction. While both types of photodiodes exhibit a high degree of linearity, Schottky devices have lower junction capacitance and are, thus, faster than p-n junction photodiodes. In phototransistors, incident light on the base of a transistor controls the collector current. These devices are typically used in switching and modulation applications where high gain and fast response are more important than linearity. Avalanche photodetectors are reverse biased junction detectors wherein the optically generated carriers are accelerated so as to further generate carriers by impact. These devices are typically used in high-speed communication applications.

Since several of the junction photodetectors mentioned can be fabricated from silicon, it is possible to incorporate the receiver circuitry with the photodetector to create a low-cost solution to light detection problems. (The processing of the optical signals is performed using decoding receiver circuitry.) Incorporating a preamplifier with the photodetector also permits smaller photodetectors, resulting in lower

junction capacitance and smaller device size. Extremely sensitive optical detectors may be constructed since lower light currents can now be amplified without external noise coupling. Integrated circuit optical sensors typically use silicon-based photodiodes since they are easy to fabricate and are compatible with the IC process.

PHOTODIODES

Photodiodes are reverse biased p-n junctions that respond to optical radiation. Photons captured close to the p-n junction release electrons into the conduction band which are swept across the junction. This electron flow represents the photocurrent (or light current) of the diode.

Light current is greatly dependent on the spectrum of the incident light. The spectral response of a photodiode is determined by the material from which it is fabricated and the diode junction depth. The response of the long wavelength of the photodiode is controlled by the band-gap energy of the material, that is, the energy needed to release an electron from the valence band to the conduction band. The energy of an incident photon is given by:

$$E = hv$$

where:

h = Planck's constant

$v = c/\lambda$ is the frequency of light

c = velocity of light

The electron will be released only when:

$$E \geq E_g$$

where E_g is the energy gap of the semiconductor defined in electronvolts, or:

$$hv \geq E_g$$

The longest wavelength absorbed is given by:

$$\lambda = E_g/hc$$

The short wavelength response of the photodiode is determined by the depth of the junction from the surface. Shorter wavelengths are absorbed near the surface, generating electron-hole pairs. These pairs recombine before they reach the p-n junction, so do not result in photocurrent. Deep junction photodiodes have low responses to short wavelength radiation.

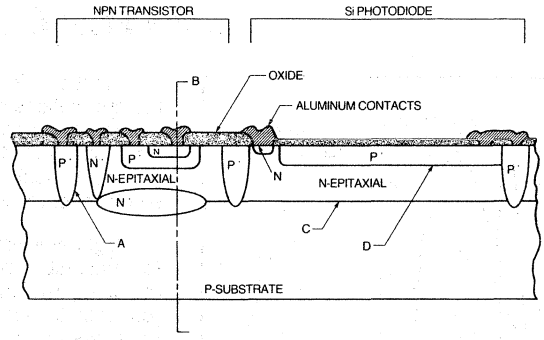


FIGURE 2

A cross section of silicon IC shows a typical npn transistor and a photodiode (drawing is not to scale).

These processes result in spectral responsivity curves that are nonuniform with wavelength. Figure 1 shows the spectral responsivity curves of Si and Ge, along with the CIE photopic response curves. The peak response of Ge is at 1.5 µm, while Si is at 0.85 µm. This corresponds to a band-gap energy of 1.1 eV for Si and 0.67 eV for Ge. The drop in responsivity at low wavelengths is due to lower efficiencies for a deep junction. Note the low photodiode spectral response in the region of the photopic curve.

Since the diode is reverse biased, ideally no other current should flow; however, fabrication impurities cause leakage current that flows even when no light is incident on the junction. This leakage current (also known as dark current) is a function of reverse bias, diode junction size, and ambient temperature. Large dark current values limit the signal-to-noise ratio of the photodiode and place constraints on the maximum operational temperature of the receiver circuitry. Dark current is given by:

$$I_{Dark} = -I_0 \left(e^{(V/V_t)} - 1\right)$$

where:

I_0 = reverse saturation current

V = reverse bias voltage

$V_t = kT/q$ (k = Boltzmann's constant, q = electron charge, T = absolute temperature)

From this equation, it can be seen that for no incident light, the dark current is dependent on the applied voltage and the absolute temperature. It can also be noted that theoretically, dark current goes to zero for no applied voltage and, hence, loses its temperature dependence.

LIGHT SENSING USING OPTICAL INTEGRATED CIRCUITS

LIGHT MEASUREMENT

Due to the nonuniform response of a photodiode to the spectrum of incident light, photodiode sensitivity is generally specified in radiometric units as the power of light incident ($\mu A/\mu W/cm^2$) for a given wavelength. Absolute light levels are specified in power incident ($\mu W/cm^2$) for a given light bandwidth. Since it is difficult to generate a light source of a single wavelength, the light is assumed to have the spectral output of a specified LED, e.g., an AlGaAs LED is normally used with a silicon photodiode. Other optical units, such as foot-candles and lumens, are not appropriate since they assume a photopic spectral response.

INTEGRATED CIRCUIT OPTICAL SENSORS

Traditionally, photodiodes have been used in conjunction with hybrid amplifier circuitry to perform certain signal processing applications. These operations may include light current amplification, light threshold detection, and light demodulation. Building photodiodes out of silicon has given the IC designer the ability to fabricate both the hybrid circuitry and the photodiode on the same silicon substrate, thus eliminating the need for additional circuitry.

Figure 2 shows the cross section of a silicon IC containing an npn transistor and a photodiode fabricated using a bipolar integrated circuit process. Most bipolar processes are fabricated by growing an n-type epitaxial layer on a p-type substrate. Individual devices are separated into epitaxial pockets by forming a reverse biased isolation-epitaxial junction A (p^+ -n) at the pocket walls. Impurities are then diffused into these epitaxial pockets to create devices (npn and pnp transistors, resistors).

The npn transistor shown in Figure 2 is manufactured using the above techniques. The collector of the transistor is the lightly doped epitaxial layer. Diffused into this layer is a heavily doped p^+ layer that forms the base of the transistor. The emitter is the strongly doped n^+ layer. The npn junctions are formed along the vertical axis B. Aluminum contacts are directly made to the emitter and base. Contact to the collector is made by the aluminum through a low-resistance n^+ plug and buried layer.

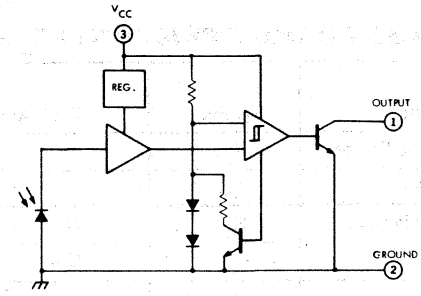


FIGURE 3

A functional block diagram of the ULN3330 IC optical receiver is shown.

The substrate-epitaxial interface C forms a p-n junction which, when reverse biased, can be used as a photodiode. P-type impurities in the form of base diffusion form an additional junction D, across which optically generated carriers may be transferred. The photodiode is normally the largest single component on the IC. Photodiodes can vary in size from 20 by 20 mils to 30 by 30 mils.

TYPICAL OPTICAL RECEIVER

Using these techniques, an IC designer can fabricate a high-quality, low-noise receiver that can be incorporated onto a single silicon substrate. There are two basic types of integrated sensors: linear and digital. The output of a linear sensor is proportional to the incident light level. This device is generally factory calibrated for repeatable sensitivity. A digital sensor is a level detector that switches on at a fixed light level. The device incorporates positive feedback circuitry that induces a hysteresis that inhibits release until the output moves much lower than the previous trip point.

Figure 3 describes a typical digital optical sensor, the ULN3330. This device has an on-chip ground-referenced photodiode whose photocurrent is fed into a current amplifier. This amplified current is then converted into a voltage level by dropping it through an adjustable load resistor. A comparator checks this voltage level and switches on at a predetermined threshold level. For noise immunity, internal feedback disables switching until the light level falls approximately 12 percent below the switching threshold. The output interface allows switching of TTL and CMOS devices, as well as the ability to drive low-current relays.

Circuit designers benefit from the use of IC technology in the design of optoelectronic sensor circuits. Low photodiode currents on the order of a few hundred nanoamperes can be amplified without worrying about external noise sources; hence, smaller diodes can be used. Matching accuracy of transistors and resistors helps create high-quality, low-offset amplifiers. Amplifier and photodiode characteristics can be internally compensated using the repeatable temperature characteristics of IC resistors and diode junctions, while switching thresholds can be adjusted at wafer test by trimming on-chip resistors. In addition, the reliability of these devices may be much greater than for hybrid assemblies.

TABLE I

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 6.0 V, λ = 880 nm

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}		4.0	6.0	15	V
Supply Current	I_{CC}		—	4.0	8.0	mA
Light Threshold Level	E_{ON}	Output ON	45	55	65	μW/cm²
	E_{OFF}	Output OFF	—	62	—	μW/cm²
Hysteresis	ΔE	$(E_{OFF} - E_{ON})/E_{OFF}$	10	12	14	%
Output ON Voltage	V_{OUT}	I_{OUT} = 15 mA	—	300	500	mV
		I_{OUT} = 25 mA	—	500	800	mV
Output OFF Current	I_{OUT}	V_{OUT} = 15 V	—	—	1.0	μA
Output Fall Time	t_f	90% to 10%	—	200	500	ns
Output Rise Time	t_r	10% to 90%	—	200	500	ns

OPTICAL SENSOR APPLICATIONS

Optical ICs do not, however, replace careful engineering review on the part of the optical assembly designer. Several factors contribute to a successful optical system design. These factors include light threshold levels, ambient light interference, output load conditions, and voltage supply.

Table I shows a typical specification table for a digital output optical sensor (in this case, the ULN3330). Defined in this table are the supply voltage ranges, supply current limits, and sink current capabilities. An important specification is the light threshold level. The ULN3330 is a highly sensitive device, with light threshold levels under 65 μW/cm² and a hysteresis of 10-14 percent. When designing transducing assemblies using a sensitive optical receiver, ambient light levels may provide a significant and unwanted noise contribution. In addition, the light emitted by a commercial LED may vary a great deal for a given LED driver current. If optical measurements are not carefully taken, high ambient light levels (noise) may keep the detector always switched, while low LED light outputs (signal) may never switch the detector.

When measuring light levels it is important to use a linear receiver whose photodiode is of the same material and is roughly the same area as that of the digital sensor. If a different material is used, the difference in spectral responsivity will result in inaccurate readings. If the linear receiver is much larger in area, then optical patterns on the receiver may not be the same as those on the digital sensor, thereby creating faulty readings. When using the ULN3330 or any other optical IC, the ambient light level can be accurately measured using the ULN3311/12.

By carefully following the device specification table and by making the appropriate optical measurements, optical integrated circuit sensors can be used in a variety of detection applications. The availability of vast amounts of circuitry in a small package provides optical system designers with a powerful tool.

LIGHT SENSING USING OPTICAL INTEGRATED CIRCUITS

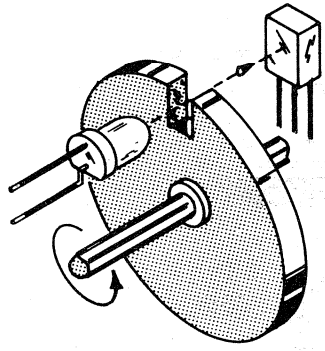
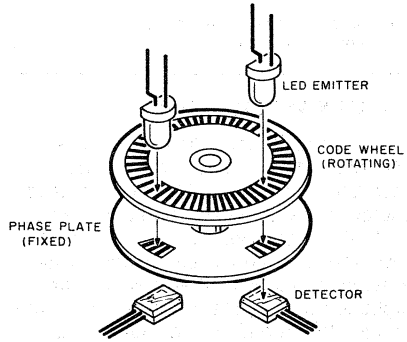


FIGURE 4

Shown is a commonly used speed-sensing assembly. The light field between the emitter-detector pair is interrupted by the rotating code wheel.



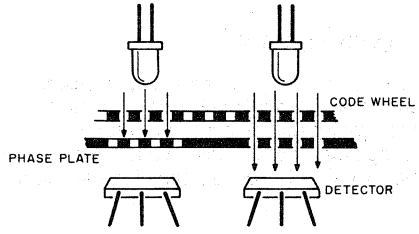


FIGURE 5A and B

This high-resolution rotary encoder shows the fixed phase plate along with the rotating code wheel. The two photodetectors are placed such that a light field on one device corresponds to a dark field on the other.

ABSOLUTE LIGHT MEASUREMENTS

The ULN3311/12 have been used in several applications for the measurement of light such as automatic brightness control for CRTs, feedback for photocopiers, and light measurement for cameras. These linear optical ICs are preferred over other photodetectors because of the factory calibration of their sensitivity.

Absolute light sensing is also used for switching street, emergency, and automotive lighting. In these applications, the light level is measured using a photosensor (usually a cadmium sulfide photoconductor) and the switching assembly is designed so as to trip when the light falls below a specified value. Photoconductors are highly sensitive to ambient temperature, making the trip points difficult to stabilize over temperature extremes. The same function can be accomplished using the internally compensated ULN3390. This device is a highly sensitive digital output device that trips and releases at 10 $\mu W/cm^2$ and 20 $\mu W/cm^2$ respectively. Internal hysteresis provides immunity to small light variations (due, for example, to changing cloud cover), thus lowering the chances of oscillations in the switching circuitry.

OPTOCOUPLERS-OPTOISOLATORS

Emitter-detector pairs are linked together through an optical waveguide to couple electrical signals for communications and isolation applications. In communication applications, the waveguide is generally a fiber-optic cable. Low-speed communications problems may be solved using digital ICs. Higher speed applications demand fast responding avalanche photodiodes and hybrid receiver circuitry.

Optical isolation is accomplished by inserting an emitter-detector assembly between sensitive electronics and controller switching circuitry. The waveguide is the package itself. This isolates electrical processes on the receiver end from those on the emitter end—a technique that is used to protect expensive circuitry from the effects of shorts or faults on the controller switching lines.

ROTARY ENCODING

Speed sensing and rotary position encoding are best done using optical emitter-detector assemblies. Figure 4 shows a common assembly used in speed measurement applications. Here, the rotating wheel interrupts the light field, causing the detector to switch, generating a pulse for each slot in the wheel. In this assembly, the number of pulses per revolution is limited by the emitter beam width as well as the detector element size. Typical interrupter widths of 200-300 mils are used.

A newer technique used in high-resolution rotary encoding is illustrated in Figure 5. Interrupting the light path are a rotating code wheel and a fixed phase plate. The code wheel has a fixed number of apertures (as many as 256) around its circumference. The fixed phase plate also has a number of apertures of the same size as those in the code wheel and is fixed directly above the light sensing photodetector, as shown in Figure 5a. Rotation of the code wheel creates alternate light and dark periods on the surface of the detector. Using this technique, high-resolution measurements have been obtained by sensing code wheel apertures of 10 to 20 mils. In addition, the phase plate can be coded to allow placement of another photodetector IC that is 90 degrees out of phase with the first detector, as shown in Figure 5b. This allows the sensing of both position of the wheel and direction of rotation.

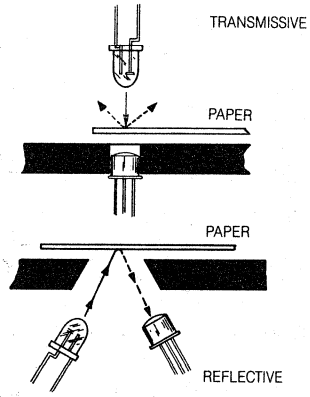


FIGURE 6

Sheet detector configurations using transmissive and reflective modes of operation are shown.

MISCELLANEOUS APPLICATIONS

Optical sensors are used in several other applications. Some smoke detectors use sensitive optical detectors to ascertain the presence of smoke in the assembly. Emitter-detector pairs are used as sheet edge detectors in photocopiers for detection of paper size. Detection can be done in both the transmissive and reflective modes, as shown in Figure 6. Fluid level measurement systems use emitter-detector pairs that cause the detector to switch when fluid in a tube interrupts the beam path. Burglar alarm systems use infrared emitter-detector pairs that switch when the beam path is interrupted by an object. The same strategy can also be used to generate signals for counting moving objects such as bottles and cans on a moving assembly line.

CONCLUSION

Optical integrated circuits give the designer the ability to design complex transducing functions using a small number of integrated components at a low cost. The small package sizes allow for use in a large number of size-critical applications. Clearly, in many measuring and sensing applications, optical integrated circuit-based transducers are the sensors of choice.

REFERENCES

1. Budde, W. "Optical Radiation Measurements," *Physical Detectors of Optical Radiation,* v. 4, Academic Press, p. 239.

2. Streetman, Ben. *Solid State Electronic Devices,* 2nd ed., Prentice-Hall, p. 211-212.

3. Silicon and CIE, Photodiode spectral response from Sprague Integrated Circuit Bulletin 27480B, p. 3.

GLOSSARY OF TERMS

Band-gap energy (E_g): The energy difference between energy levels of the conduction band and the valence band. It is also the minimum energy required to free an electron from the valence band to the conduction band.

CIE: Acronym for the Commission Internationale de l'Eclairage. The International Commission on Illumination has been responsible for setting several lighting standards.

Conduction band: The band of energy levels occupied by a valence electron when it is liberated from an atom. Electrical conduction in a semiconductor crystal takes place through the transport of electrons in the conduction band.

Epitaxial material: A material whose atoms are arranged in single crystal fashion upon a crystalline substrate so that its lattice structure duplicates that of the substrate.

Hysteresis: To provide noise immunity, the switch points of a comparator are altered using positive feedback so that the voltage required to switch the comparator output low (operate point voltage) is greater than the voltage required to switch the output high (release point voltage). The difference between these switch points is a measure of the hysteresis of the comparator.

n^+-type material: Heavily doped n-type material, formed by introducing donor impurities into a silicon substrate. Conduction takes place by the movement of free electrons.

p^+-type material: Heavily doped p-type material, formed by introducing acceptor impurities into a silicon substrate. Conduction takes place by the movement of holes.

p-n junction: Material interface between positively doped (p-type) and negatively doped (n-type) semiconductor. These junctions are fundamental to the performance of switching, rectification, and amplification functions in electronic devices and circuits.

Photometric units: Radiometric quantities spectrally weighted by the spectral response of the human eye (also called the photopic response). Typical units of illuminance are foot-candles or lumens.

Photopic response: Spectral response of vision mediated essentially or exclusively by the cones in the human eye. Standards for this response have been laid down by the International Commission on Illumination (CIE).

Valence band: The electrons in the outermost shell of an atom (valence electrons) occupy a band of energy levels called the valence band. Electrons in this band do not participate in electrical conduction in silicon.

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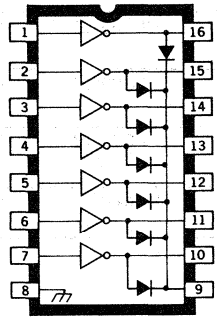
2001 THRU 2025

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

ULS20XXH/R



Dwg. No. A-9594

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
(ULS200X*, ULS201X*) . . . . . **50 V**
(ULS202X*) . . . . . **95 V**
Input Voltage, V_{IN}
(ULS20X2*, X3*, X4*) . . . . . **30 V**
(ULS20X5*) . . . . . **15 V**
Peak Output Current, I_{OUT}
(ULS200X*, ULS202X*) . . . . . **500 mA**
(ULS201X*) . . . . . **600 mA**
Ground Terminal Current, I_{GND} . . . . . **3.0 A**
Continuous Input Current, I_{IN} . . . . . **25 mA**
Power Dissipation, P_D
(one Darlington pair) . . . . . **1.0 W**
(total package) . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

X = digit to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown.

*Complete part number includes a final letter to indicate package.

Comprised of seven silicon NPN Darlington power drivers on a common monolithic substrate, Series ULS2000EK, ULS2000H, and ULS2000R arrays drive relays, solenoids, magnetic print hammers, lamps, and other devices in high-reliability military or aerospace applications with up to 3 A of output current per package.

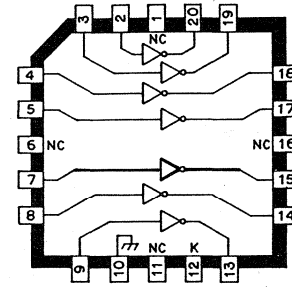
These devices are screened to MIL-STD-883, Class B and are supplied in a leadless ceramic chip carrier with Kovar lid (suffix 'EK'), the popular ceramic/metal side-brazed 16-pin hermetic package (suffix 'H'), or ceramic/glass cer-DIP hermetic package (suffix 'R'). All package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of -55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

The 35 integrated circuits described here permit the circuit designer to select the optimal device for any application. In addition to the three package styles (note that the ceramic chip carrier is available only for the ULS2001EK through ULS2005EK devices), there are five input characteristics, two output-voltage ratings, and two output-current ratings. The appropriate part for specific applications can be determined from the Device Part Number Designation chart. All units have open-collector outputs and on-chip diodes for inductive-load transient suppression .

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B
- -55°C to +125°C Temperature Range

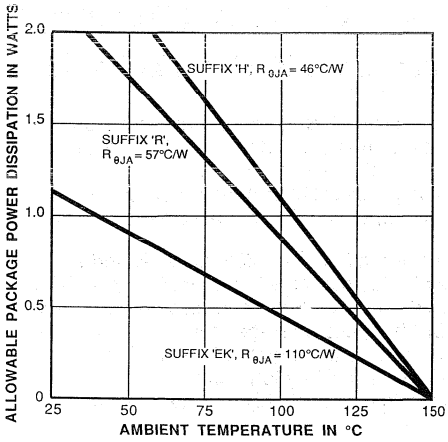
ULS200XEK



Dwg. No. A-14,378

Always order by complete part number, e.g., **ULS2013H883** . See matrix on next page.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS



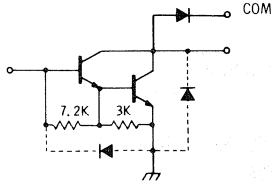
Dwg. GM-004

DEVICE PART NUMBER DESIGNATION

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic		**Part Number**	
General Purpose PMOS, CMOS	ULS2001*	ULS2011*	ULS2021*
14-25 V PMOS	ULS2002*	ULS2012*	ULS2022*
5 V TTL, CMOS	ULS2003*	ULS2013*	ULS2023*
6-15 V CMOS, PMOS	ULS2004*	ULS2014*	ULS2024*
High-Output TTL	ULS2005*	ULS2015*	ULS2025*

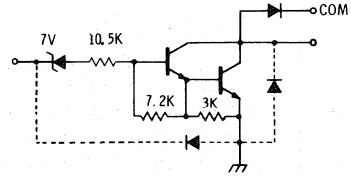
PARTIAL SCHEMATICS

ULS20X1*
(Each Driver)



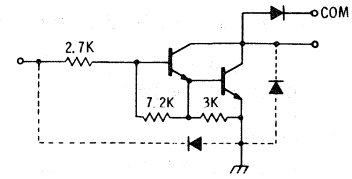
Dwg. No A-9595

ULS20X2*
(Each Driver)



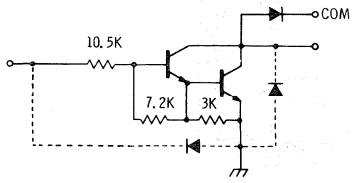
Dwg. No A-9650

ULS20X3*
(Each Driver)



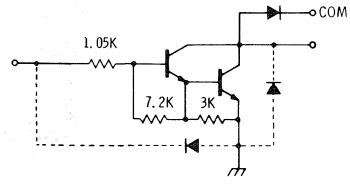
Dwg. No. A-9651

ULS20X4*
(Each Driver)



Dwg. No. A-9898A

ULS20X5*
(Each Driver)



Dwg. No. A-10,228

** Complete part number includes a final letter to indicate package (EK = leadless ceramic chip carrier, H = ceramic/metal side-brazed, R = cermic/glass cer-DIP.*

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

ULS2001EK/H/R THRU ULS2005EK/H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS2002*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2004*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS2002*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2003*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2004*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2005*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2002*	-55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	13	V
		ULS2003*	-55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V

*Complete part number includes a final letter to indicate package
(EK = leadless/ceramic chip carrier, H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

Continued next page...

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2001EK/H/R THRU ULS2005EK/H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2004*	-55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS2005*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2001*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (EK = leadless ceramic chip carrier, H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2011H/R THRU ULS2015H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS2012*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2014*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 500 mA, I_B = 1100 µA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 µA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+125°C	I_C = 500 mA†, I_B = 600 µA	2	—	1.8	2.1	V
				I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS2012*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2013*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2014*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2015*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2012*	-55°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	23.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	17	V
		ULS2013*	-55°C	V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	6.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	3.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

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NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2011H/R THRU ULS2015H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2014*	-55°C	V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
			+125°C	V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	9.5	V
		ULS2015*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	3.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2011*	-55°C	V_{CE} = 2.0 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 500 mA	2	900	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V
				I_F = 500 mA†	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2021H/R THRU ULS2025H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	µA
		ULS2022*		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2024*	+25°C	V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	µA
			+125°C	V_{CE} = 95 V, V_{IN} = 0.5 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS2022*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2023*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2024*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2025*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	20	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2022*	-55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	13	V
		ULS2023*	-55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

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NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2021H/R THRU ULS2025H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2024*	-55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS2025*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2021*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate pachage (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

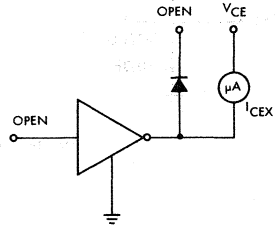
NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

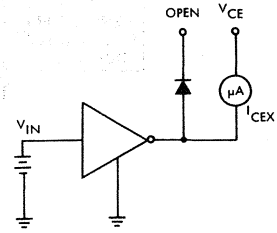
TEST FIGURES

FIGURE 1A



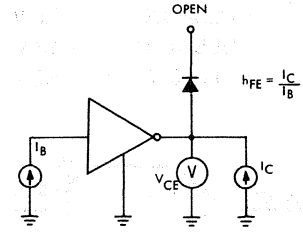
Dwg. No. A.-9729A

FIGURE 1B



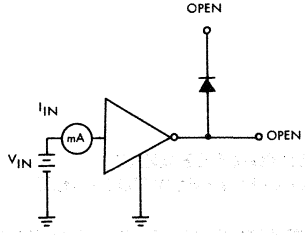
Dwg. No. A-9730A

FIGURE 2



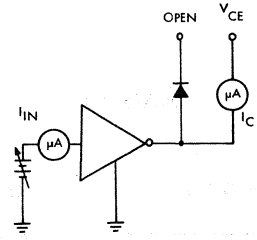
Dwg. No. A-9731

FIGURE 3



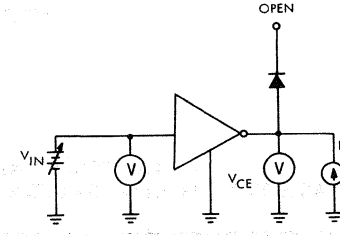
Dwg. No. A-9732

FIGURE 4



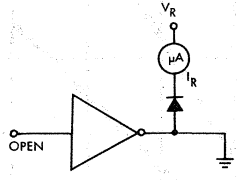
Dwg. No. A-9733A

FIGURE 5



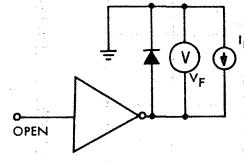
Dwg. No. A-9734A

FIGURE 6



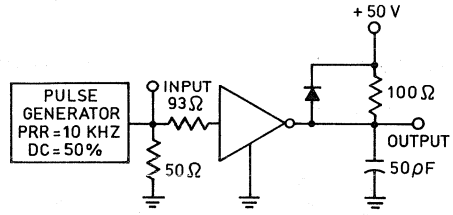
Dwg. No. A-9735A

FIGURE 7

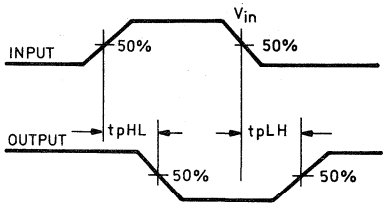


Dwg. No. A-9736

	V_{IN}
ULS20X1*	3.5 V
ULS20X2*	13 V
ULS20X3*	3.5 V
ULS20X4*	12 V
ULS20X5*	3.5 V



Dwg. No. A-13,273



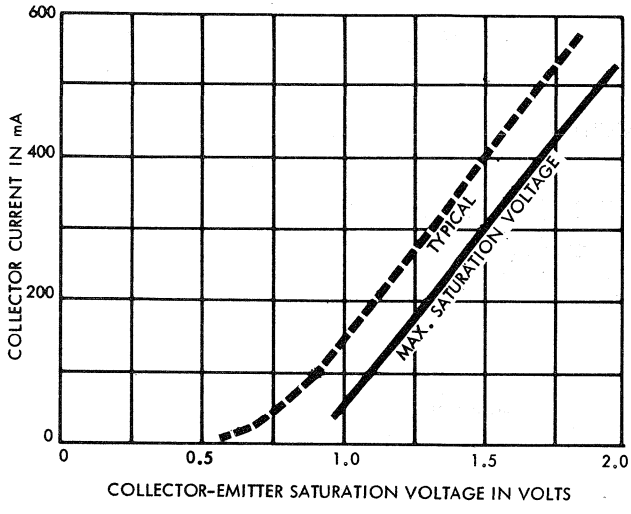
Dwg. No. A-13,272

* Complete part number includes a final letter to indicate package.

X= Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

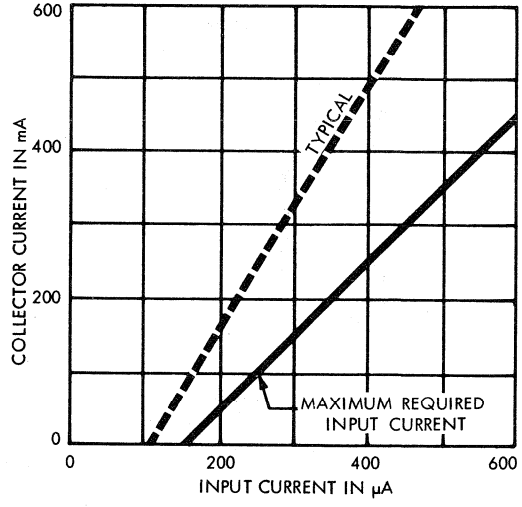
FIGURE 8

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



Dwg. No. A-9754C

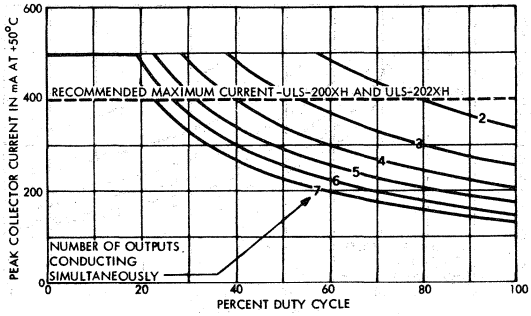
COLLECTOR CURRENT AS A FUNCTION OF INPUT VOLTAGE



Dwg. No. A-10,872B

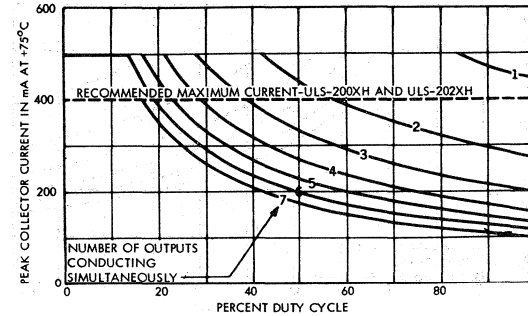
ULS20XXH

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



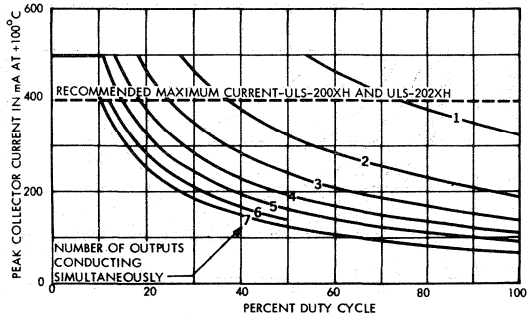
Dwg. No. A-10,197B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



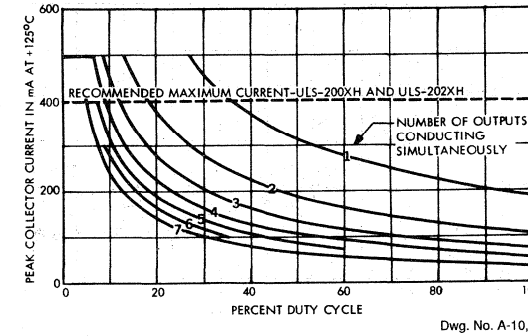
Dwg. No. A-10,199B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-10,200B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

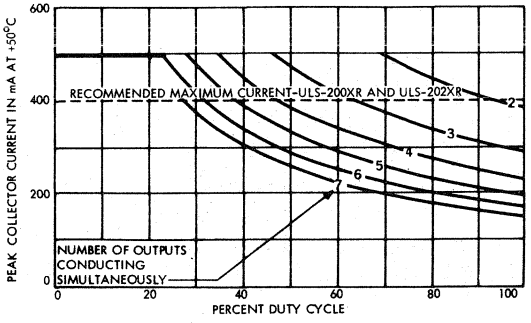


Dwg. No. A-10,201B

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

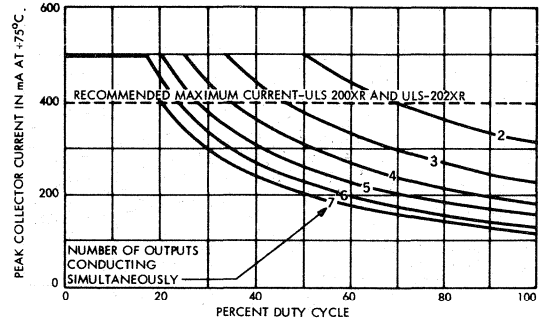
ULS20XXR

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



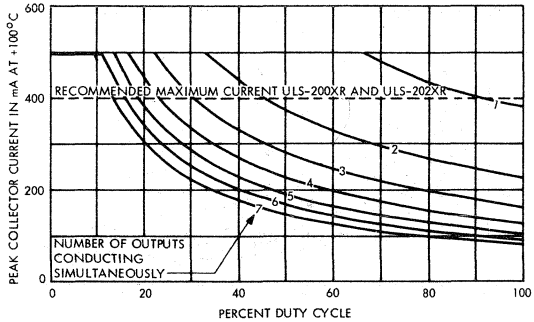
Dwg. No. A-10,883B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



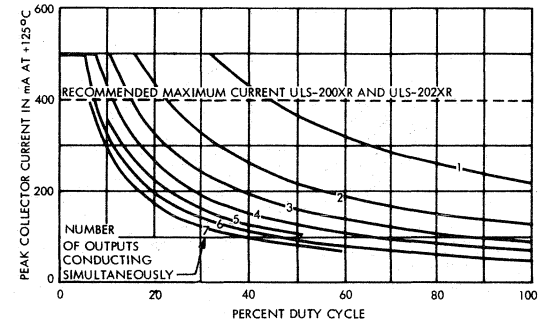
Dwg. No. A-10,887B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-12,434

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

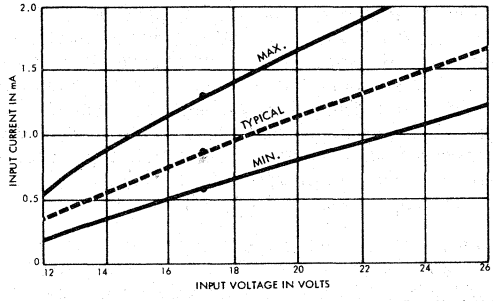


Dwg. No. A-12,435

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

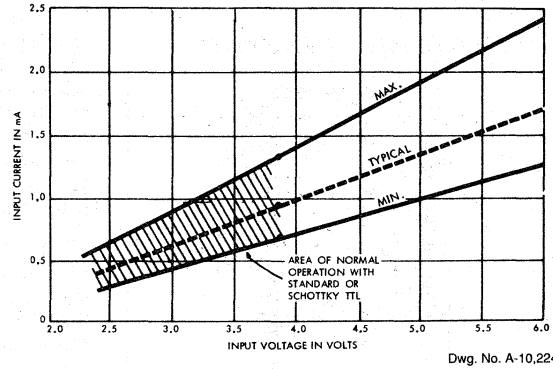
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS20X2*



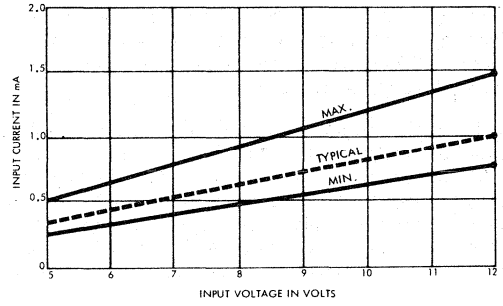
Dwg. No. A-10,225A

ULS20X3*



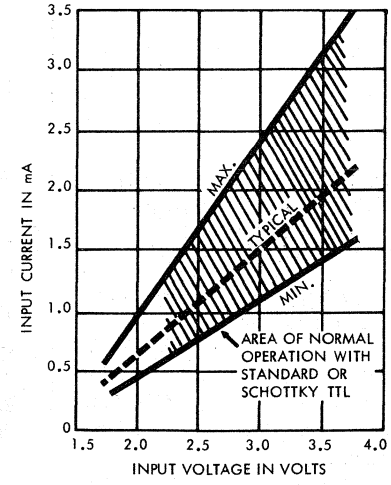
Dwg. No. A-10,224A

ULS20X4*



Dwg. No. A-10,226A

ULS20X5*



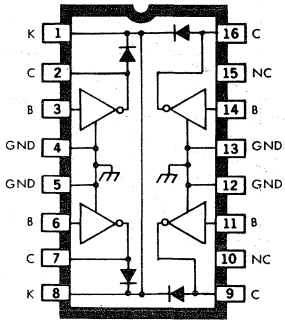
Dwg. No. A-10,874A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

2064 THRU 2077

1.25 A QUAD DARLINGTON SWITCHES —MIL-STD-883 COMPLIANT

ULS2064H – ULS2067H



Dwg. No. A-11,025

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature for any one driver (unless otherwise noted).

Output Voltage, V_{CEX} . . . . . **See Table**
Output Sustaining Voltage, $V_{CE(SUS)}$ . . . . . **See Table**
Output Current, I_{OUT} (Note 1) . . . . . **1.5 A**
Input Voltage, V_{IN} (Note 2) . . . . . **See Table**
Input Current, I_B (Note 3) . . . . . **25 mA**
Supply Voltage, V_S
(ULS2068/69H) . . . . . **10 V**
(ULS2070/71H) . . . . . **20 V**
Power Dissipation, P_D
(Each Output) . . . . . **2.2 W**
(Total Package) . . . . . **See Graph**
Operating Ambient Temperature Range, T_A . . . . . **-55°C to +125°C**
Storage Temperature Range, T_S . . . . . **-65°C to +150°C**

Intended for military, aerospace, and related applications, ULS2064H through ULS2077H quad Darlington switches interface between low-level logic and a variety of peripheral power loads such as relays, solenoids, dc and stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, heaters, and similar loads of up to 400 watts (1.25 A per output, 80 V, 12.5% duty cycle, +50°C). The devices are specified with a minimum output breakdown of 50 volts (35 volts sustaining at 100 mA) or 80 volts (50 volts sustaining), and a saturated output current specification of 1.25 A.

The ULS2064/65/68/69H switches are designed for use with TTL, DTL, Schottky TTL, and 5 V CMOS logic. The ULS2066/67/70/77H are intended for use with 6 V to 15 V CMOS and PMOS logic. Except for the ULS2077H, these devices include integral transient-suppression diodes for use with inductive loads.

Types ULS2068H and ULS2069H incorporate a pre-driver stage operating from a low-current, 5 V supply. The pre-driver for the ULS2070H and ULS2071H operates from a low-current, 12 V supply. The input drive requirements for these devices are reduced, while still allowing the outputs to switch currents up to 1.5 A.

The ULS2074H through ULS2077H switches are intended for use in emitter-follower applications. These circuits are identical with the ULS2064H through ULS2067H except for the uncommitted emitters and the omission of the suppression diodes.

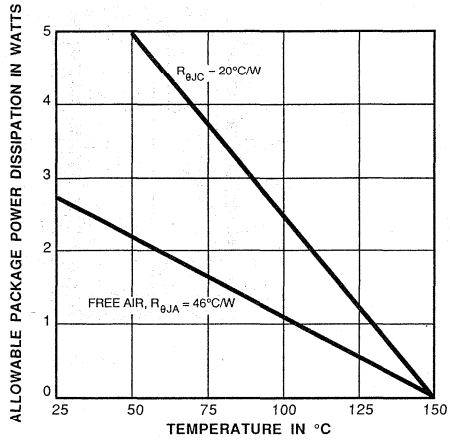
These quad Darlington switches are supplied in 16-pin ceramic/metal side-brazed hermetic packages. On special order, economical ceramic/glass cer-DIP hermetic packages can be specified by changing the part number suffix from 'H' to 'R'. Both package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the military temperature range of -55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Units
- Transient-Protected Outputs
- Hermetically Sealed Packages
- High-Reliability Screening to MIL-STD-883, Class B

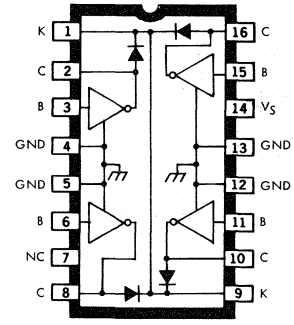
Always order by complete part number, e.g., **ULS2064H883**.
See matrix on next page.

2064 THRU 2077
1.25 A QUAD DARLINGTON SWITCHES



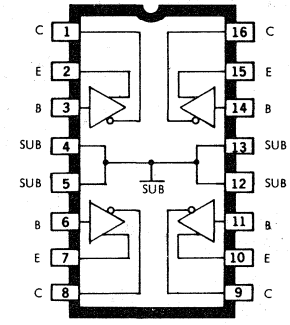
Dwg. GM-002

ULS2068H – ULS2071H



Dwg. No. A-11,026

ULS2074H – ULS2077H



Dwg. No. A-11,027

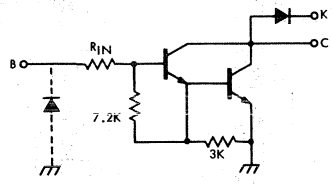
Type Number	V_{CEX} (Max.)	$V_{CE(SUS)}$ (Min.)	V_{IN} (Max.)	Application
ULS2064H	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULS2065H	80 V	50 V	15 V	and 5 V CMOS
ULS2066H	50 V	35 V	30 V	6 to 15 V CMOS
ULS2067H	80 V	50 V	30 V	and PMOS
ULS2068H	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULS2069H	80 V	50 V	15 V	and 5 V CMOS
ULS2070H	50 V	35 V	30 V	6 to 15 V CMOS
ULS2071H	80 V	50 V	30 V	and PMOS
ULS2074H	50 V	35 V	30 V	General-Purpose
ULS2075H	80 V	50 V	60 V	
ULS2076H	50 V	35 V	30 V	6 to 15 V CMOS
ULS2077H	80 V	50 V	60 V	and PMOS

NOTES: 1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.
2. Input voltage is with reference to the substrate (no connection to any other pins) for the ULS2074/75/76/77H, reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

2064 THRU 2077
1.25 A QUAD DARLINGTON SWITCHES

ULS2064H THROUGH ULS2067H

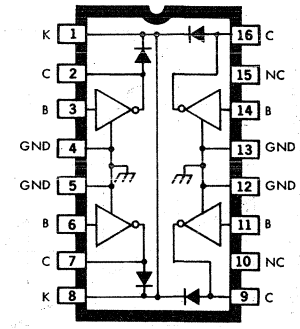
PARTIAL SCHEMATIC



Dwg. No. A-10,353

ULS2064H
ULS2065H R_{IN} = 350 Ω

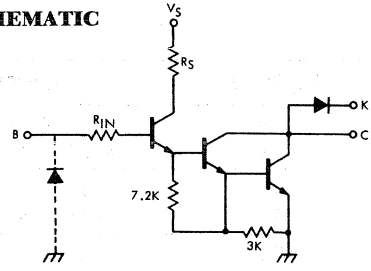
ULS2066H
ULS2067H R_{IN} = 3 kΩ



Dwg. No. A-11,025

ULS2068H THROUGH ULS2071H

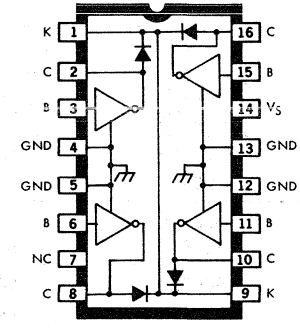
PARTIAL SCHEMATIC



Dwg. No. A-10,354

ULS2068H
ULS2069H R_{IN} = 2.5 kΩ, R_S = 900 Ω

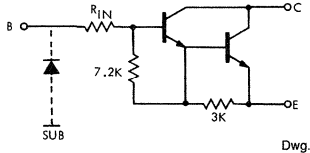
ULS2070H
ULS2071H R_{IN} = 11.6 kΩ, R_S = 3.4 kΩ



Dwg. No. A-11,026

ULS2074H THROUGH ULS2077H

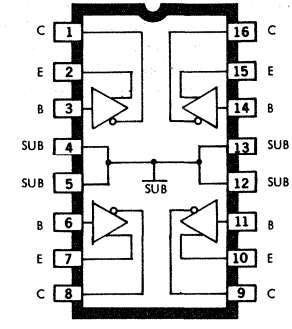
PARTIAL SCHEMATIC



Dwg. No. A-10,355

ULS2074H
ULS2075H R_{IN} = 350 Ω

ULS2076H
ULS2077H R_{IN} = 3 kΩ



Dwg. No. A-11,027

ULS2064H THRU ULS2067H
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS2064/66H		V_{CE} = 50 V	1	—	500	µA
		ULS2065/67H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS2064/66H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS2065/67H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 500 mA, I_B = 1.1 mA	3	—	1.35	V
				I_C = 750 mA, I_B = 1.7 mA	3	—	1.55	V
				I_C = 1.0 A, I_B = 2.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 3.75 mA	3	—	1.95	V
			+25°C	I_C = 500 mA, I_B = 625 µA	3	—	1.20	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.35	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.55	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.75	V
			+125°C	I_C = 500 mA, I_B = 625 µA	3	—	1.35	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.55	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS2064/65H		V_{IN} = 2.4 V	4	—	4.3	mA
				V_{IN} = 3.75 V	4	—	9.6	mA
		ULS2066/67H		V_{IN} = 5.0 V	4	—	1.8	mA
				V_{IN} = 12 V	4	—	5.2	mA
Input Voltage	$V_{IN(ON)}$	ULS2064/65H	-55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.1	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.0	V
		ULS2066/67H	-55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	11.5	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	6.5	V
Turn-On Delay	t_{pHL}	All	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	All	+25°C		9	—	1.5	µs
Clamp Diode Leakage Current	I_R	ULS2064/66H		V_R = 50 V	6	—	100	µA
		ULS2065/67H		V_R = 80 V	6	—	100	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 1.25 A	7	—	2.1	V

ULS2068H AND ULS2069H
ELECTRICAL CHARACTERISTICS over operating temperature range, V_S = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS2068H		V_{CE} = 50 V	1	—	500	µA
		ULS2069H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS2068H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS2069H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	Both	-55°C	I_C = 500 mA, V_{IN} = 3.2 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 3.2 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 3.2 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 3.2 V	3	—	1.95	V
			+25°C	I_C = 500 mA, V_{IN} = 2.9 V	3	—	1.20	V
				I_C = 750 mA, V_{IN} = 2.9 V	3	—	1.35	V
				I_C = 1.0 A, V_{IN} = 2.9 V	3	—	1.55	V
				I_C = 1.25 A, V_{IN} = 2.9 V	3	—	1.75	V
			+125°C	I_C = 500 mA, V_{IN} = 2.8 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 2.8 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 2.8 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 2.8 V	3	—	1.95	V
Input Current	$I_{IN(ON)}$	Both	-55°C	V_{IN} = 3.2 V	4	—	600	µA
			+25°C	V_{IN} = 2.75 V	4	—	550	µA
			+125°C	V_{IN} = 2.75 V	4	—	850	µA
				V_{IN} = 3.75 V	4	—	850	µA
Input Voltage	$V_{IN(ON)}$	Both	-55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.2	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.75	V
Supply Current	I_S	Both		I_C = 500 mA, V_{IN} = 3.2 V	8	—	6.0	mA
Turn-On Delay	t_{pHL}	Both	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	Both	+25°C		9	—	1.5	µs
Clamp Diode Leakage Current	I_R	ULS2068H		V_R = 50 V	6	—	100	µA
		ULS2069H		V_R = 80 V	6	—	100	µA
Clamp Diode Forward Voltage	V_F	Both		I_F = 1.25 A	7	—	2.1	V

ULS2070H AND ULS2071H
ELECTRICAL CHARACTERISTICS over operating temperature range, V_S = 12 V (unless otherwise noted).

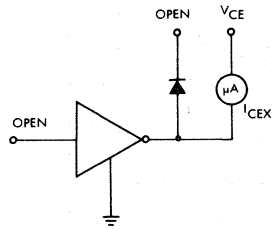
Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS2070H		V_{CE} = 50 V	1	—	500	µA
		ULS2071H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS2070H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS2071H		I_C =100 mA,V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	Both	-55°C	I_C = 500 mA, V_{IN} = 5.5 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 5.5 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 5.5 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 5.5 V	3	—	1.95	V
			+25°C	I_C = 500 mA, V_{IN} = 5.1 V	3	—	1.20	V
				I_C =750 mA, V_{IN} = 5.1 V	3	—	1.35	V
				I_C = 1.0 A, V_{IN} = 5.1 V	3	—	1.55	V
				I_C = 1.25 A, V_{IN} = 5.1 V	3	—	1.75	V
			+125°C	I_C = 500 mA, V_{IN} = 5.0 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 5.0 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 5.0 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 5.0 V	3	—	1.95	V
Input Current	$I_{IN(ON)}$	Both	-55 to +25°C	V_{IN} = 5.0 V	4	—	400	µA
				V_{IN} = 12 V	4	—	1250	µA
			+125°C	V_{IN} = 5.0 V	4	—	800	µA
				V_{IN} = 12 V	4	—	1600	µA
Input Voltage	$V_{IN(ON)}$	Both	-55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	5.0	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	5.0	V
Supply Current	I_S	Both	-55 to +25°C	I_C = 500 mA, V_{IN} = 5.0 V	8	—	4.5	mA
			+125°C	I_C = 500 mA, V_{IN} = 5.0 V	8	—	6.0	mA
Turn-On Delay	t_{pHL}	Both	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	Both	+25°C		9	—	1.5	µs
Clamp Diode Leakage Current	I_R	ULS2070H		V_R = 50 V	6	—	100	µA
		ULS2071H		V_R = 80 V	6	—	100	µA
Clamp Diode Forward Voltage	V_F	Both		I_F = 1.25 A	7	—	2.1	V

ULS2074H THROUGH ULS2077H
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS2074/76H		V_{CE} = 50 V	1	—	500	µA
		ULS2075/77H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS2074/76H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS2075/77H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 500 mA, I_B = 1.1 mA	3	—	1.35	V
				I_C = 750 mA, I_B = 1.7 mA	3	—	1.55	V
				I_C = 1.0 A, I_B = 2.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 3.75 mA	3	—	1.95	V
			+25°C	I_C = 500 mA, I_B = 625 µA	3	—	1.20	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.35	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.55	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.75	V
			+125°C	I_C = 500 mA, I_B = 625 µA	3	—	1.35	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.55	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS2074/75H		V_{IN} = 2.4 V	4	—	4.3	mA
				V_{IN} = 3.75 V	4	—	9.6	mA
		ULS2076/77H		V_{IN} = 5.0 V	4	—	1.8	mA
				V_{IN} = 12 V	4	—	5.2	mA
Input Voltage	$V_{IN(ON)}$	ULS2074/75H	-55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.1	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.0	V
		ULS2076/77H	-55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	11.5	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	6.5	V
Turn-On Delay	t_{pHL}	All	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	All	+25°C		9	—	1.5	µs

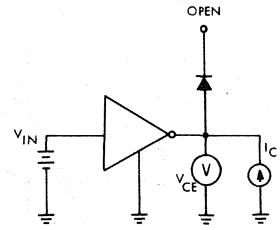
TEST FIGURES

Figure 1



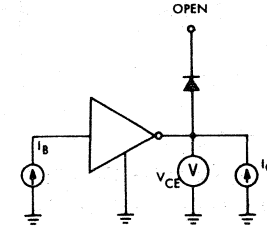
Dwg. No. A-9729A

Figure 2



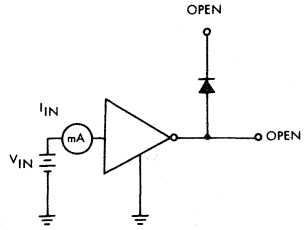
Dwg. No. A-10,350

Figure 3



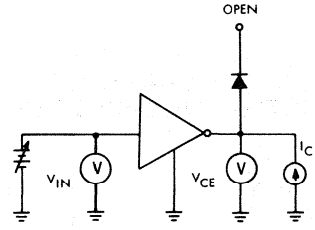
Dwg. No. A-10,349

Figure 4



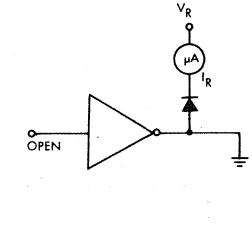
Dwg. No. A-9732

Figure 5



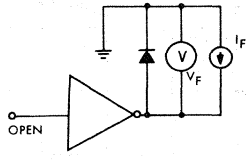
Dwg. No. A-9734A

Figure 6



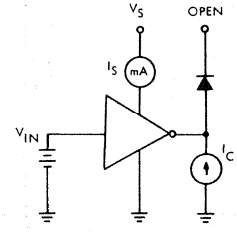
Dwg. No. A-9735A

Figure 7



Dwg. No. A-9736

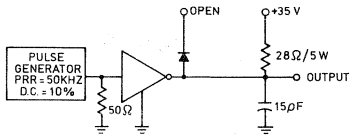
Figure 8



Dwg. No. A-10,351

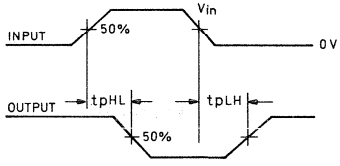
NOTE: Diodes not applicable to Types ULS2074H through ULS2077H.

Figure 9



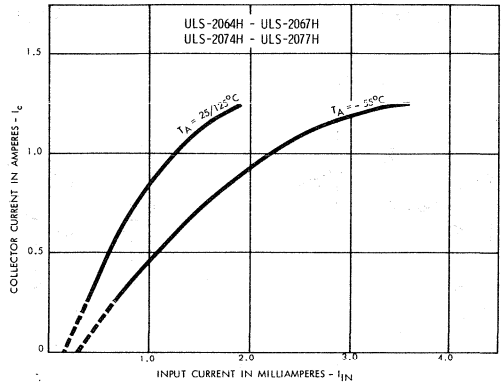
Dwg. No. A-13,247

	V_{IN}
ULS2064/65/68/69/74/75H	2.4 V
ULS2066/67/70/71/76/77H	5.0 V



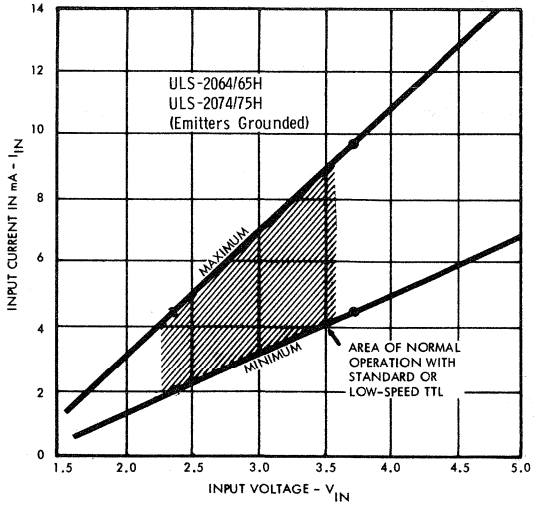
Dwg. No. A-13,248

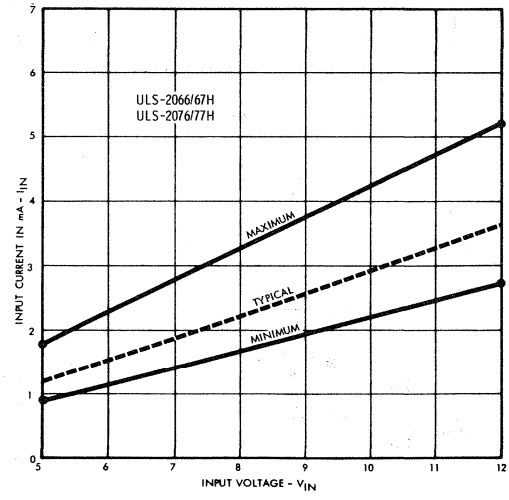
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



Dwg. No. A-11,030

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

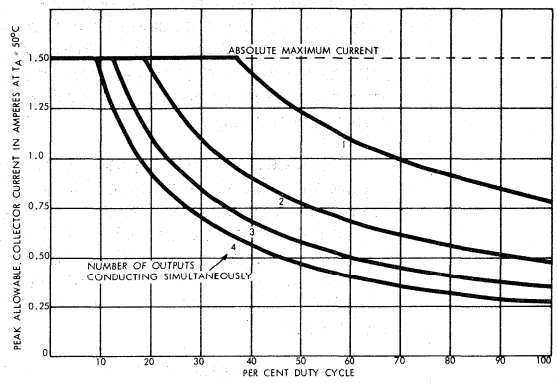




Dwg. No. A-11,035

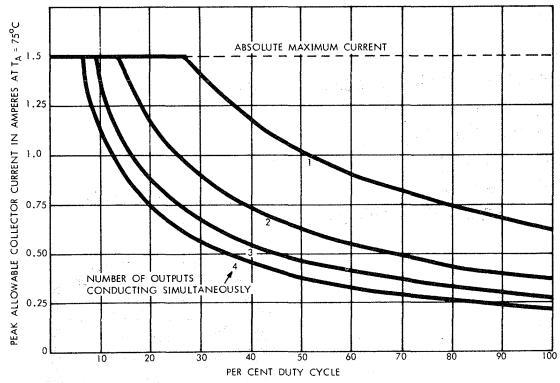
RECOMMENDED PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

AT T_A = +50°C



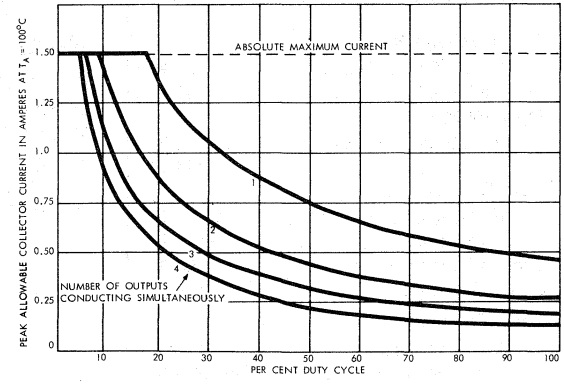
Dwg. No. A-11,031

AT T_A = +75°C



Dwg. No. A-11,032

AT T_A = +100°C

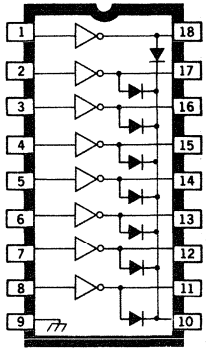


Dwg. No. A-11,033

2801 THRU 2825

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

ULS28XXH/R



Dwg. No. A-10,322

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
(ULS280X*, ULS281X*) . . . . . **50 V**
(ULS282X*) . . . . . **95 V**
Input Voltage, V_{IN}
(ULS28X2*, X3*, X4*) . . . . . **30 V**
(ULS28X5*) . . . . . **15 V**
Peak Output Current, I_{OUT}
(ULS280X*, ULS282X*) . . . . . **500 mA**
(ULS281X*) . . . . . **600 mA**
Ground Terminal Current, I_{GND} . . . . . **3.0 A**
Continuous Input Current, I_{IN} . . . . . **25 mA**
Power Dissipation, P_D
(one Darlington pair) . . . . . **1.0 W**
(total package) . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

X = digit to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown.

*Complete part number includes a final letter to indicate package.

Designed to serve as interface between low-level circuitry and high-power loads, Series ULS2800EK, ULS2800H, and ULS2800R arrays consist of eight silicon NPN Darlington power drivers on a common monolithic substrate. They are ideally suited to driving relays, solenoids, magnetic print hammers, lamps, and other devices in high-reliability military or aerospace applications with up to 3 A output current per package.

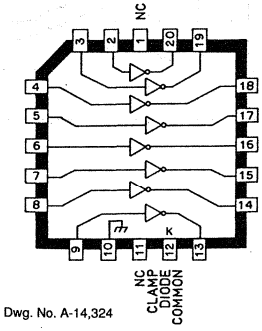
These devices are screened to MIL-STD-883, Class B and are supplied in a leadless ceramic chip carrier with Kovar lid (suffix 'EK'), the popular ceramic/metal side-brazed 18-pin hermetic package (suffix 'H'), or ceramic/glass cer-DIP hermetic package (suffix 'R'). All package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of -55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

The 35 integrated circuits described here permit the circuit designer to select the optimal device for any application. In addition to the three package styles (note that the ceramic chip carrier is available only for the ULS2801EK through ULS2805EK devices), there are five input characteristics, two output-voltage ratings, and two output-current ratings. The appropriate part for specific applications can be determined from the Device Part Number Designation chart. All units have open-collector outputs and on-chip diodes for inductive-load transient suppression.

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B
- -55°C to +125°C Temperature Range

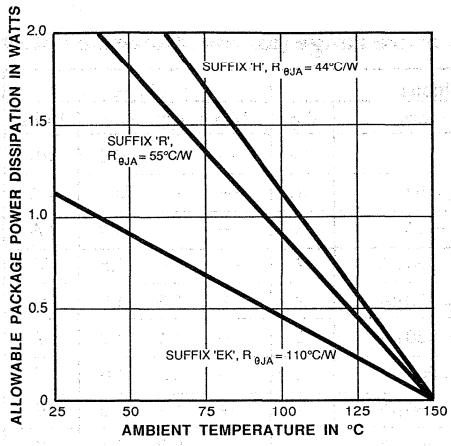
ULS280XEK



Dwg. No. A-14,324

Always order by complete part number, e.g., **ULS2813H883** .
See matrix on next page.

2801 THRU 2825
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS



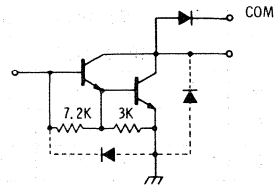
Dwg. GM-005

DEVICE PART NUMBER DESIGNATION

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic		**Part Number**	
General Purpose PMOS, CMOS	ULS2801*	ULS2811*	ULS2821*
14-25 V PMOS	ULS2802*	ULS2812*	ULS2822*
5 V TTL, CMOS	ULS2803*	ULS2813*	ULS2823*
6-15 V CMOS, PMOS	ULS2804*	ULS2814*	ULS2824*
High-Output TTL	ULS2805*	ULS2815*	ULS2825*

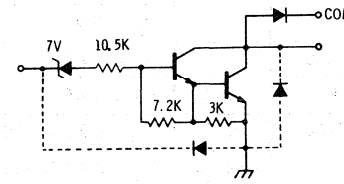
PARTIAL SCHEMATICS

ULS28X1*
(Each Driver)



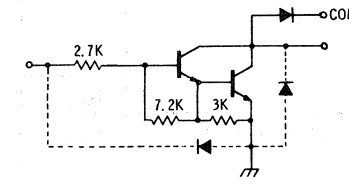
Dwg. No A-9595

ULS28X2*
(Each Driver)



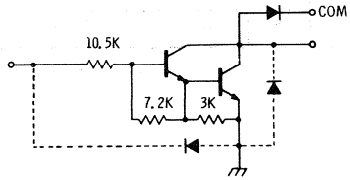
Dwg. No A-9650

ULS28X3*
(Each Driver)



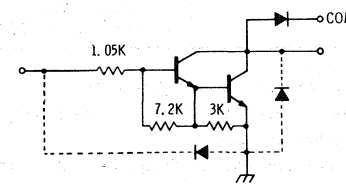
Dwg. No. A-9651

ULS28X4*
(Each Driver)



Dwg. No. A-9898A

ULS28X5*
(Each Driver)



Dwg. No. A-10,228

** Complete part number includes a final letter to indicate package (EK = leadless ceramic chip carrier, H = ceramic/metal side-brazed, R = cermic/glass cer-DIP.*

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

ULS2801EK/H/R THRU ULS2805EK/H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS2802*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2804*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS2802*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2803*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2804*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2805*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2802*	-55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	13	V
		ULS2803*	-55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V

*Complete part number includes a final letter to indicate package
(EK = leadless ceramic chip carrier, H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

Continued next page...

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2801EK/H/R THRU ULS2805EK/H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2804*	-55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS2805*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2801*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (EK = leadless ceramic chip carrier, H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2811H/R THRU ULS2815H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS2812*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2814*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 500 mA, I_B = 1100 µA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 µA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+125°C	I_C = 500 mA†, I_B = 600 µA	2	—	1.8	2.1	V
				I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS2812*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2813*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2814*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2815*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2812*	-55°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	23.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	17	V
		ULS2813*	-55°C	V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	6.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	3.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

Continued next page...

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2811H/R THRU ULS2815H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2814*	-55°C	V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
			+125°C	V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	9.5	V
		ULS2815*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	3.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2811*	-55°C	V_{CE} = 2.0 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 500 mA	2	900	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V
				I_F = 500 mA†	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2821H/R THRU ULS2825H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	µA
		ULS2822*		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2824*	+25°C	V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	µA
			+125°C	V_{CE} = 95 V, V_{IN} = 0.5 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS2822*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2823*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2824*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2825*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	20	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2822*	-55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	13	V
		ULS2823*	-55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

Continued next page...

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2821H/R THRU ULS2825H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2824*	-55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS2825*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2821*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate pachage (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

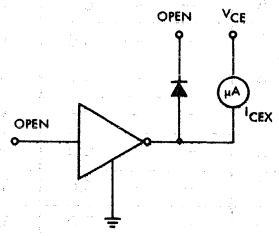
NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

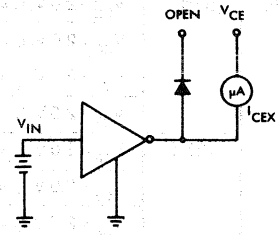
TEST FIGURES

FIGURE 1A



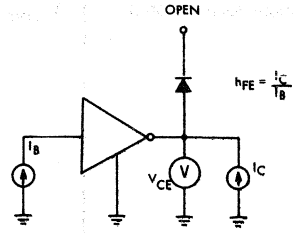
Dwg. No. A.-9729A

FIGURE 1B



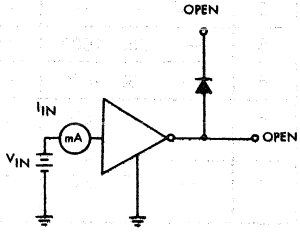
Dwg. No. A-9730A

FIGURE 2



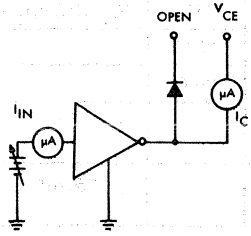
Dwg. No. A-9731

FIGURE 3



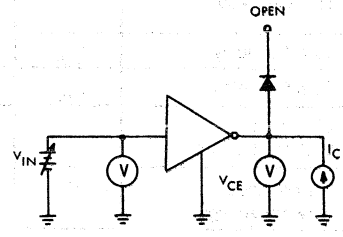
Dwg. No. A-9732

FIGURE 4



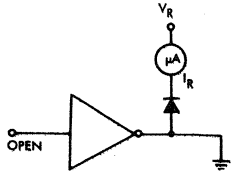
Dwg. No. A-9733A

FIGURE 5



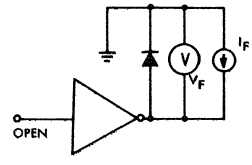
Dwg. No. A-9734A

FIGURE 6



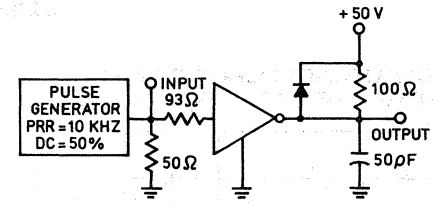
Dwg. No. A-9735A

FIGURE 7

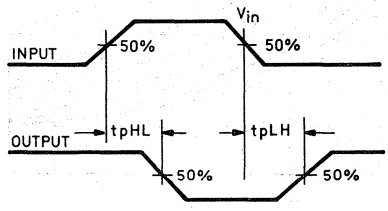


Dwg. No. A-9736

	V_{IN}
ULS28X1*	3.5 V
ULS28X2*	13 V
ULS28X3*	3.5 V
ULS28X4*	12 V
ULS28X5*	3.5 V



Dwg. No. A-13,273



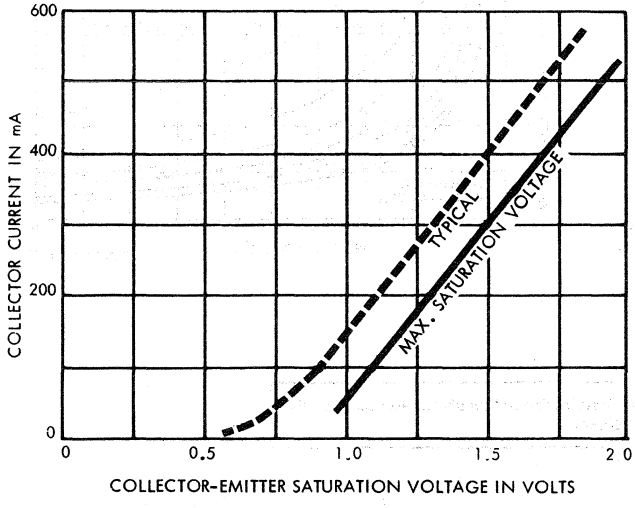
Dwg. No. A-13,272

* Complete part number includes a final letter to indicate package.

X= Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

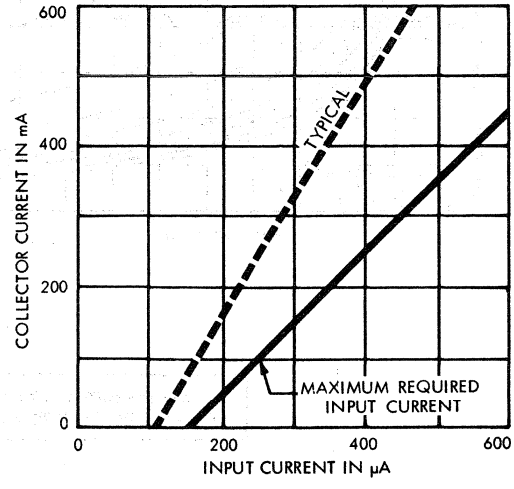
FIGURE 8

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



Dwg. No. A-9754C

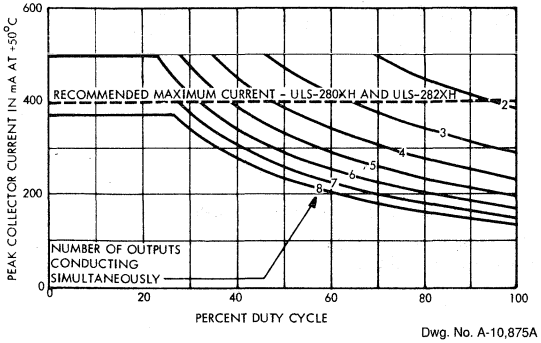
COLLECTOR CURRENT AS A FUNCTION OF INPUT VOLTAGE



Dwg. No. A-10,872B

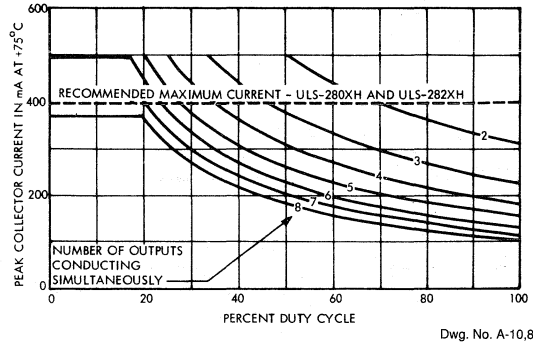
ULS28XXH

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



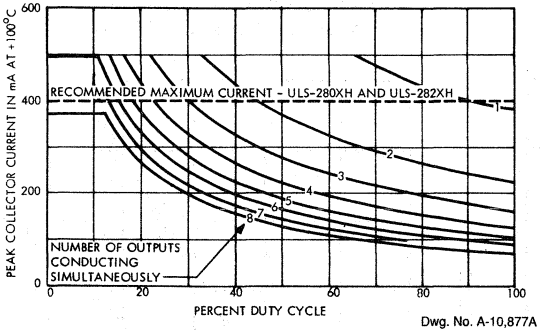
Dwg. No. A-10,875A

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



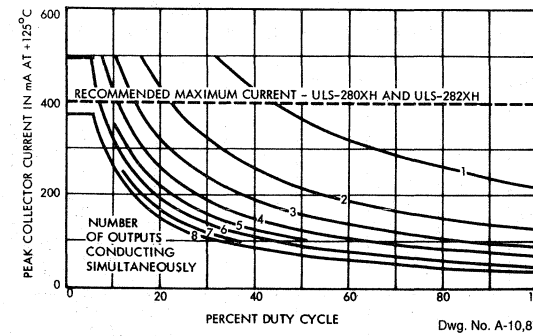
Dwg. No. A-10,876A

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-10,877A

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

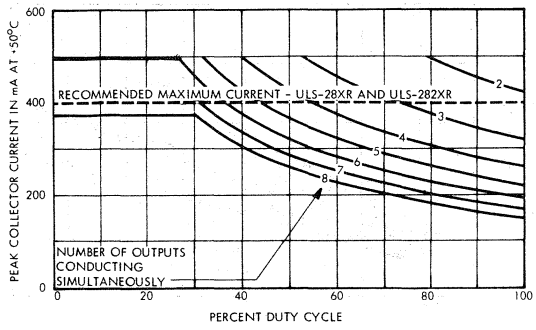


Dwg. No. A-10,878A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

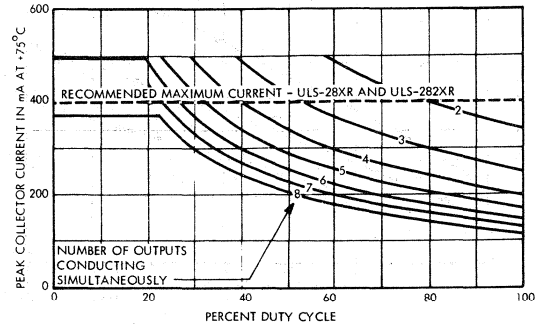
ULS28XXR

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



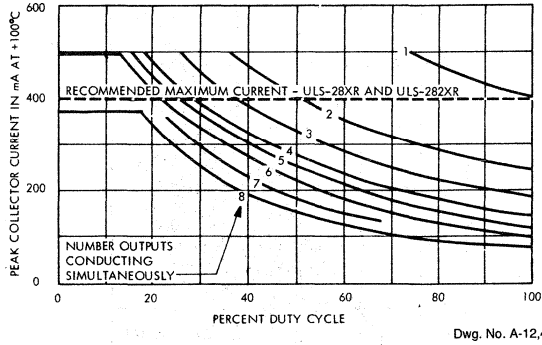
Dwg. No. A-10,870A

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



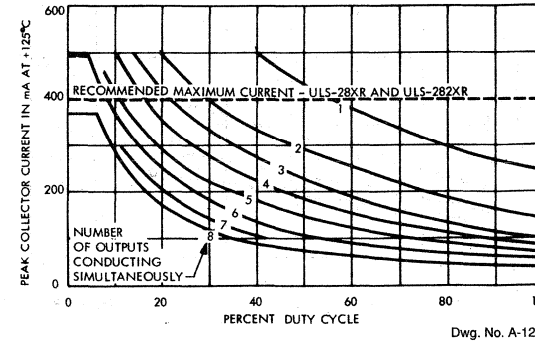
Dwg. No. A-10,871A

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-12,466

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

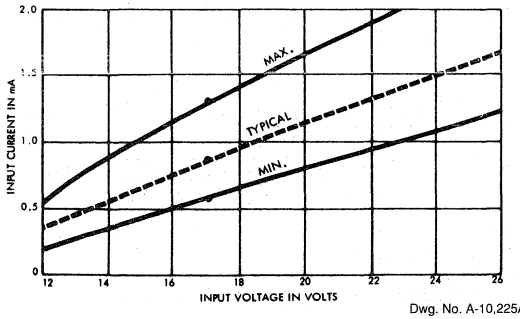


Dwg. No. A-12,467

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

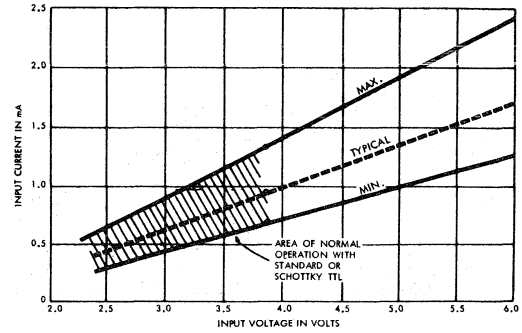
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS28X2*



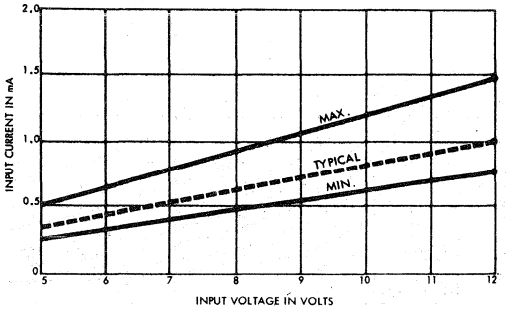
Dwg. No. A-10,225A

ULS28X3*



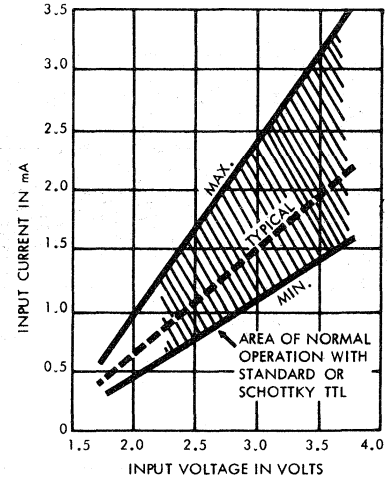
Dwg. No. A-10,224A

ULS28X4*



Dwg. No. A-10,226A

ULS28X5*

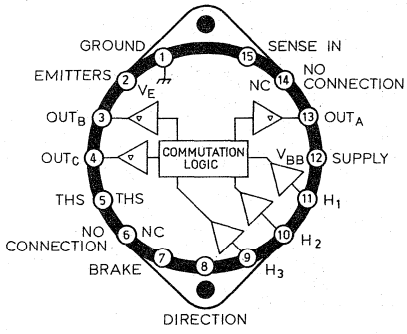


Dwg. No. A-10,874A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

2936
MIL-STD-883 COMPLIANT

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER



Dwg. PM-001

ABSOLUTE MAXIMUM RATINGS

Motor Supply Voltage, V_{BB} . . . . . **45 V**
Output Current, I_{OUT} (300 ms) . . . . . **±2.3 A**
(Continuous) . . . . . **±2.0 A**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to +15 V***
Threshold Voltage, V_{THS} . . . . . **15 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**
Junction Temperature, T_J . . . . . **+150°C†**
Storage Temperature,
T_S . . . . . **-65°C to +150°C**

*V_{IN} must not exceed V_{BB}.

† Fault conditions which produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation the specified maximum junction temperature should not be exceeded.

The UDS2936V combines logic and power to provide commutation and drive for a three-phase brushless dc motor. Each of the three push-pull outputs are rated at 45 V and ±2 A (±2.3 A peak), and have internal inductive-load transient suppression diodes. The driver also includes PWM current control and thermal shutdown protection. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

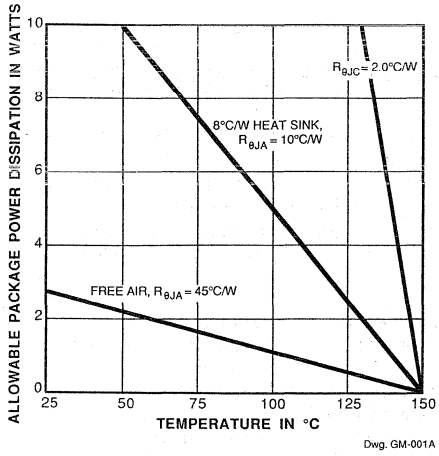
The UDS2936V is compatible with single-ended digital or linear Hall effect sensors and is programmed for 60° electrical separation (other separation sequences, such as 120°, are available). Current control is accomplished by sensing current through an external resistor and pulse-width modulating the source drivers. Voltage thresholds and hysteresis can be externally set by the user. If desired, internal threshold and hysteresis defaults (300 mV, 7.5%) can be used. Internal protection circuitry prevents crossover current when braking or changing direction. The UDS2936V differs from its commercial version (UDN2936W); the output emitters are separated from the current sensor input, thus allowing increased versatility in control techniques.

The UDS2936V is supplied in a 15-pin, flange-mount MO-097AA style hermetic package for improved power dissipation capabilities. An external heatsink is required for high-current applications. The flange is at ground potential and normally needs no isolation.

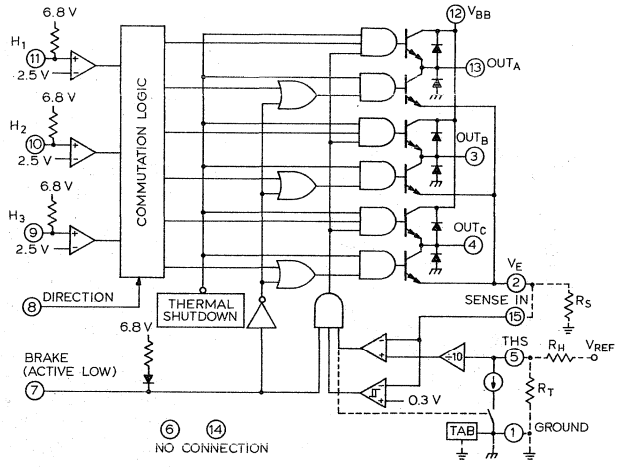
FEATURES

- 10 V to 45 V Operation
- ±2 A Output Current
- Internal Clamp Diodes
- Internal PWM Current Control
- 60° Commutation Decoding Logic
- Internal Thermal Shutdown Circuitry
- Compatible with Digital, Open-Collector Hall Effect Sensors
- Braking and Direction Control
- Hermetically Sealed Package
- High-Reliability Screening

Always order by complete part number: **UDS2936V883** .



FUNCTIONAL BLOCK DIAGRAM



COMMUTATION TRUTH TABLE

Hall Sensor Inputs					Outputs		
H_1	H_2	H_3	DIRECTION	BRAKE	OUT_A	OUT_B	OUT_C
High	High	High	Low	High	Z	Low	High
High	High	Low	Low	High	High	Low	Z
High	Low	Low	Low	High	High	Z	Low
Low	Low	Low	Low	High	Z	High	Low
Low	Low	High	Low	High	Low	High	Z
Low	High	High	Low	High	Low	Z	High
High	High	High	High	High	Z	High	Low
High	High	Low	High	High	Low	High	Z
High	Low	Low	High	High	Low	Z	High
Low	Low	Low	High	High	Z	Low	High
Low	Low	High	High	High	High	Low	Z
Low	High	High	High	High	High	Z	Low
X	X	X	X	Low	Low	Low	Low

X= Irrelevant

Z = High Impedance

ELECTRICAL CHARACTERISTICS at T_A = -55°C to +125°C, V_{BB} = 45 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	V_{BB}	Operating	10	—	45	V
Supply Current	I_{BB}	V_{BRAKE} = 2.0 V, Outputs Open	—	52	60	mA
		V_{BRAKE} = 0.8 V	—	54	60	mA
Output Drivers						
Output Leakage Current	I_{CEX}	V_{OUT} = V_{BB}, Output State = Z	—	<1.0	10	µA
		V_{OUT} = 0 V, Output State = Z	—	< -1.0	-10	µA
Output Saturation Voltage (T_A = -55°C to +25°C)	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -1.0 A	—	1.7	2.1	V
		Sink Driver, I_{OUT} = +1.0 A	—	1.1	1.4	V
		Source Driver, I_{OUT} = -2.0 A	—	1.9	2.3	V
		Sink Driver, I_{OUT} = +2.0 A	—	1.4	1.7	V
Output Saturation Voltage (T_A = +125°C)	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -1.0 A	—	—	1.9	V
		Sink Driver, I_{OUT} = +1.0 A	—	—	1.2	V
		Source Driver, I_{OUT} = -2.0 A	—	—	2.1	V
		Sink Driver, I_{OUT} = +2.0 A	—	—	1.5	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±2.0 A, L = 3.0 mH, T_A = +25°C	45	—	—	V
Output Switching Time (Resistive Load)	t_r	Source Driver, 0 to -2.0 A, 10% to 90%	—	1.25	—	µs
		Sink Driver, 0 to +2.0 A, 10% to 90%	—	1.9	—	µs
	t_f	Source Driver, -2.0 A to 0, 90% to 10%	—	1.7	—	µs
		Sink Driver, +2.0 A to 0, 90% to 10%	—	0.9	—	µs
Clamp Diode Leakage Current	I_R	V_R = 45 V	—	<1.0	10	µA
Clamp Diode Forward Voltage	V_F	I_F = 2.0 A, T_A = -55°C to +25°C	—	1.8	2.3	V
		I_F = 2.0 A, T_A = +125°C	—	—	2.5	V

Typical Data is for design information only and is at T_A = +25°C.

Continued Next Page...

ELECTRICAL CHARACTERISTICS (cont'd)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Logic						
Logic Input Voltage	$V_{IN(1)}$	V_{DIR} or V_{BRAKE}	2.0	—	—	V
	$V_{IN(0)}$	V_{DIR} or V_{BRAKE}	—	—	0.8	V
Sensor Input Threshold	V_{IN}	H_1, H_2, or H_3	—	2.5	—	V
Input Current	$I_{IN(1)}$	V_{DIR} = 2.0 V	—	150	400	µA
		V_{BRAKE} = 2.0 V	—	<1.0	5.0	µA
		V_H = 5.0 V	—	-190	-220	µA
	$I_{IN(0)}$	V_{DIR} = 0.8 V	—	35	100	µA
		V_{BRAKE} = 0.8 V	—	-5.0	-20	µA
		V_H = 0.8 V	—	-640	-1000	µA
	I_{THS}	$V_{THS} \geq 3.0$ V	—	-8.0	-15	µA
		$V_{THS} < 3.0$ V, $V_{SENSE} < V_{THS}/10.5$	—	-15	-30	µA
		$V_{THS} < 3.0$ V, $V_{SENSE} < V_{THS}/9.5$	190	250	310	µA
Current Limit Threshold		V_{THS}/V_{SENSE} at trip point, $V_{THS} < 3.0$ V	9.5	10	10.5	—
Default Sense Trip Voltage	V_{SENSE}	$V_{THS} \geq 3.0$ V	270	300	330	mV
Default Hysteresis		$V_{THS} \geq 3.0$ V	—	7.5	—	%
Propagation Delay Time	t_{pd}	I_{OUT} = ±2.0 A, 50% V_H to 90% I_{OUT}	—	2.0	8.0	µs
Deadtime	t_d	BRAKE or DIRECTION	—	2.0	—	µs
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	25	—	°C

Typical Data is for design information only and is at T_A = +25°C.

APPLICATIONS INFORMATION

The UDS2936V power driver provides commutation logic and power outputs to drive a three-phase brushless dc motor.

It is designed to interface with single-ended linear or digital Hall effect devices (HEDs). Internal pull-up resistors on the inputs allow for direct use with open-collector digital HEDs. The H_N inputs have 2.5 V thresholds.

The commutation logic provides decoding for HEDs with 60° electrical separation (120° separation is also available). At any one step in the sequencing, one half-bridge driver is sourcing, one driver is sinking, and one driver is in a high-impedance state (see truth table). Changing the logic level of the DIRECTION input inverts the output states, thus reversing the direction of the load current and the motor. A logic low on the BRAKE input turns ON all three sink drivers and turns OFF all source drivers, dynamically braking the motor. An internally generated deadtime (t_d) of approximately 2 µs prevents potentially destructive crossover currents that can occur when changing direction or braking. Circuit design consideration and care should preclude exceeding the specified peak current rating during braking or directional change, especially in applications involving high inertial loads and/or higher motor supply voltage operation.

Motor current is internally controlled by pulse-width modulating the source drivers with a preset hysteresis format. Load current through an external sense resistor (R_S) is constantly monitored. When the current reaches the set trip point (determined by an external reference voltage or internal default), the source driver is disabled. The actual load current will peak slightly higher because of the internal logic and switching delays. Current recirculates through the ground clamp diode, motor winding, and sink driver. An internal constant-current sink reduces the trip current (hysteresis). When the decaying current reaches this lower threshold, the source driver is enabled again and the cycle repeats.

Thresholds and hysteresis can be set with external resistors or internal defaults can be used. With V_{THS} < 3.0 V, the trip point is internally set at 300 mV with 7.5% hysteresis. Load trip current is then determined by the equation:

$$I_{TRIP} = 0.3/R_S$$

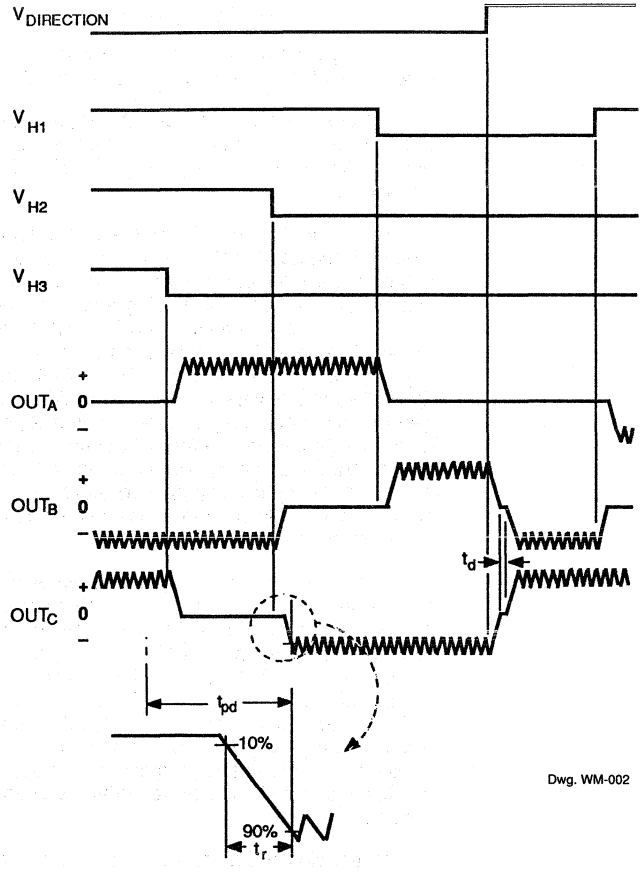
With V_{THS} < 3.0 V, the threshold, hysteresis percentage, and load trip current are set with external resistors according to the equations:

$$\text{Threshold Voltage } (V_{THS}) = \frac{V_{REF} \cdot R_T}{R_H + R_T}$$

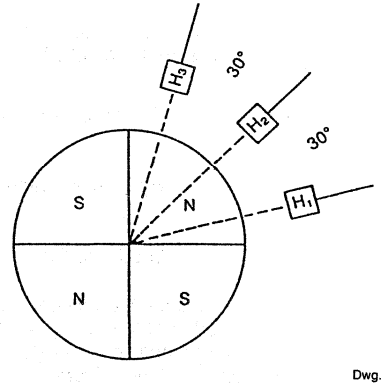
$$\text{Hysteresis Percentage} = \frac{R_H}{50 \cdot V_{REF}}$$

$$\text{Load Trip Current } (I_{TRIP}) = \frac{V_{THS}}{10\ R_S}$$

Percentage hysteresis is a fixed value independent of load current. The PWM frequency is a function of circuit parameters including load inductance, load resistance, supply voltage, hysteresis, and switching speed of the drivers.

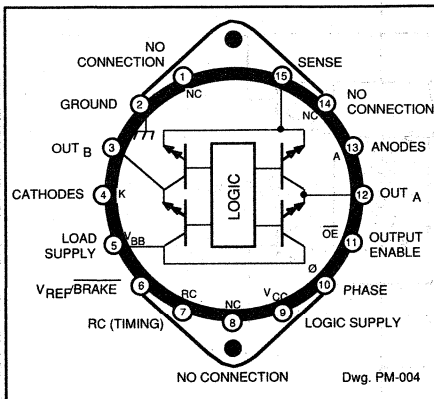


TYPICAL HALL EFFECT/SENSOR LOCATIONS



2953
MIL-STD-883 COMPLIANT

FULL-BRIDGE PWM MOTOR DRIVER



Dwg. PM-004

ABSOLUTE MAXIMUM RATINGS

Motor Supply Voltage, V_{BB} . . . . . **50 V**
Output Current, I_{OUT} (300 ms) . . . . . **±2.3 A**
(Continuous) . . . . . **±2.0 A**
Flyback Diode Voltage, V_K . . . . . **V_{BB}**
Minimum Clamp Diode Voltage, V_A . . . . . **Ground**
Logic Supply Voltage, V_{CC} . . . . . **7.0 V**
Logic Input Voltage Range, V_{IN} . . . . . **-0.3 V to +7.0 V***
Sense Voltage, V_{SENSE} . . . . . **1.5 V**
Reference Voltage, V_{REF}/BRAKE . . . . . **15 V**
Package Power Dissipation, P_D . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-55°C to +125°C**
Junction Temperature, T_J . . . . . **+150°C†**
Storage Temperature Range, T_S . . . . . **-65°C to +150°C**

*V_{IN} must not exceed V_{CC}.

†Fault conditions which produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation the specified maximum junction temperature should not be exceeded.

Designed for bidirectional control of dc or stepper motors, the UDS2953V is rated for continuous output currents to ±2 A. For pulse-width modulated (chopped mode) operation, the output current is determined by the user's selection of a reference voltage and sensing resistor while the OFF pulse duration is set by an external RC timing network. Extensive internal circuit protection includes thermal shutdown with hysteresis, output suppression diodes to protect the bridges from the transients generated when switching inductive loads, and crossover current protection. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

When the V_{REF}/BRAKE pin is low (<0.8 V), the braking function is enabled. This turns both sink drivers OFF and the source drivers are turned ON. When V_{REF}/BRAKE is set above 2.4 V, that voltage (and the current sensing resistor) determines the load current trip point. An RC TIMING pin is provided for control of an internal one-shot and load current decay time.

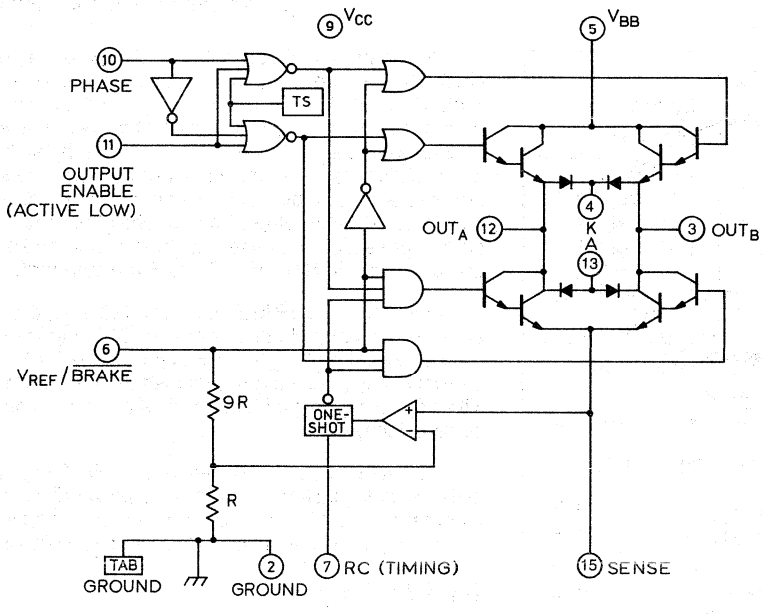
The UDS2953V is supplied in a 15-pin, flange-mount MO-097AA style hermetic package for improved power dissipation capabilities. An external heatsink is required for high-current applications. The flange is at ground potential and normally needs no isolation.

FEATURES

- ±2 A Output Current
- Output Voltage to 50 V
- Internal Flyback Diodes
- Output Current Sensing
- Internal Thermal Shutdown Circuitry
- Crossover-Current Protected
- Hermetically Sealed Package
- High-Reliability Screening

Always order by complete part number: **UDS2953V883**.

FUNCTIONAL BLOCK DIAGRAM

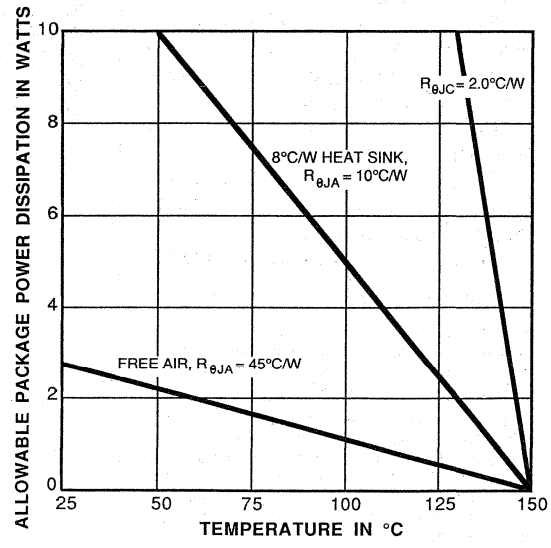


Dwg. FM-002-1

TRUTH TABLE

OUTPUT ENABLE	PHASE	V_{REF}/BRAKE	OUT_A	OUT_B
Low	High	>2.4 V	High	Low
Low	Low	>2.4 V	Low	High
High	X	>2.4 V	Open	Open
X	X	<0.8 V	High	High

x = Irrelevant



Dwg. GM-001A

ELECTRICAL CHARACTERISTICS at T_A = -55°C to +125°C, V_{BB} = 50 V, V_{CC} = 5 V, V_{SENSE} = 0 V, 5 kΩ RC to Ground (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Supply Voltage Range	V_{BB}	Operating	6.5	—	50	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$, V_{ENABLE} = 5.0 V, Note 3	—	<1.0	10	µA
		V_{OUT} = 0 V, V_{ENABLE} = 5.0 V, Note 3	—	<-1.0	-10	µA
Output Saturation Voltage (T_A = -55°C to +25°C)	$V_{CE(SAT)}$	I_{OUT} = ±0.5 A	—	—	1.2	V
		I_{OUT} = ±1.0 A	—	—	1.4	V
		I_{OUT} = ±2.0 A	—	—	1.8	V
Output Saturation Voltage (T_A = +125°C)	$V_{CE(SAT)}$	I_{OUT} = ±0.5 A	—	—	1.0	V
		I_{OUT} = ±1.0 A	—	—	1.2	V
		I_{OUT} = ±2.0 A	—	—	1.6	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±2.0 A, L = 3 mH, T_A = +25°C, Note 3	50	—	—	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	—	10	µA
Clamp Diode Forward Voltage	V_F	I_F = 2.0 A, T_A = -55°C to +25°C	—	—	2.1	V
		I_F = 2.0 A, T_A = +125°C	—	—	2.3	V
Motor Supply Current (No Load)	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V, V_{REF} = 2.4 V	—	20	35	mA
	$I_{BB(OFF)}$	$V_{ENABLE} = V_{REF}$ = 2.4 V	—	2.4	4.0	mA
		V_{ENABLE} = 5.0 V, V_{REF} = 0.8 V	—	40	60	mA

NOTES: 1. Typical Data is for design information only and is at T_A = +25°C.

Continued next page...

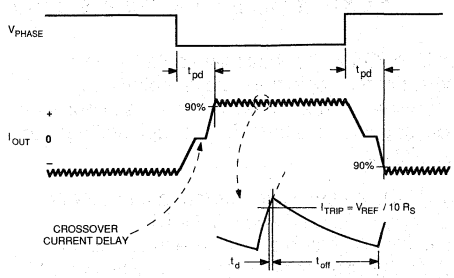
2. Each driver is tested separately.
3. Test is performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.4 V.
4. Negative current is defined as coming out of (sourcing) the specified device pin.

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Control Logic						
Supply Voltage Range	V_{CC}	Operating	4.5	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<-1.0	-20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-50	-200	µA
Current Limit Threshold		V_{REF}/V_{SENSE} at trip point, T_A = +25°C	9.5	10	10.5	—
Reference Voltage	V_{REF}	I_{REF} = 0	—	$V_{CC}/2$	—	V
Propagation Delay Time	t_{pd}	I_{OUT} = ±2.0 A, Note 3, 50% V_{PHASE} to 90% I_{OUT}	—	4.0	8.0	µs
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	8.0	—	°C
Logic Supply Current	I_{CC}	V_{ENABLE} = V_{REF} = 2.4 V	—	17	30	mA
		V_{ENABLE} = 0.8 V, V_{REF} = 2.4 V	—	22	35	mA

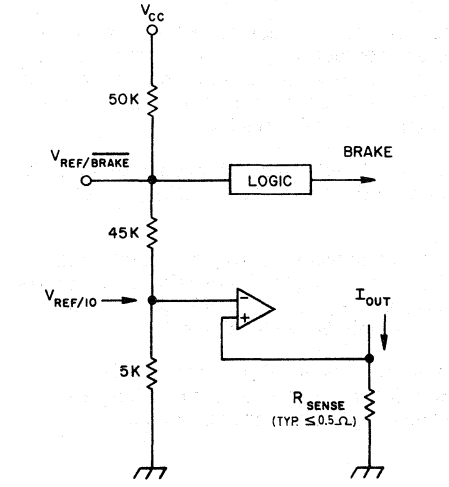
NOTES: 1. Typical Data is for design information only and is at T_A = +25°C.
2. Each driver is tested separately.
3. Test is performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.4 V.
4. Negative current is defined as coming out of (sourcing) the specified device pin.

FIGURE 1



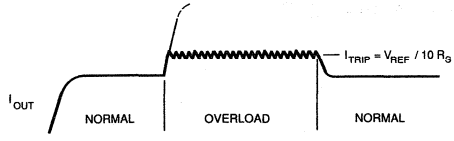
Dwg. WM-003

FIGURE 2



Dwg. No. A-13,025

FIGURE 3



Dwg. WM-004

APPLICATIONS INFORMATION

The UDS2953V full-bridge driver is ideal for driving 2-phase bipolar stepper, bidirectional dc servo, and brushless dc motors with various pulse-width modulation (PWM) current-control formats. Output current is controlled by using an external sense resistor and an optional RC network and reference voltage for an internal fixed-frequency PWM circuit, or by using an external PWM source.

The output current trip point is set up by:

$$I_{TRIP} = \frac{V_{REF}}{10\ R_{SENSE}}$$

When the current in the sense resistor (typically ≤0.5 Ω) reaches the set point, an internal one-shot turns OFF the sink drivers for a time period (t_{off}) determined by the RC time constant. The actual peak load current will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 µs.

The t_{off} time interval (see Fig. 1) is approximately 1/RC within the range of 20 kΩ to 100 kΩ and 200 pF to 500 pF. If the RC pin is tied to V_{CC}, internal delay circuitry is activated, allowing PWM operation without the external RC network. Under this condition, I_{CC} will increase approximately 6 mA. The internally generated t_{off} is approximately 12 µs at V_{CC} = 5 V and T_A = +25°C, increasing slightly with increasing temperatures. The RC pin must be connected to an RC network or to V_{CC}. It must *not* be left unconnected.

For external current control, V_{REF} can be between 2.4 V and 15 V. If left unconnected, V_{REF} defaults to $V_{CC}/2$ (see Fig. 2).

Average load current can also be adjusted by external pulse-width modulation using the OUTPUT ENABLE pin. Toggling the OUTPUT ENABLE line shuts OFF both the source and sink drivers. Both the flyback and ground-clamp diodes conduct, resulting in very fast current decay. In this mode, the RC pin should be connected to ground through a 5 kΩ resistor.

With the RC pin connected to V_{CC}, V_{REF} and R_{SENSE} selected for a trip point greater than normal operation, but less than the absolute maximum allowable, over-current protection is provided (Fig. 3).

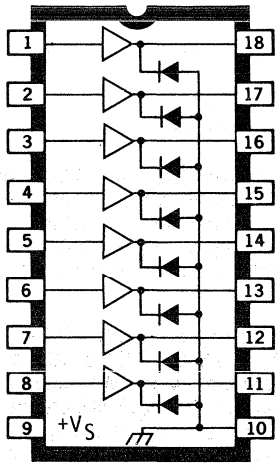
A logic low at the V_{REF}/BRAKE pin turns ON both source drivers and turns OFF both sink drivers, thus dynamically braking the motor.

An internally generated deadtime of approximately 3 µs reduces crossover currents that can occur when switching phases or braking.

Thermal protection circuitry is activated and turns OFF all drivers at a junction temperature of typically 165°C. It is only intended to protect the chip from catastrophic failures due to excessive junction temperatures. The thermal shutdown has a hysteresis of approximately 8°C.

SERIES 2980
MIL-STD-883 COMPLIANT

HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS



Dwg. No. A-10,243

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage Range, V_{CE}
(UDS2981 and UDS2982H/R) . . . . . **5 V to 50 V**
(UDS2983 and UDS2984H/R) . . . . . **35 V to 80 V**
Input Voltage, V_{IN}
(UDS2981 and UDS2983H/R) . . . . . **15 V**
(UDS2982 and UDS2984H/R) . . . . . **30 V**
Output Current, I_{OUT} . . . . . **-500 mA**
Ground Terminal Current, I_{GND} . . . . . **3.0 A**
Power Dissipation, P_D
(any one driver) . . . . . **1.1 W**
(total package) . . . . . **See Graph**
Operating Temperature Range, T_A . . . . . **-55°C to +125°C**
Storage Temperature Range, T_S . . . . . **-65°C to +150°C**

Series UDS2980H and UDS2980R hermetically sealed source drivers link standard low-power digital logic and relays, solenoids, magnetic print hammers, stepping motors, LEDs, and lamps in applications requiring separate logic and load grounds, load supply voltages to +80 V, and load currents to 500 mA.

Types UDS2981H/R and UDS2983H/R are intended for use with 5 V logic systems (TTL, Schottky TTL, DTL and 5 V CMOS). UDS2982H/R and UDS2984H/R integrated circuits are intended for MOS interface (PMOS and CMOS) operating from supply voltages of from 6 to 16 V.

Types UDS2981H/R and UDS2982H/R will withstand an output OFF voltage of 50 V. UDS2983H/R and UDS2984H/R drivers will withstand a maximum output OFF voltage of 80 V.

Under normal operating conditions, the devices will sustain 50 mA continuously on each of the eight outputs at an ambient temperature of +85°C and with a supply voltage of 15 V. All types include input current-limiting resistors and output transient-suppression diodes. In all cases, outputs are switched ON by an active high input level.

Note that the maximum current rating may not be obtained at -55°C because of reduced beta, or at +125°C because of package power limitations.

Series UDS2980H drivers are furnished in 18-pin ceramic/metal (side-brazed) hermetic dual in-line packages. Series UDS2980R drivers are supplied in ceramic/glass (cer-DIP) hermetic packages. Both are processed to the requirements of MIL-STD-883, Class B.

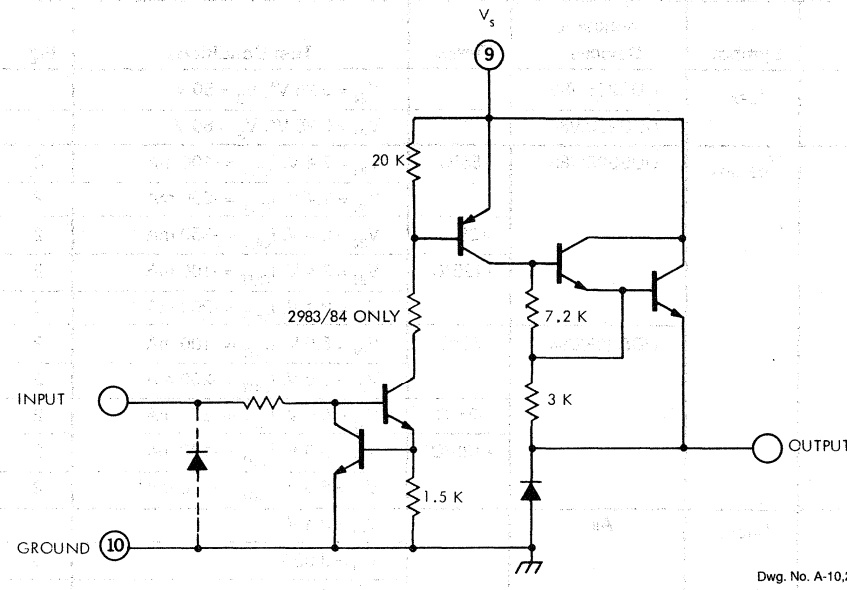
The same circuits are also available in 18-pin plastic dual in-line packages (Series UDN2980A) for operation over a limited temperature range, or where higher package power dissipation is needed.

FEATURES

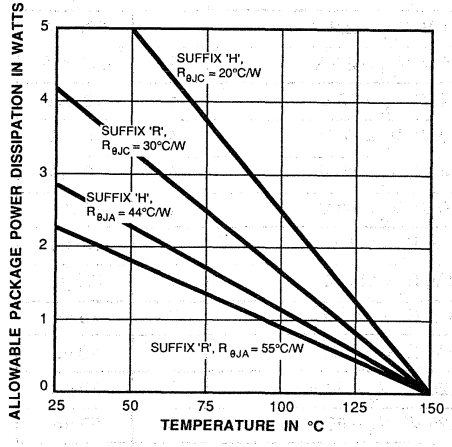
- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature -55°C to +125°C

Always order by complete part number, e.g., **UDS2981H883** .
See table on next page for differences between devices.

ONE OF EIGHT DRIVERS



Dwg. No. A-10,242B



Dwg. GM-003

Device Type	$V_{CE(MAX)}$	$V_{IN(MAX)}$	Applications
UDS2981H/R	50 V	15 V	TTL, DTL, 5 V CMOS
UDS2982H/R	50 V	30 V	6-15 V CMOS/PMOS
UDS2983H/R	80 V	15 V	TTL, DTL, 5 V CMOS
UDS2984H/R	80 V	30 V	6-15 V CMOS/PMOS

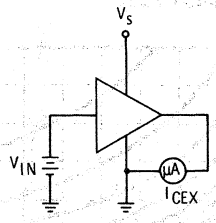
ELECTRICAL CHARACTERISTICS from -55°C to +125°C (unless otherwise specified).

Characteristic	Symbol	Applicable Devices†	Temp.	Test Conditions	Fig.	Limit
Maximum Output Leakage Current	I_{CEX}	UDS2981/82		V_{IN} = 0.25 V*, V_S = 50 V	1	200 µA
		UDS2983/84		V_{IN} = 0.25 V*, V_S = 80 V	1	200 µA
Maximum Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDS2981/83	-55°C	V_{IN} = 2.4 V, I_{OUT} = -100 mA	2	2.0 V
				V_{IN} = 2.4 V, I_{OUT} = -200 mA	2	2.1 V
			+25°C	V_{IN} = 2.4 V, I_{OUT} = -350 mA	2	2.0 V
			+125°C	V_{IN} = 2.4 V, I_{OUT} = -100 mA	2	1.8 V
				V_{IN} = 2.4 V, I_{OUT} = -200 mA**	2	1.9 V
		UDS2982/84	-55°C	V_{IN} = 5.0 V, I_{OUT} = -100 mA	2	2.0 V
				V_{IN} = 5.0 V, I_{OUT} = -200 mA	2	2.1 V
			+25°C	V_{IN} = 5.0 V, I_{OUT} = -350 mA	2	2.0 V
			+125°C	V_{IN} = 5.0 V, I_{OUT} = -100 mA	2	1.8 V
				V_{IN} = 5.0 V, I_{OUT} = -200 mA**	2	1.9 V
Maximum Input Current	$I_{IN(ON)}$	All		V_{IN} = 2.4 V	3	295 µA
				V_{IN} = 3.85 V	3	600 µA
				V_{IN} = 12 V	3	2.3 mA
	$I_{IN(OFF)}$	UDS2981/82		V_{IN} = 0 V, V_S = 50 V	3	10 µA
		UDS2983/84		V_{IN} = 0 V, V_S = 80 V	3	10 µA
Minimum Output Source Current	I_{OUT}	UDS2981/83		V_{IN} = 2.4 V, V_{CE} = 2.2 V	2	-200 mA
		UDS2982/84		V_{IN} = 5.0 V, V_{CE} = 2.2 V	2	-200 mA
Maximum Supply Current (Outputs Open)	I_S	UDS2981	+25°C	V_{IN} = 2.4 V*, V_S = 50 V	4	10 mA
		UDS2982		V_{IN} = 5.0 V*, V_S = 50 V	4	10 mA
		UDS2983		V_{IN} = 2.4 V*, V_S = 80 V	4	10 mA
		UDS2984		V_{IN} = 5.0 V*, V_S = 80 V	4	10 mA
Maximum Turn-ON Delay Time	t_{pHL}	UDS2981/82	+25°C	V_S = 35 V, R_L = 175 Ω	7	2.0 µs
		UDS2983/84		V_S = 50 V, R_L = 250 Ω	7	2.0 µs
Maximum Turn-OFF Delay Time	t_{pLH}	UDS2981/82	+25°C	V_S = 35 V, R_L = 175 Ω	7	10 µs
		UDS2983/84		V_S = 50 V, R_L = 250 Ω	7	10 µs
Maximum Clamp Diode Leakage Current	I_R	UDS2981/82		V_{IN} = 0.25 V*, V_S = 50 V	5	50 µA
		UDS2983/84		V_{IN} = 0.25 V*, V_S = 80 V	5	50 µA
Maximum Clamp Diode Forward Voltage	V_F	ALL		I_F = 200 mA	6	1.75 V

*All inputs simultaneously.
**Pulsed test.
†Complete part number includes a terminal letter that indicates package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

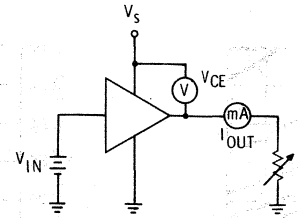
TEST FIGURES

Figure 1



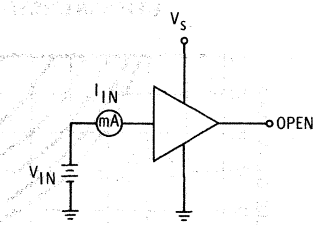
Dwg. No. A-11,083

Figure 2



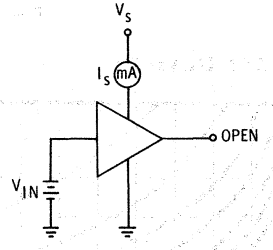
Dwg. No. A-11,084

Figure 3



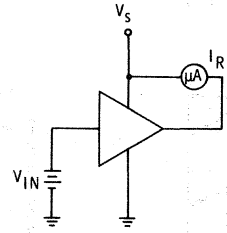
Dwg. No. A-11,085

Figure 4



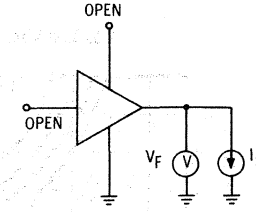
Dwg. No. A-11,086

Figure 5



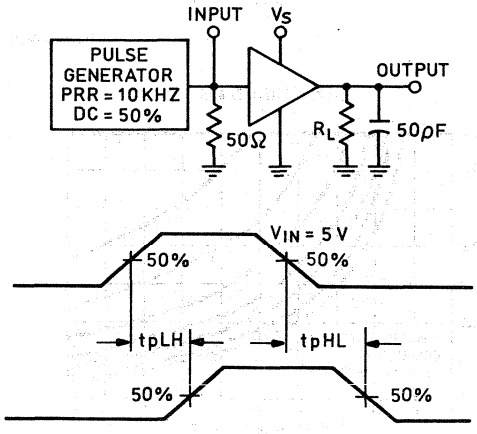
Dwg. No. A-11,087

Figure 6



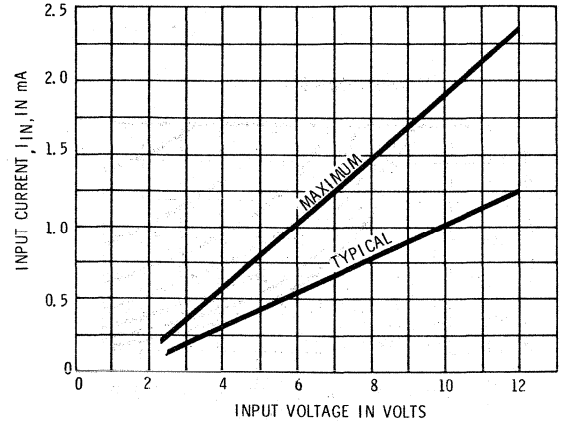
Dwg. No. A-11,088

Figure 7



Dwg. No. A-13,26A

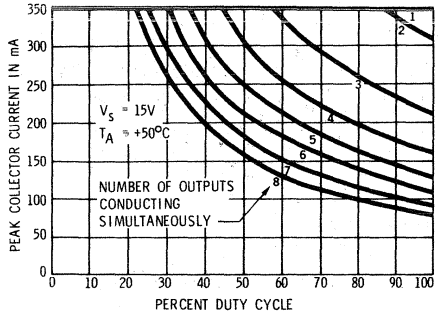
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



Dwg. No. A-11,115B

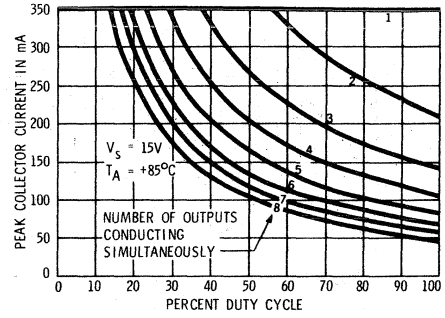
RECOMMENDED PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE
SERIES UDS2980H

UDS2981/82H



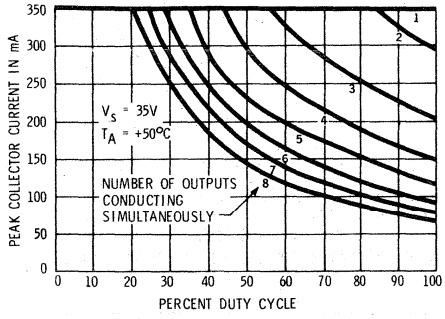
Dwg. No. A-11,078B

UDS2981/82H



Dwg. No. A-11,076B

ALL DEVICES



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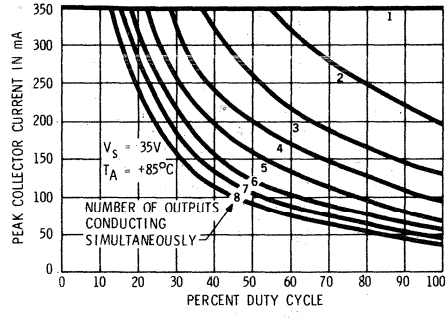
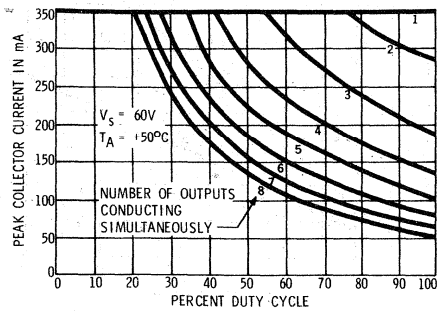


Dwg. No. A-11,080B

UDS2983/84H



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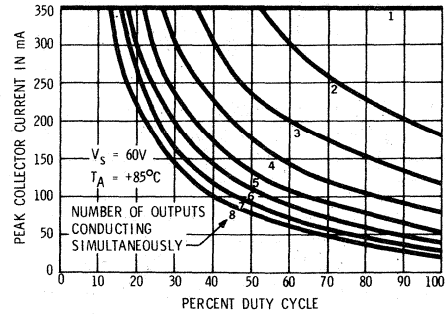
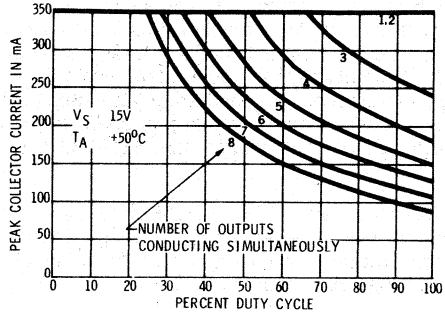


Dwg. No. A-11,081A

RECOMMENDED PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE
SERIES UDS2980R

UDS2981/82R



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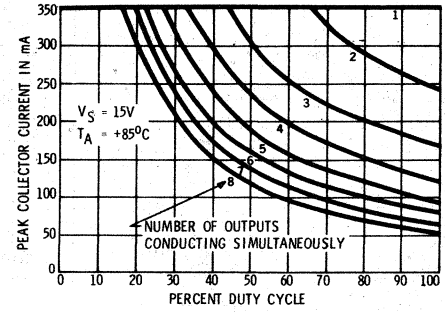
UDS2981/82R



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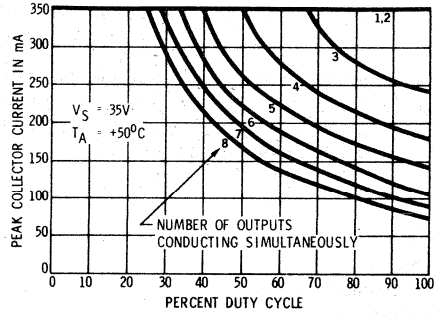

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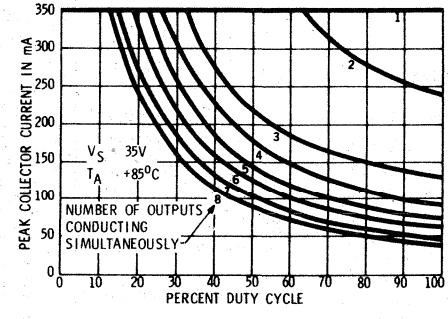

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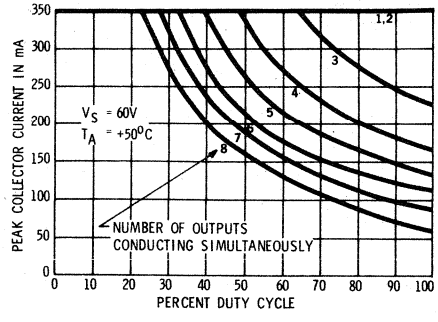
UDS2983/84R



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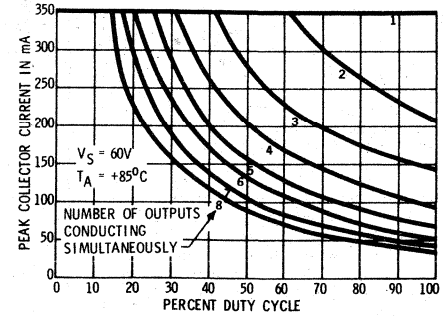
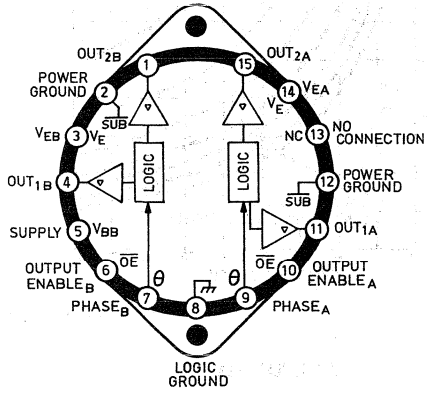
UDS2983/84R



Dwg. No. A-12,406

2998
MIL-STD-883 COMPLIANT

DUAL FULL-BRIDGE MOTOR DRIVER



Dwg. No. PM-003

ABSOLUTE MAXIMUM RATINGS

Motor Supply Voltage, V_{BB} . . . . . **50 V**
Output Current, I_{OUT} (300 ms) . . . . . **±2.2 A**
(Continuous) . . . . . **±1.8 A**
Sink Driver Emitter Voltage, V_E . . . . . **1.5 V**
Logic Input Voltage Range,
V_{IN} . . . . . **-0.3 V to +15 V***
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-55°C to + 125°C**
Junction Temperature,
T_J . . . . . **+150°C†**
Storage Temperature Range,
T_S . . . . . **-65°C to + 150°C**

*V_{IN} must not exceed V_{BB}.

†Fault conditions which produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

The UDS2998V dual full-bridge driver is designed for bidirectional operation of 2-phase stepper motors, a pair of dc servo motors, 2-phase brushless dc motors, or two solenoids at up to 50 V with continuous output currents to ±1.8 A per bridge or peak (start-up) currents to ±2.2 A. The control inputs are compatible with standard logic families. Except for a common supply voltage and thermal shutdown, the two drivers in a device are completely independent. Static burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

For external PWM control, an OUTPUT ENABLE for each bridge circuit is provided and the sink driver emitters are brought out for connection to external current-sensing resistors. A PHASE input to each bridge determines load-current direction.

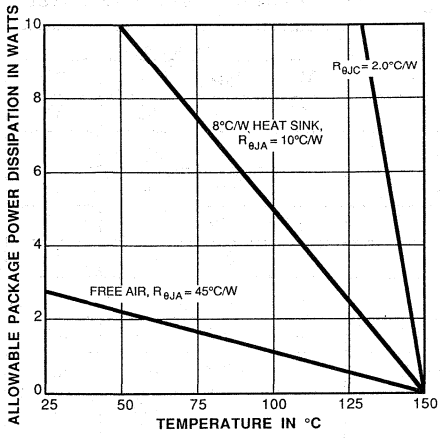
Extensive circuit protection is provided on-chip. Output suppression diodes protect the bridges from the transients generated when switching inductive loads. A thermal shutdown circuit disables all of the source drivers if chip temperature rating (package power dissipation) is exceeded. Internal delays provide protection against crossover currents (adjacent source and sink drivers conducting simultaneously) during switching intervals.

The UDS2998V is supplied in a 15-pin, flange-mount MO-097AA style hermetic package for improved power dissipation capabilities. An external heatsink is required for high-current applications. The flange is at ground potential and normally needs no isolation.

FEATURES

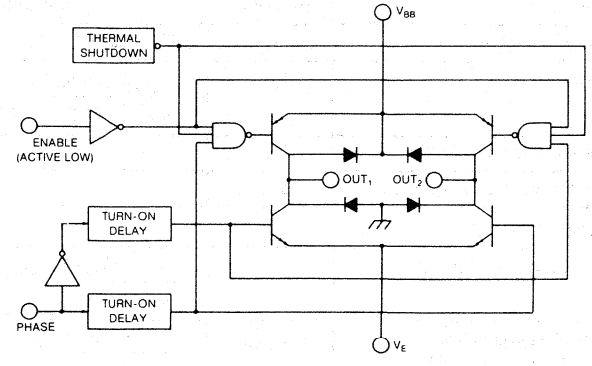
- ±1.8 A Output Current
- Output Voltage to 50 V
- Integral Output Suppression Diodes
- Output Current Sensing
- Logic Compatible Inputs
- Internal Thermal Shutdown Circuitry
- Crossover-Current Protected
- Hermetically Sealed Package
- High-Reliability Screening

Always order by complete part number: **UDS2998V883** .



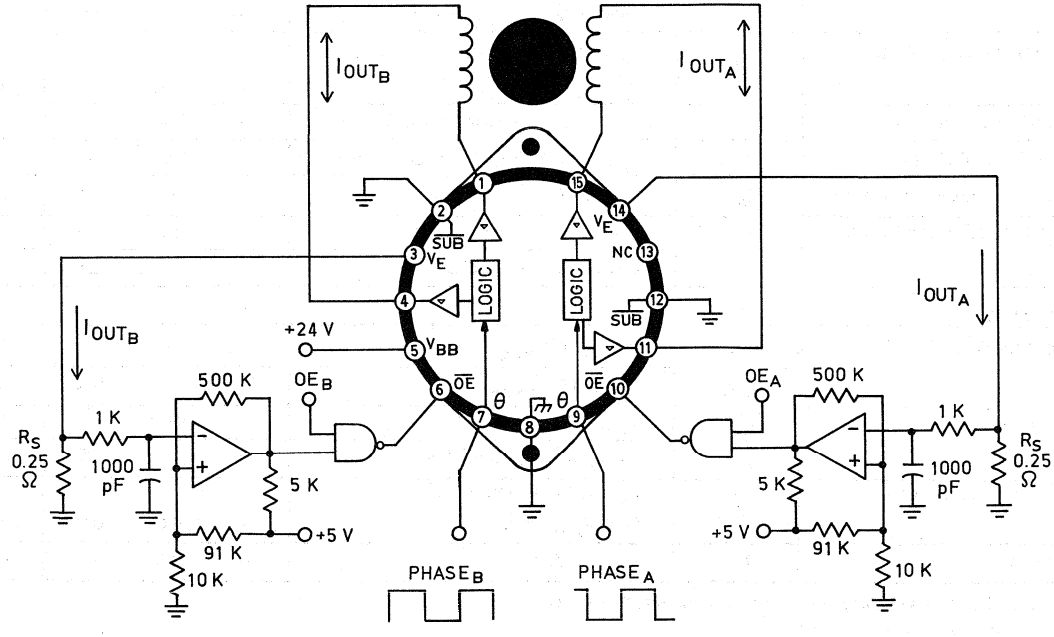
Dwg. GM-001

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. W-107A

TYPICAL APPLICATION
2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)



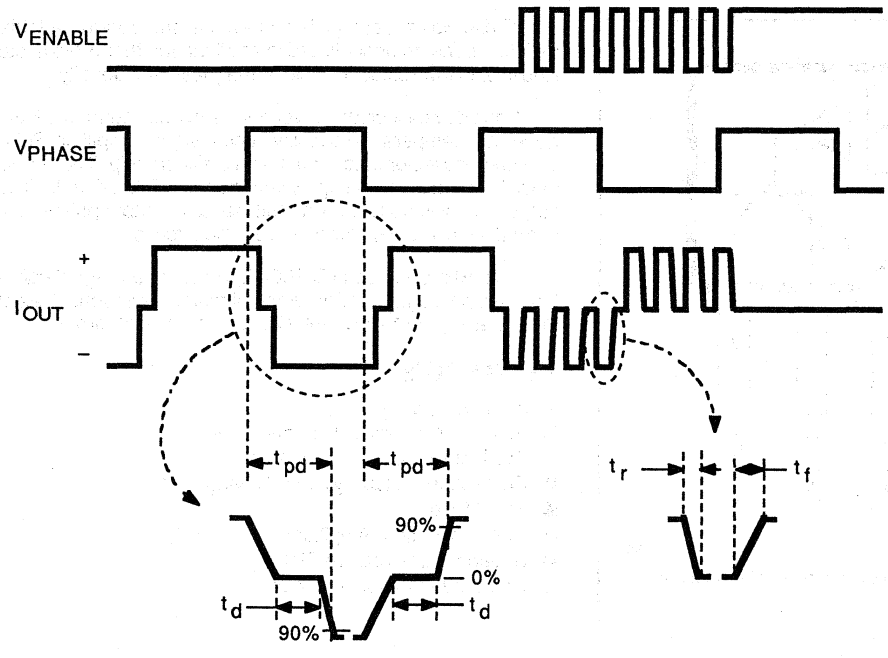
Dwg. EM-001

ELECTRICAL CHACTERISTICS at T_A = -55°C to +125°C, V_{BB} = 50 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	V_{BB}	Operating	10	—	50	V
Supply Current	I_{BB}	V_{ENABLE} (A & B) = 0.8 V, No Load	—	25	50	mA
		V_{ENABLE} (A & B) = 2.0 V, No Load	—	—	45	mA
Thermal Shutdown Temp.	T_J		—	175	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	25	—	°C
Output Drivers						
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$, V_{ENABLE} = 2.0 V, Note 3	—	<5.0	50	µA
		V_{OUT} = 0 V, V_{ENABLE} = 2.0 V, Note 3	—	<-5 0	-50	µA
Output Saturation Voltage (T_A = -55°C to + 25°C)	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -1.0 A	—	1.7	2.0	V
		Sink Driver, I_{OUT} = +1.0 A	—	1.2	1.5	V
		Source Driver, I_{OUT} = -1.8 A	—	2.0	2.4	V
		Sink Driver, I_{OUT} = +1.8 A	—	1.7	2.1	V
Output Saturation Voltage (T_A = +125°C)	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -1.0 A	—	—	1.8	V
		Sink Driver, I_{OUT} = +1.0 A	—	—	1.3	V
		Source Driver, I_{OUT} = -1.8 A	—	—	2.2	V
		Sink Driver, I_{OUT} = +1.8 A	—	—	1.9	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±1.8 A, L = 3.0 mH, T_A = +25°C, Note 3	50	—	—	V
Source Driver Rise Time	t_r	I_{OUT} = -1.8 A, Resistive Load, Note 3	—	500	—	ns
Source Driver Fall Time	t_f	I_{OUT} = -1.8 A, Resistive Load, Note 3	—	750	—	ns
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	<5.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 1.8 A, T_A = -55°C to +25°C	—	1.5	1.9	V
		I_F = 1.8 A, T_A = +125°C	—	—	2.1	V
Control Logic						
Logic Input Voltage	$V_{IN(1)}$	V_{PHASE} or V_{ENABLE}	2.0	—	—	V
	$V_{IN(0)}$	V_{PHASE} or V_{ENABLE}	—	—	0.8	V
Input Current	$I_{IN(1)}$	V_{PHASE} or V_{ENABLE} = 2.0 V	—	<1.0	10	µA
	$I_{IN(0)}$	V_{PHASE} or V_{ENABLE} = 0.8 V	—	-5.0	-25	µA
Propagation Delay Time	t_{pd}	I_{OUT} = ±1.8 A, Note 3, 50% V_{PHASE} to 90% I_{OUT}	—	4.0	8.0	µs
Deadtime	t_d	I_{OUT} = ±1.8 A	—	2.5	—	µs

NOTES: 1. Typical Data is for design information only and is at T_A = +25°C.
2. Each driver is tested separately.
3. Test is performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.4 V.
4. Negative current is defined as coming out of (sourcing) the specified device pin.

TIMING DEFINITIONS



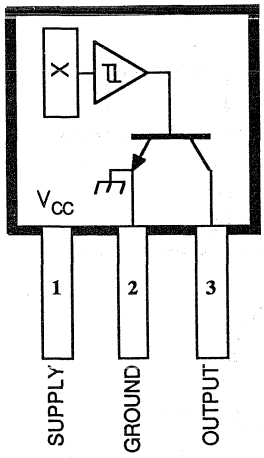
Dwg. WM-001

TRUTH TABLE

ENABLE INPUT	PHASE INPUT	OUTPUT 1	OUTPUT 2
Low	High	High	Low
Low	Low	Low	High
High	High	Open	Low
High	Low	Low	Open

SERIES 3100

HALL EFFECT SWITCHES



Dwg. PH-003

Pinning is shown viewed from branded side.

These Hall effect switches are highly temperature-stable and stress-resistant sensors best utilized in applications that provide steep magnetic slopes and low residual levels of magnetic flux density.

Each device includes a voltage regulator, quadratic Hall voltage generator, temperature stability circuit, signal amplifier, Schmitt trigger, and open-collector output on a single silicon chip. The on-board regulator permits operation with supply voltages of 4.5 to 24 volts. The switch output can sink up to 20 mA. With suitable output pull up, they can be used directly with bipolar or MOS logic circuits.

The 'HH' package (TO-260AA) provides a magnetically optimized hermetic package for military and similar applications. Selected devices, for operation to +170°C, are available on special order.

FEATURES

- 4.5 V to 24 V Operation
- Activate With Small, Commercially Available Permanent Magnets
- Solid-State Reliability... No Moving Parts
- Small Size
- Constant Output Amplitude
- Superior Temperature Stability
- Resistant to Physical Stress

ABSOLUTE MAXIMUM RATINGS

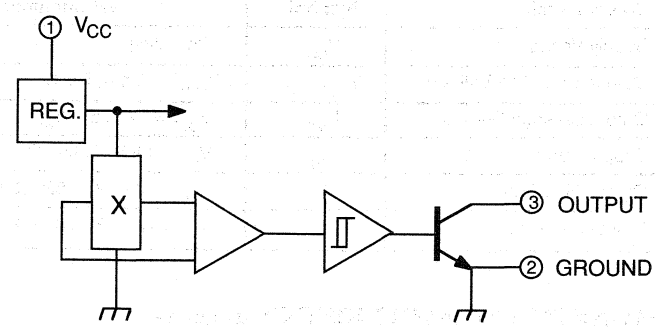
Supply Voltage, V_{CC} . . . . . **25 V**
Magnetic Flux Density, B . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . . **25 V**
Continuous Output Current, I_{OUT} . . . . **25 mA**
Operating Temperature Range,
T_A . . . . . **-40°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C***

* Devices can be stored at +200°C for short periods of time.

These devices are NON-COMPLIANT regarding MIL-STD-883C because of moisture resistance test method.

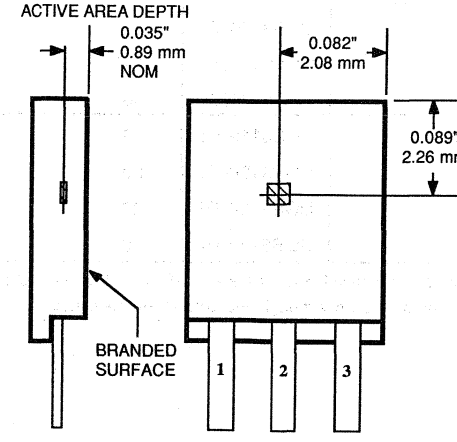
Always order by complete part number including prefix and suffix, e.g., **UGS3119HHMIL**. See Magnetic Characteristics table for differences between devices.

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-005

SENSOR LOCATION



Dwg. MH-013

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	150	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	<1.0	10	µA
Supply Current	I_{CC}	V_{CC} = 4.5 V, Output Open	—	4.7	8.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.04	2.0	µs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.18	2.0	µs

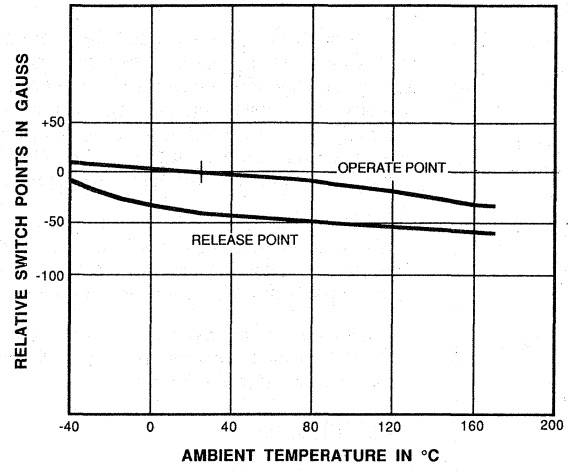
MAGNETIC CHARACTERISTICS in gauss

Characteristic	Part Number	T_A = +25°C		T_A = -20°C to +85°C*		T_A = -40°C to +125°C	
		Min.	Max.	Min.	Max.	Min.	Max.
Operate Point, B_{OP}	UGS3119HH	175	500	100	545	45	575
	UGS3120HH	70	350	70	425	35	450
	UGS3130HH	—	150	—	175	—	200
	UGS3140HH	70	200	45	260	45	270
Release Point, B_{RP}	UGS3119HH	125	450	50	495	25	555
	UGS3120HH	50	330	50	405	25	430
	UGS3130HH	-150	—	-175	—	-200	—
	UGS3140HH	50	180	25	240	25	250
Hysteresis, B_{hys}	UGS3119HH	50	—	50	—	20	—
	UGS3120HH	20	—	20	—	20	—
	UGS3130HH	20	—	20	—	20	—
	UGS3140HH	20	—	20	—	20	—

NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention).

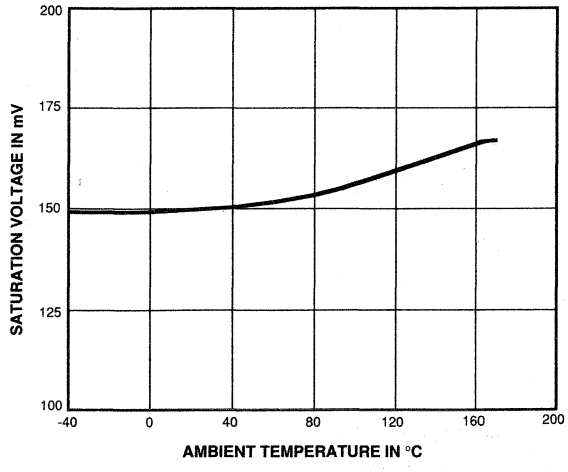
* These characteristics, although guaranteed, are not tested.

TYPICAL CHARACTERISTICS AS FUNCTIONS OF TEMPERATURE



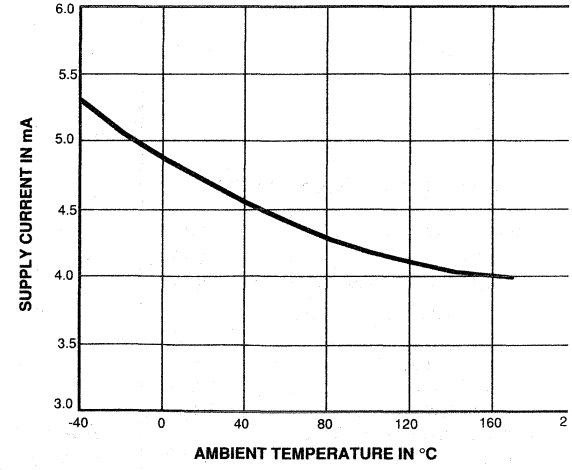
Dwg. GH-018

OUTPUT SATURATION VOLTAGE



Dwg. GH-013

SUPPLY CURRENT

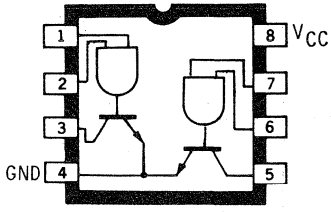


Dwg. GH-01

3611 THRU 3614

DUAL 2-INPUT PERIPHERAL/POWER DRIVERS

UDS3612H



Dwg. No. A-9793A

These mini-DIP dual 2-input peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 250 mA continuously at an ambient temperature of +75°C. In the OFF state, these drivers will withstand at least 80 V. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

The Series UDS3610H dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

With appropriate external diode transient suppression, Series UDS3610H drivers can also be used with inductive loads such as relays, solenoids, and stepping motors.

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Standoff Voltage of 80 V
- Hermetically Sealed Package
- High-Reliability Screening

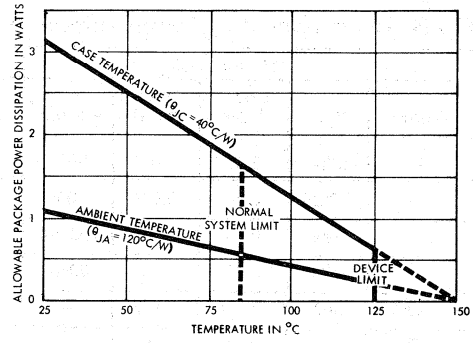
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **7.0 V**
Input Voltage, V_{IN} . . . . . **30 V**
Output Off-State Voltage, V_{OFF} . . . . . **80 V**
Output On-State Sink Current,
I_{ON} . . . . . **600 mA**
Power Dissipation, P_D
(One Output) . . . . . **1.0 W**
(Total Package) . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

These devices are NON-COMPLIANT regarding MIL-STD-883C because of package dimensions.

Always order by complete part number:

Part Number	Description
UDS3611H883	Dual AND Driver
UDS3612H883	Dual NAND Driver
UDS3613H883	Dual OR Driver
UDS3614H883	Dual NOR Driver



Dwg. No. A-10,978

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	-55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted

Characteristic	Symbol	Test Conditions			Limits				Notes
		V_{CC}	Driven Input	Other Input	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{IN(1)}$	MIN	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	MIN	—	—	—	—	0.8	V	—
"0" Input Current	$I_{IN(0)}$	MAX	0.4 V	30 V	—	-50	-100	µA	2
"1" Input Current	$I_{IN(1)}$	MAX	30 V	0 V	—	—	10	µA	2
Input Clamp Voltage	V_{IK}	MIN	-12 mA	—	—	—	-1.5	V	—

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts), C_l = 15 pF	—	200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts), C_L = 15 pF	—	300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

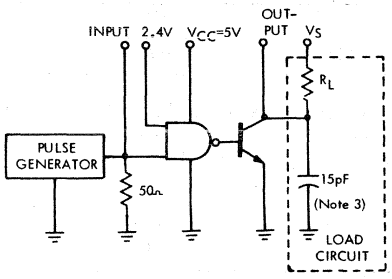
INPUT PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	$t_f \leq 7$ ns	t_p = 1 µs
$V_{IN(1)}$ = 3.5 V	$t_r \leq 14$ ns	PRR = 500 kHz

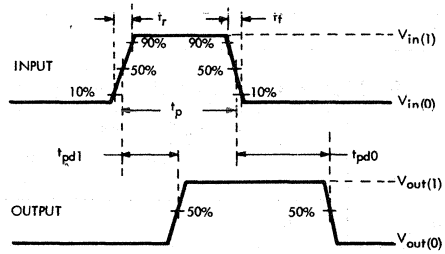
UDS3611H DUAL AND DRIVER
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	MIN	2.0 V	2.0 V	80 V	—	—	100	µA	—
		—	OPEN	2.0 V	2.0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	0.8 V	V_{CC}	150 mA	—	0.4	0.5	V	—
		—	MIN	0.8 V	V_{CC}	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V	—	—	8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V	—	—	35	49	mA	1, 2

NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.



Dwg. No. A-7876D



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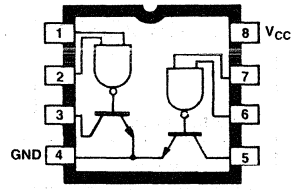
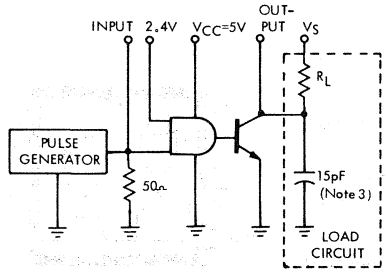


Dwg. No. A-9792A

UDS3612H DUAL NAND DRIVER
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise note

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	MIN	0.8 V	V_{CC}	80 V	—	—	100	µA	—
		—	OPEN	0.8 V	V_{CC}	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	2.0 V	2.0 V	150 mA	—	0.4	0.5	V	—
		—	MIN	2.0 V	2.0 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V	—	—	40	53	mA	1, 2

NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.



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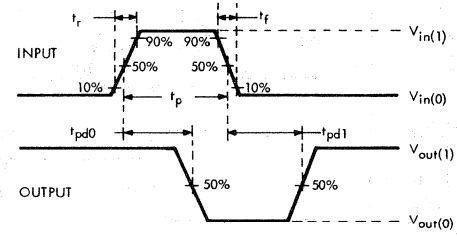

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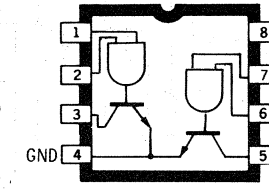
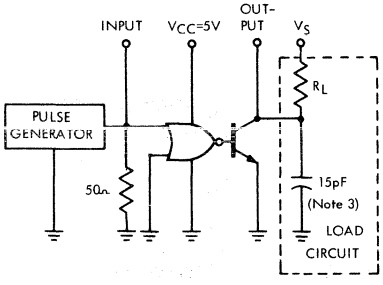


Dwg. No. A-979

UDS3613H DUAL OR DRIVER
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	MIN	2.0 V	0 V	80 V	—	—	100	µA	—
		—	OPEN	2.0 V	0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	0.8 V	0.8 V	150 mA	—	0.4	0.5	V	—
		—	MIN	0.8 V	0.8 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V	—	—	8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V	—	—	36	50	mA	1, 2

NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.



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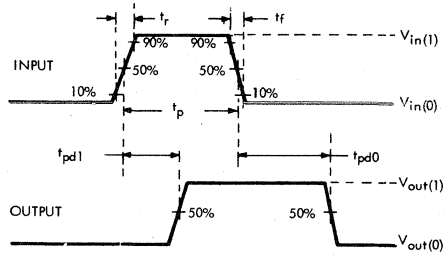

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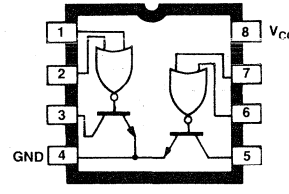
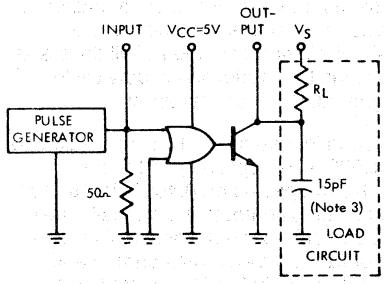


Dwg. No. A-9795A

UDS3614H DUAL NOR DRIVER
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise note

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	MIN	0.8 V	0.8 V	80 V	—	—	100	µA	—
		—	OPEN	0.8 V	0.8 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	2.0 V	0 V	150 mA	—	0.4	0.5	V	—
		—	MIN	2.0 V	0 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V	—	—	40	50	mA	1, 2

NOTES: 1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.



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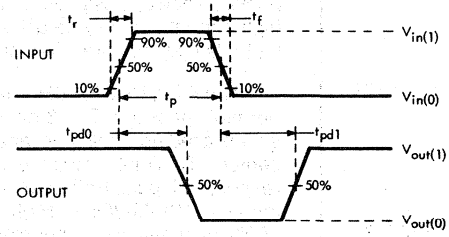

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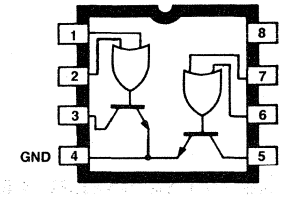
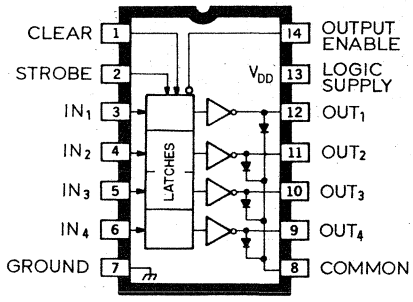


Dwg. No. A-97

5800 AND 5801
MIL-STD-883 COMPLIANT

BiMOS II LATCHED DRIVERS

UCS5800H



Dwg. No. A-10,499D

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . **50 V**
Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Collector Current,
I_C . . . . . **500 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Ambient Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Note: Output current rating may be limited by duty cycle, ambient temperature, air flow, and number of outputs conducting. Under any set of conditions, do not exceed a maximum junction temperature of +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Simplifying interface between LSI and peripheral power loads, the hermetically sealed UCS5800H (4-bit) and UCS5801H (8-bit) latched drivers combine the advantages of CMOS logic and control and high-voltage, high-current bipolar output buffers. Typical applications include microprocessor interface to relays, solenoids, dc and stepper motors, printers, LED or incandescent displays requiring hermetic packaging and an operating temperature range of -55°C to +125°C.

BiMOS II latched drivers have data input rates faster than those of the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors.

The Darlington open-collector outputs will drive power loads rated to 50 V and 350 mA (500 mA, maximum). Integral diodes for inductive load transient suppression are included. Because of limitations on package power dissipation, the simultaneous operation of all drivers at high current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load-current capability.

The 4-bit, UCS5800H is furnished in a standard 14-pin side-brazed hermetic package. The 8-bit, UCS5801H is supplied in a 22-pin side-brazed hermetic package with row spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs. Both packages conform to the dimensional requirements of MIL-M-38510. High-temperature reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

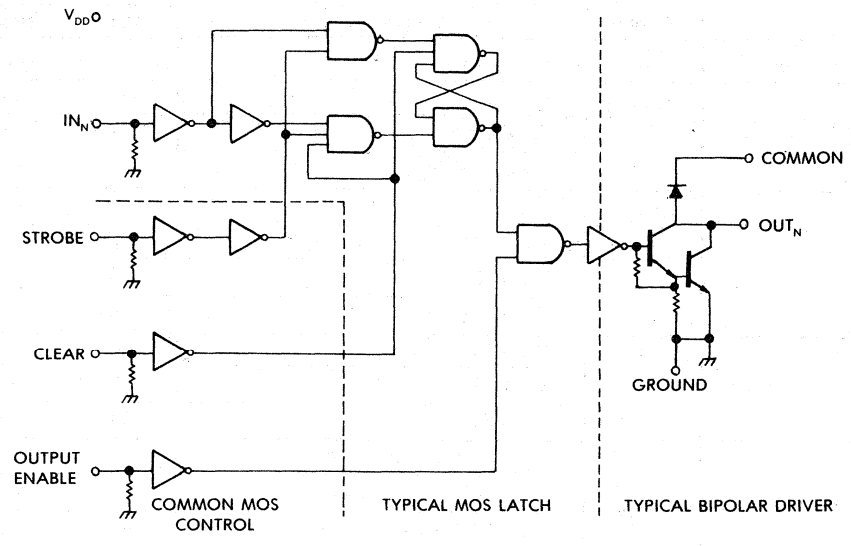
FEATURES

- 4.4 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Control and Latches
- High-Voltage, High-Current Outputs
- Transient-Protected Outputs
- Operating Temperature -55°C to +125°C
- High-Reliability Screening to MIL-STD-883, Class B

Always order by complete part number:

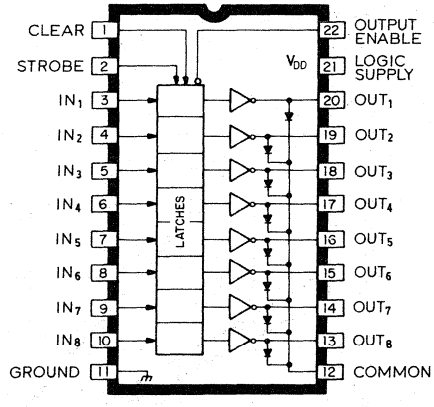
Part Number	Description
UCS5800H883	4-Bit Latched Driver
UCS5801H883	8-Bit Latched Driver

FUNCTIONAL BLOCK DIAGRAM



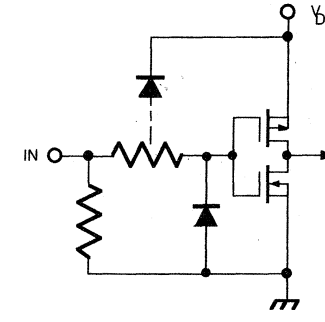
Dwg. No. A-10,495A

UCS5801H



Dwg. No. A-10,498D

TYPICAL INPUT CIRCUIT

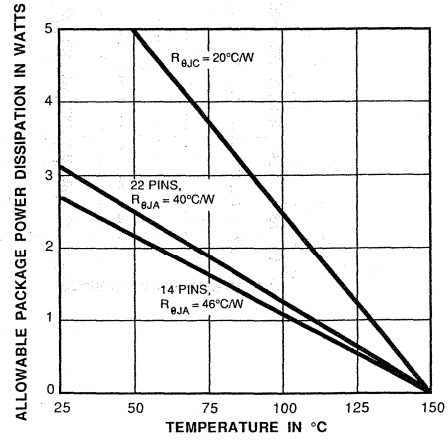


Dwg. EP-010-4

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.1	V
		I_C = 200 mA	—	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 10 V	8.5	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".



Dwg. GM-008

ELECTRICAL CHARACTERISTICS at T_A = -55°C, V_{DD} = 5 V (unless otherwise specified).

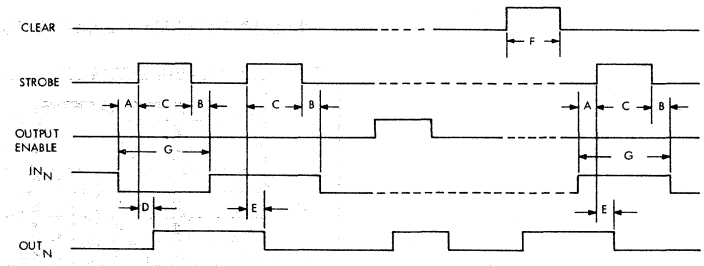
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.3	V
		I_C = 200 mA	—	1.5	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	11	—	V
		V_{DD} = 10 V	9.0	—	V
		V_{DD} = 5.0 V (See Note)	3.6	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	35	—	kΩ
		V_{DD} = 10 V	35	—	kΩ
		V_{DD} = 5.0 V	35	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.5	mA
		V_{DD} = 10 V, Outputs Open	—	2.1	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.1	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.3	V
		I_C = 200 mA	—	1.5	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 10 V	8.5	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".



Dwg. No. A-10,895A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . . **50 ns**
C. Minimum Strobe Pulse Width . . . . . **125 ns**
D. Typical Time Between Strobe Activation and Output On to Off Transition . . . . . **500 ns**
E. Typical Time Between Strobe Activation and Output Off to On Transition . . . . . **500 ns**
F. Minimum Clear Pulse Width . . . . . **300 ns**
G. Minimum Data Pulse Width. . . . . **225 ns**

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

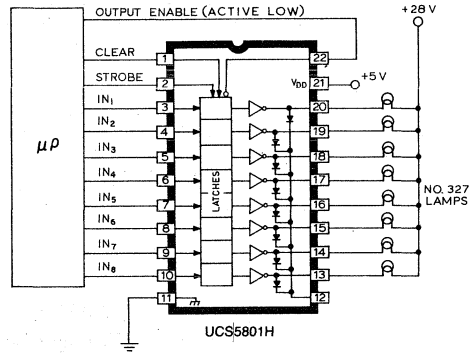
TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_{IN} t-1	OUT_{IN} t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant
t-1 = Previous Output State
t = Present Output State

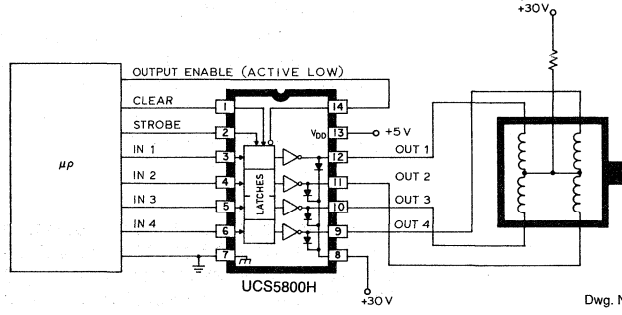
TYPICAL APPLICATIONS

INCANDESCENT LAMP DRIVER



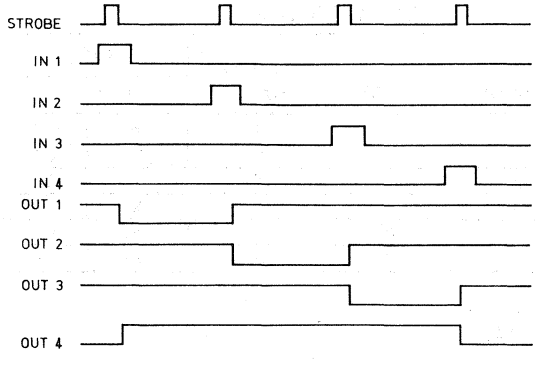
Dwg. No. 13,000A

UNIPOLAR STEPPER-MOTOR DRIVE



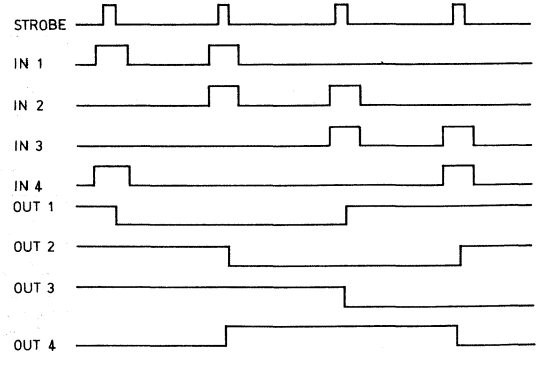
Dwg. No. 13,001A

UNIPOLAR WAVE DRIVE



Dwg. No. A-11,446

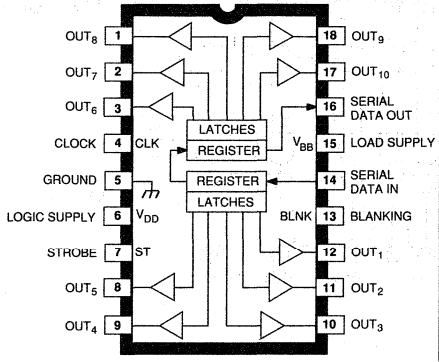
UNIPOLAR 2-PHASE DRIVE



Dwg. No. A-11,447

5810
MIL-STD-883 COMPLIANT

BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER



Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **60 V**
Logic Supply Voltage Range,
V_{DD} . . . . . **4.5 V to 15 V**
Driver Supply Voltage Range,
V_{BB} . . . . . **5.0 V to 60 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **-40 mA**
Package Power Dissipation, P_D **1.67W***
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

* Derate at 13.3 mW/°C above +25°C

Caution: This CMOS device has input static protection but is susceptible to damage when exposed to extremely high static electrical charges.

Combining low-power CMOS logic with bipolar source drivers, Type UCS5810H will simplify many display-system designs. Primarily intended for use with vacuum-fluorescent displays, this BiMOS 10-bit serial-input, latched driver can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS 10-bit shift register and associated latches are designed for operation over a 5 V to 15 V supply-voltage range. They cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low-speed TTL logic, appropriate pull-up resistors may be required to ensure an input logic high. A CMOS serial-data output allows cascading these devices for interface applications requiring many drive lines (dot matrix, alphanumeric, bargraph).

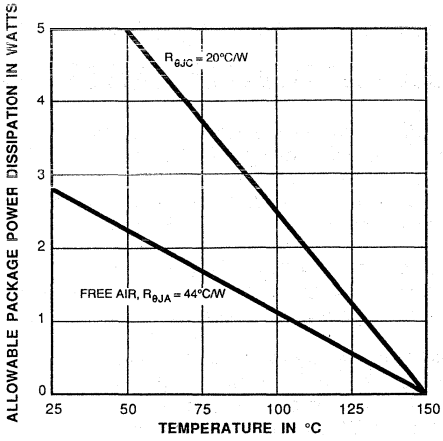
The 10 bipolar outputs are used as segment or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 85°C at a duty cycle of 83%. Other combinations of number of conducting outputs and duty cycle are shown in the specifications.

Type UCS5810H, when combined with the UCS5815H, an 8-bit latched source driver, comprises a minimum component display subsystem requiring few, if any, discrete components. The UCS5810H is furnished in an 18-pin hermetic dual in-line side-brazed package. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

FEATURES

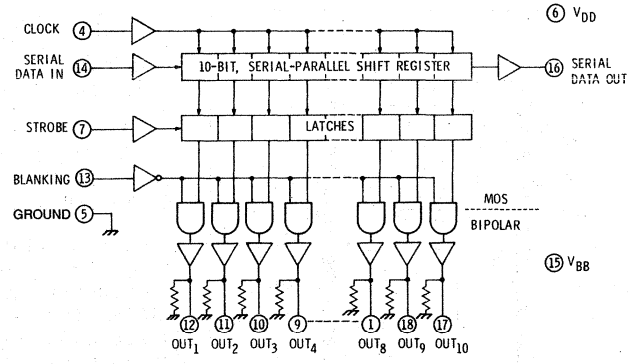
- 5 MHz Minimum Data Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature -55°C to +125°C

Always order by complete number: **UCS5810H883** .



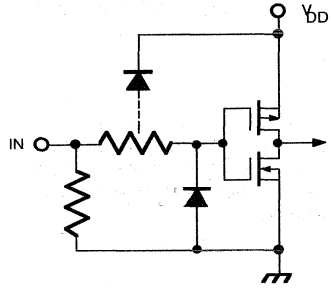
Dwg. GM-006

FUNCTIONAL BLOCK DIAGRAM



Dwg. No A-10,989A

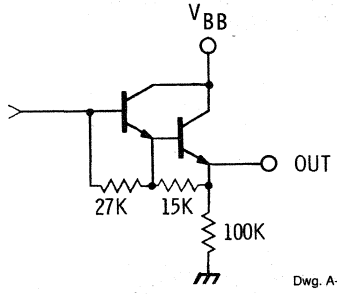
TYPICAL INPUT CIRCUIT



Dwg. EP-010-4

Number of Outputs ON (I_{OUT} = -25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of 85°C
10	83%
9	93%
8	100%
7	100%
6	100%
5	100%

TYPICAL OUTPUT DRIVER



Dwg. A-10,981C

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = -25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	µA
Output Leakage Current			—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 12 V	10.5	—	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN}$ = 5.0 V	—	100	µA
		$V_{DD} = V_{IN}$ = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	200	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL of DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at T_A = -55°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = -25 mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	µA
Output Leakage Current			—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.6	—	V
		V_{DD} = 12 V	11.0	—	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN}$ = 5.0 V	—	145	µA
		$V_{DD} = V_{IN}$ = 12 V	—	430	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	35	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, Outputs OFF, All Inputs = 0 V	—	100	µA
		V_{DD} = 12 V, Outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

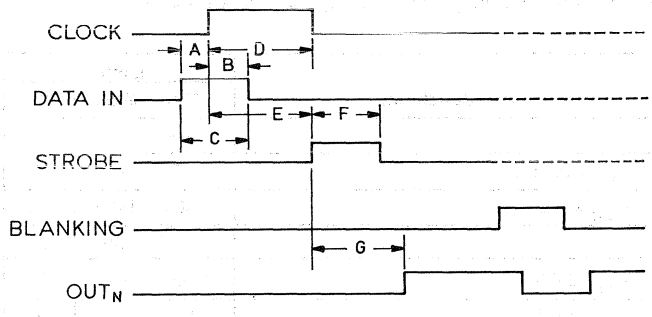
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL of DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = -25 mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	1400	µA
Output Leakage Current			—	-30	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 12 V	10.5	—	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN}$ = 5.0 V	—	100	µA
		$V_{DD} = V_{IN}$ = 12 V	—	300	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	27	kΩ
		V_{DD} = 12 V	—	8.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	15	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL of DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

5810
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER



Dwg. No. A-12,649

TIMING CONDITIONS

(V_{DD} = 5 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transition . . . . . **1.0 µs**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

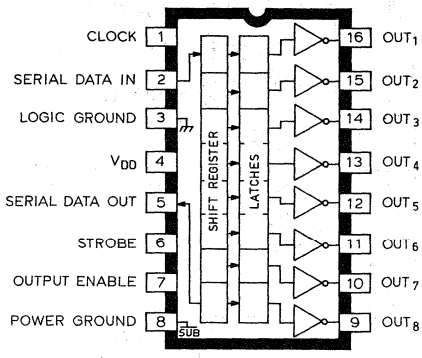
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⊓	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⊓	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⊔	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5822
MIL-STD-883 COMPLIANT

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVER



Dwg. PP-026

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **80 V**
Logic Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **500 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Intended for military, aerospace, and related applications. The UCS5822H 8-bit, serial-input, latched driver combines bipolar Darlington drivers with MOS logic circuitry (BiMOS) to provide an interface flexibility beyond the reach of standard logic buffers and power driver arrays.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Each driver contains a CMOS shift register and associated latches designed for operation over a 5 V to 15 V supply-voltage range. High-impedance inputs cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or Schottky TTL, appropriate pull-up resistors may be required to ensure an input-logic high. The CMOS serial-data output allows cascading these devices for interface applications requiring additional drive lines.

The eight high-current bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads. Under normal operating conditions, and without heat sinking, these devices can sustain 200 mA per output at 85°C at a 51% duty cycle. Other combinations of number of conducting outputs, temperature, and duty cycle are shown on the following page.

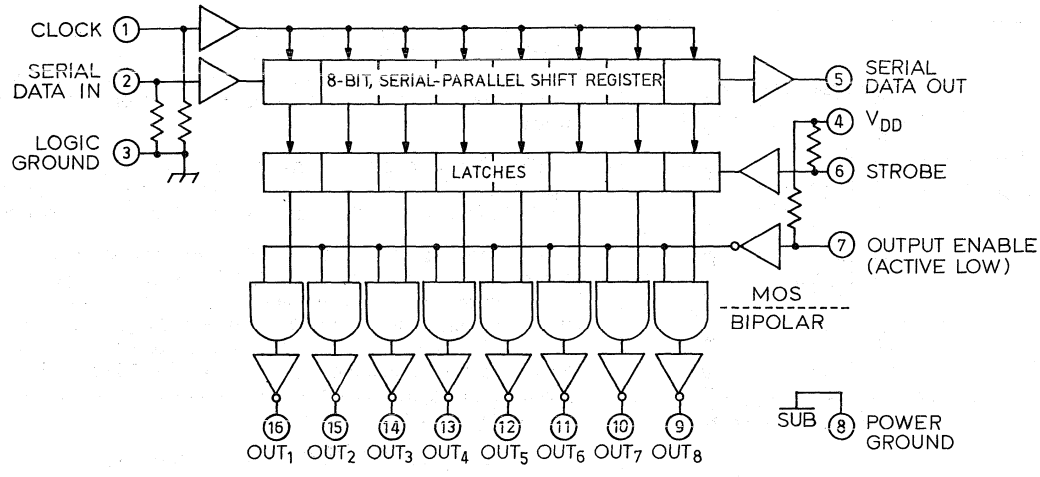
The UCS5822H is furnished in 16-pin side-brazed dual in-line hermetic packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

FEATURES

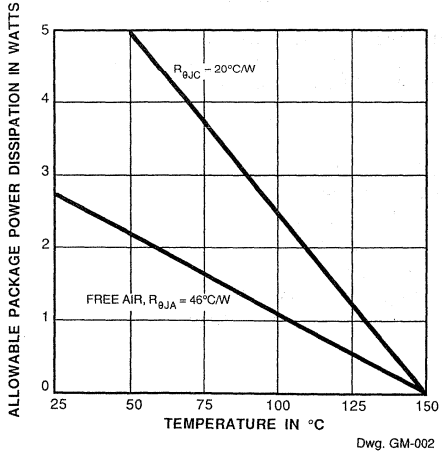
- 3.3 MHz Minimum Data Input Rate
- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

Always order by complete part number: **UCS5822H883**.

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-013



Dwg. GM-002

Number of Outputs ON (I_{OUT} = 200 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of 85°C
8	51%
7	58%
6	70%
5	84%
4	100%
3	100%
2	100%
1	100%

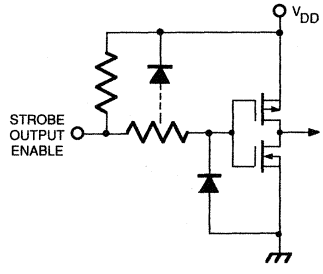
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 80 V	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA	—	1.1	V
		I_{OUT} = 200 mA	—	1.3	V
		I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 5.0 V (see note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{STROBE} = V_{DD} = 12 V	—	4.5	mA
		One Driver ON, V_{STROBE} = V_{DD} = 10 V	—	3.9	mA
		One Driver ON, V_{STROBE} = V_{DD} = 5.0 V	—	2.4	mA
	$I_{DD(OFF)}$	V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0 V	—	1.6	mA
		V_{ENABLE} = V_{STROBE} = V_{DD} = 12 V	—	2.9	mA

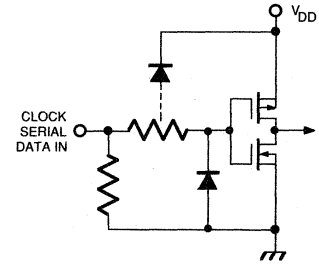
* Pulsed test.

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

TYPICAL INPUT CIRCUITS

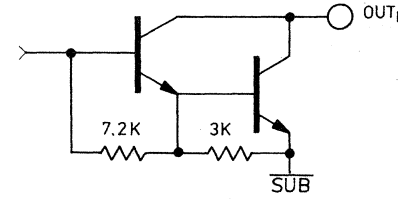


Dwg. EP-010-3



Dwg. EP-010-4

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,314

ELECTRICAL CHARACTERISTICS at T_A = -55°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 80 V	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA	—	1.3	V
		I_{OUT} = 200 mA	—	1.5	V
		I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 5.0 V (see note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	35	—	kΩ
		V_{DD} = 10 V	35	—	kΩ
		V_{DD} = 5.0 V	35	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{STROBE} = V_{DD} = 12 V	—	5.5	mA
		One Driver ON, V_{STROBE} = V_{DD} = 10 V	—	4.5	mA
		One Driver ON, V_{STROBE} = V_{DD} = 5.0 V	—	3.0	mA
	$I_{DD(OFF)}$	V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0 V	—	2.0	mA
		V_{ENABLE} = V_{STROBE} = V_{DD} = 12 V	—	3.5	mA

* Pulsed test.

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

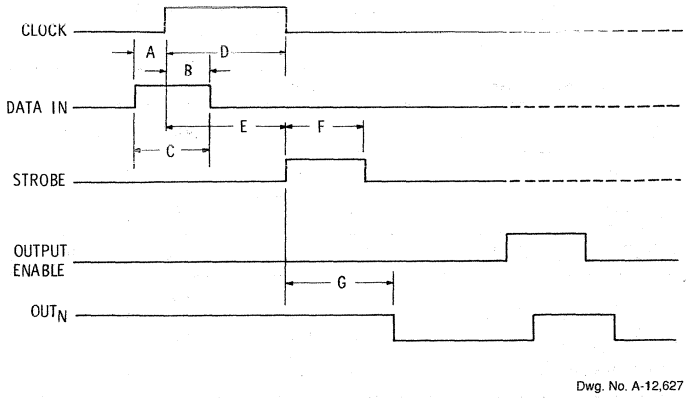
ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 80 V	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA*	—	1.3	V
		I_{OUT} = 200 mA*	—	1.5	V
		I_{OUT} = 350 mA*, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 5.0 V (see note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{STROBE} = V_{DD} = 12 V	—	4.5	mA
		One Driver ON, V_{STROBE} = V_{DD} = 10 V	—	3.9	mA
		One Driver ON, V_{STROBE} = V_{DD} = 5.0 V	—	2.4	mA
	$I_{DD(OFF)}$	V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0 V	—	1.6	mA
		V_{ENABLE} = V_{STROBE} = V_{DD} = 12 V	—	2.9	mA

* Pulsed test.

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

5822
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVER



Dwg. No. A-12,627

TIMING CONDITIONS
(V_{DD} = 5.0 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
C. Minimum Data Pulse Width ..... **150 ns**
D. Minimum Clock Pulse Width ..... **150 ns**
E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
F. Minimum Strobe Pulse Width ..... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition ..... **1.0 µs**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

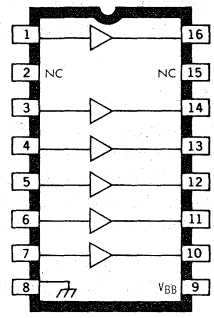
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⊥	H R_1 R_2 ..... R_7	R_7				
L	⊥	L R_1 R_2 ..... R_7	R_7				
X	⊤	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

6118
MIL-STD-883 COMPLIANT

FLUORESCENT DISPLAY DRIVER



Dwg. No. A-9641A

Consisting of eight NPN Darlington output stages and associated common-emitter input stages, the UDS6118H interfaces between low-level logic and vacuum fluorescent displays. It is furnished in an 18-pin hermetic dual in-line side-brazed package. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

Representative electrical characteristics (over an ambient temperature range of -20°C to +85°C) for the commercial type UDN6118A are shown in Section 3. Complete, detailed technical information on the UDS6118H is available on request.

FEATURES

- Digit or Segment Driver
- Low Input Current
- Integral Output Pull-Down Resistors
- High Output Breakdown Voltage
- Single or Split Supply Operation

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{BB} . . . . . **85 V**
Input Voltage, V_{IN} . . . . . **20 V**
Output Current, I_{OUT} . . . . . **-40 mA**
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**

Caution: The high input impedance of this device makes it susceptible to static discharge damage associated with handling and testing. Techniques similar to those used for handling MOS devices should be employed.

Always order by complete part number: **UDS6118H883** .

MILITARY PRODUCT STANDARDS

POWER AND HALL EFFECT ICs FOR MILITARY APPLICATIONS

High-reliability monolithic integrated circuits for a variety of military applications are available. Standard power ICs and Hall effect sensor ICs, to appropriate military specifications, provide product assurance and standardization to meet varying customer requirements. The manufacturing facilities used to produce these devices are all fully qualified for Class B microcircuits.

MIL-M-38510

The general specification for military microcircuits is MIL-M-38510. This specification is intended to support government microcircuit applications and logistic programs. It establishes the general requirements for monolithic integrated circuits and the quality assurance and reliability standards required in the acquisition of microcircuits.

Many of the devices previously furnished under MIL-M-38510 are now supplied as part of the Standardized Military Drawing Program or as MIL-STD-883 compliant products.

STANDARDIZED MILITARY DRAWING PROGRAM

The Standardized Military Drawing Program (SMDP) provides standardization when a MIL-M-38510 detail drawing (slash sheet) does not exist or certain offshore manufacturing facilities are used. This program directly replaces the original DESC drawing system (see Part Number Descriptions in Section 1).

MIL-STD-883

This standard establishes uniform methods, controls, and procedures for designing, testing, identifying, and certifying microelectronic devices suitable for use within military or aerospace electronic systems. It includes basic environmental tests, physical and electrical tests, design, package and material constraints, general marking requirements, and workmanship and training procedures.

A full line of integrated circuits are available that are fully compliant with the latest issue of MIL-STD-883. These devices are identified by adding the suffix "883" to the device part number. If, for any reason, a device is not fully compliant (usually because of special packaging), the suffix "MIL" is used instead.

APPLICATIONS INFORMATION

BiMOS II POWER DRIVER TO MIL-STD-883

BiMOS monolithic smart power drivers combine CMOS logic and control functions with bipolar and/or DMOS power drivers. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL, LSTTL, or DTL circuits may require appropriate pull-up resistors to ensure a logic high. The power driver outputs are used with VF, LED, and incandescent displays, dc and stepper motors, relays, solenoids, and thermal or electrosensitive print heads. With BiMOS integrated circuit, reliable, single-chip solutions are provided for a wide variety of peripheral power interface problems.

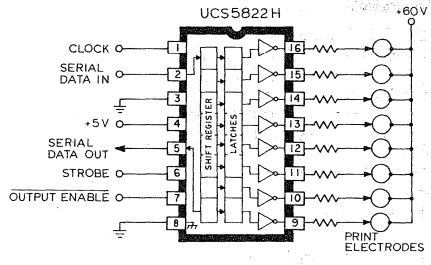
The high-current and high-voltage BiMOS drivers shown here are processed to MIL-STD-883. They furnish a higher level of interface flexibility and versatility for military, aerospace, avionics, than is provided with standard logic or discrete power drivers. They are supplied in ceramic/metal side-brazed hermetic packages (suffix letter "H"). All devices are rated for operation over the full military temperature range of -55°C to +125°C.

8-BIT SERIAL-INPUT/PARALLEL-OUTPUT LATCHED DRIVER

The UCS5822H BiMOS 8-Bit Serial-In/Parallel-Out Latched Driver augments the UCS5800H and UCS5801H devices. It contains an octal shift register, octal latch, and octal high-current, open-collector Darlington outputs. It improves system designs through a reduced package count and a reduction in I/O line requirements. By using the serial data output, the driver can be cascaded for interface applications requiring more than eight drive lines.

The bipolar outputs are suitable for a variety of peripheral loads, including incandescent lamps, LEDs, and thermal or electrosensitive printers.

ELECTROSENSITIVE PRINTER

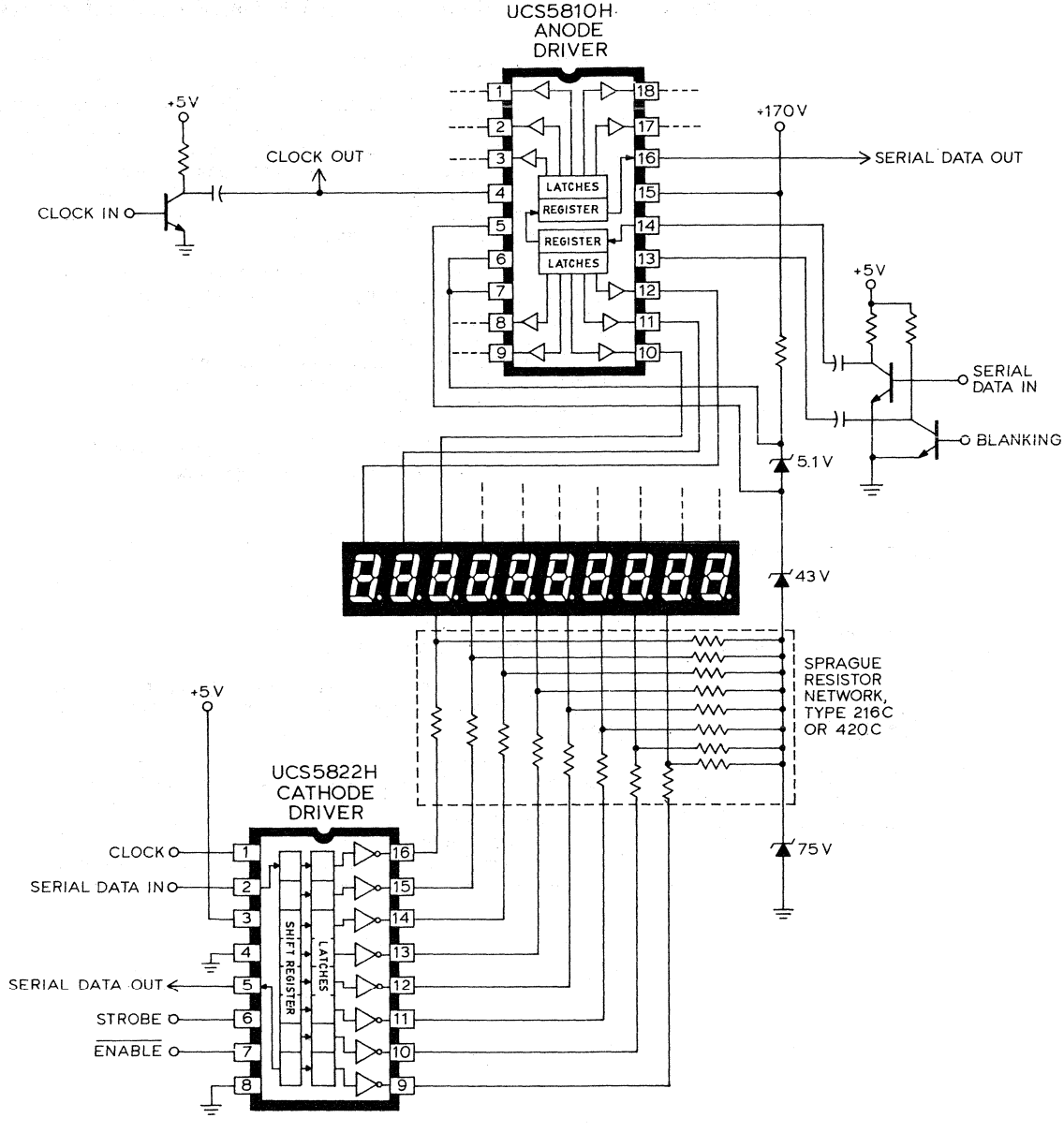


Dwg. No. A-14,188

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Output Voltage	**75 V**
Logic Supply Voltage	**12 V**
Continuous Output Current	**350 mA**

PLANAR GAS-DISCHARGE DISPLAY DRIVER



Dwg. No. A-14,189

BiMOS II POWER DRIVERS TO MIL-STD-883

4- AND 8-BIT LATCHED DRIVERS

The UCS5800H and UCS5801H are evolutionary improvements to the original BiMOS integrated circuits. They are used successfully in many applications. These high-voltage, high-current latched drivers have four or eight MOS data latches, a bipolar driver for each latch, and MOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Type UCS5800H contains four latched drivers while the UCS5801H contains eight latched drivers.

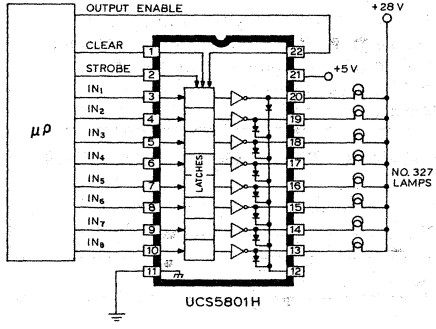
Each of the open-collector Darlington outputs can sink up to 500 mA and will sustain at least 50 V in the OFF state. Internal diodes suppress transients and allow these devices to be used with inductive loads. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximum current, and usually dictate either a reduction in output current or a suitable combination of duty cycle and number of active outputs.

The UCS5800H is supplied in a standard 14-lead side-brazed hermetic package. The UCS5801H is furnished in a 22-lead side-brazed hermetic package with lead centers on 0.400-inch spacing.

RECOMMENDED MAXIMUM OPERATING CONDITIONS

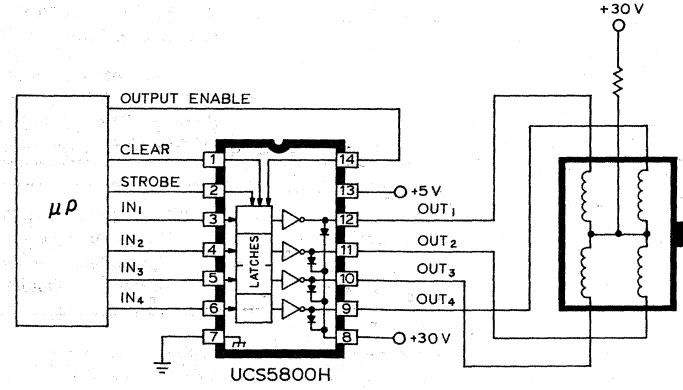
Output Voltage	**45 V**
Logic Supply Voltage	**12 V**
Continuous Output Current	**350 mA**

INCANDESCENT LAMP DRIVER



Dwg. No. A-11,743A

UNIPOLAR BIFILAR MOTOR DRIVE



Dwg. No. B-1491A

10-BIT SERIAL-INPUT/PARALLEL-OUTPUT LATCHED SOURCE DRIVER

The UCS5810H BiMOS 10-Bit Serial-In/Parallel-Out Latched Source Driver is primarily designed as interface between logic circuitry and vacuum-fluorescent displays, but may also be used with LED displays or thermal printers within its output limitations of 60 V and -40 mA per driver.

The CMOS shift register and latches will operate over a wide supply-voltage range and is compatible with standard MOS logic families. When used with TTL or low-speed TTL, pull-up resistors may be needed to ensure an input-logic high.

The 10 high-voltage outputs are used to switch the anodes (segments or dots) and/or grids (character or digit) of typical vacuum-fluorescent panels.

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Output Voltage.....**55 V**
Logic Supply Voltage.....**5.0 V to 12 V**
Continuous Output Current.....**-25 mA**

8-BIT LATCHED SOURCE DRIVER

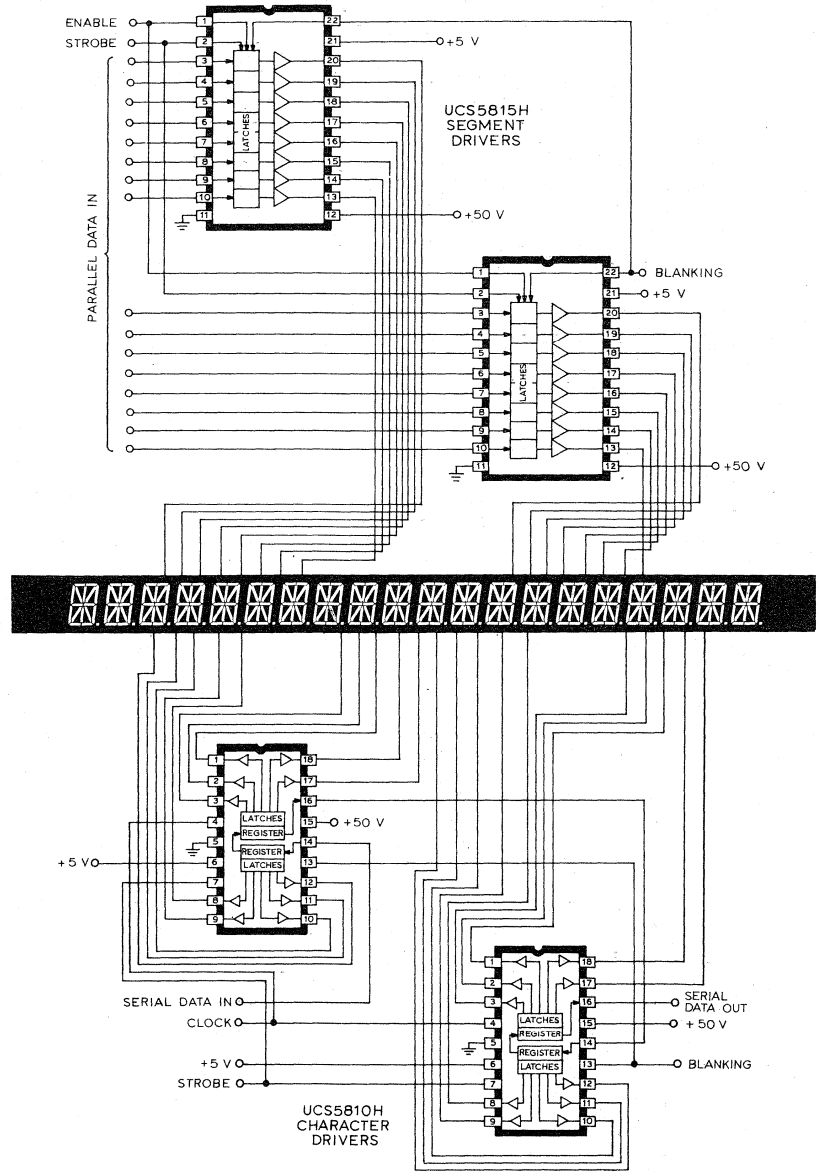
The UCS5815H BiMOS 8-Bit Latched Source Driver is designed primarily for use with high-voltage vacuum-fluorescent displays. It contains an 8-bit type D latch and eight source outputs with pull-down resistors, a common strobe, blanking, and enable functions.

The eight high-voltage outputs are generally used to drive the segments, dots (matrix panel), bars, or digits of vacuum-fluorescent displays. The UCS5815H is often used in combination with the UCS5810H 10-Bit Serial Input, Latched Driver.

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Output Voltage.....**55 V**
Logic Supply Voltage.....**5.0 V to 12 V**
Continuous Output Current.....**-25 mA**

ALPHANUMERIC VACUUM-FLUORESCENT DISPLAY DRIVERS



Dwg. No. C-1272A

GENERAL INFORMATION & PRODUCT INDEX 1

PRODUCT SELECTION GUIDES 2

PERIPHERAL POWER & DISPLAY DRIVER ICs 3

HALL-EFFECT & OPTOELECTRONIC SENSOR ICs 4

INTEGRATED CIRCUITS to MIL-STD-883 5

AUTOMOTIVE, SIGNAL-PROCESSING, & CONSUMER ICs 6

DISCRETE TRANSISTORS, DIODES, & ARRAYS 7

QUALITY & RELIABILITY INFORMATION 8

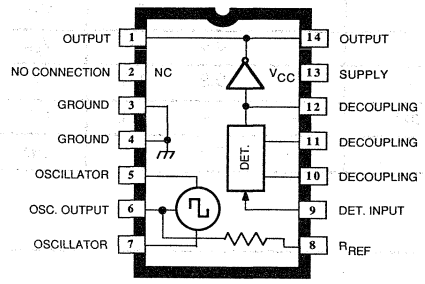
PACKAGE INFORMATION 9

SECTION 6. TECHNICAL DATA
for Automotive, Signal-Processing, and Consumer ICs

in Numerical Order ..... Beginning at 6-1

2429

FLUID DETECTOR



Dwg. PS - 017

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}
- (continuous) . . . . . **-50 V to +16 V**
- (1 hr. at +25°C) . . . . . **24 V**
- (10 µs) . . . . . **50 V**

Output Voltage, V_{OUT}
- (ULN2429A) . . . . . **30 V**
- (ULN2429A -1) . . . . . **50 V**

Output Current, I_{OUT}
- (continuous) . . . . . **700 mA**
- (1 hr. at +25°C) . . . . . **1.0 A**

Package Power Dissipation, P_D . . . . **1.33 W***

Operating Temperature Range,
- T_A . . . . . **-40°C to +85°C**

Storage Temperature Range,
- T_S . . . . . **-65°C to +150°C**

* Derate at the rate of 16.67 mW/°C above T_A = +70°C.

Primarily designed for use as an automotive low coolant detector, the ULN2429A monolithic bipolar integrated circuit is ideal for detecting the presence or absence of many different types of liquids in automotive, home, or industrial applications. Especially useful in harsh environments, reverse voltage protection, internal voltage regulation, temperature compensation, and high-frequency noise immunity are all incorporated in the design.

A simple probe, immersed in the fluid being monitored, is driven with an ac signal to prevent plating problems. The presence, absence, or condition of the fluid is determined by comparing the loaded probe resistance with an internal (pin 8) or external (pin 6) resistance. Typical conductive fluids which can be sensed are tap water, sea water, weak acids and bases, wet soil, wine, beer, and coffee. Non-conductive fluids include most petroleum products, distilled water, dry soil, and vodka. The probe can be replaced with any variable-resistance element such as a photodiode or photoconductive cell, rotary or linear position sensor, or thermistor for detecting solids, non-conducting liquids, gases, etc.

The high-current output is typically a square wave signal for use with an LED, incandescent lamp, or loudspeaker. A capacitor can be connected (pin 12) to provide a dc output for use with inductive loads such as relays and solenoids.

The ULN2429A is rated for operation with a load voltage of up to 30 volts. Selected devices, for operation up to 50 V are available as the ULN2429A-1. In all other respects, the ULN2429A and the ULN2429A-1 fluid detectors are identical.

These devices are furnished in an improved 14-lead dual in-line plastic package with a copper alloy lead frame for superior thermal characteristics. However, in order to realize the maximum current-handling capability of these devices, both of the output pins (1 and 14) and both ground pins (3 and 4) should be used.

FEATURES

- High Output Current
- AC or DC Output
- Single-Wire Probe
- Low External Parts Count
- Internal Voltage Regulator
- Reverse Voltage Protection

Always orderby complete part number:

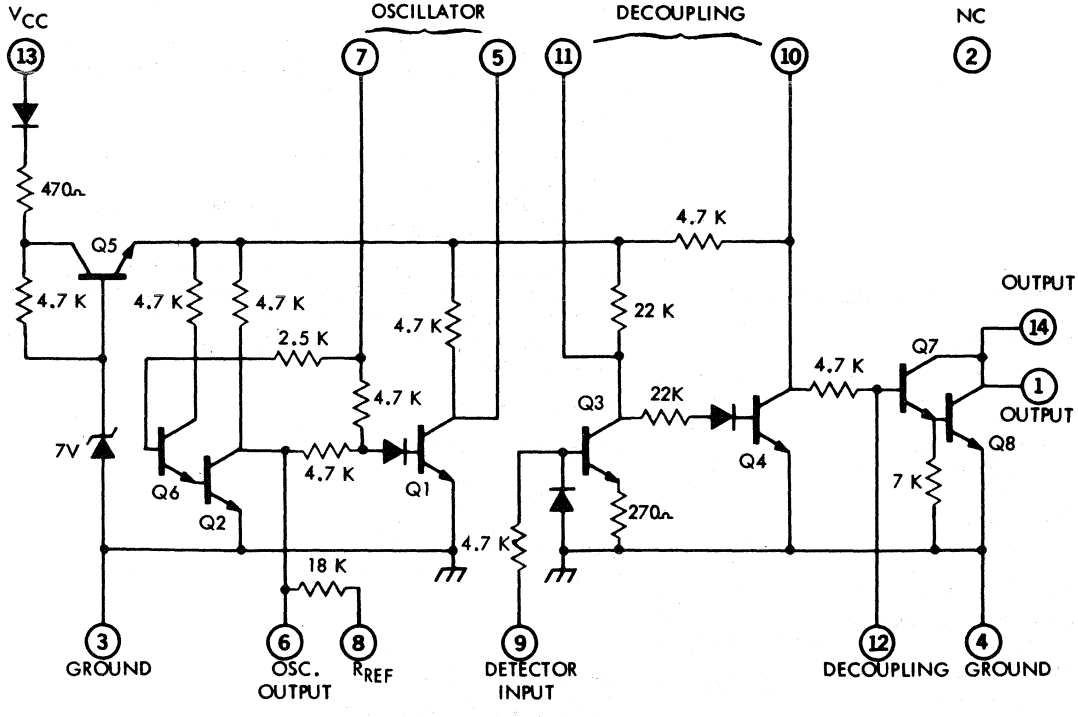
Part Number	Maximum V_{OUT}
ULN2429A	30 V
ULN2429A-1	50 V

2429
FLUID DETECTOR

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{OUT} = 12 V (unless otherwise specified).

Characteristic	Symbol	Test Pin	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	13	Operating	10	—	16	V
Supply Current	I_{CC}	13	V_{CC} = 16 V	—	—	10	mA
Oscillator Output Voltage	V_{OSC}	6	R_L = 18 kΩ	—	3.0	—	V_{PP}
Output ON Voltage	V_{OUT}	1, 14	$R_L \geq$ 30 kΩ, I_{OUT} = 500 mA	—	0.9	1.5	V
Output OFF Current	I_{OUT}	1, 14	$R_L \leq$ 10 kΩ, V_{OUT} = V_{OUT}(max)	—	—	100	µA
Oscillator Frequency	f_{OSC}	6	R_L = 18 kΩ	—	2.4	—	kHz

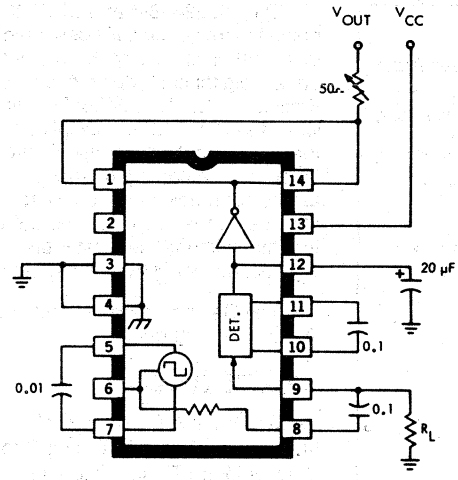
CIRCUIT SCHEMATIC



Dwg. No. A-10,825

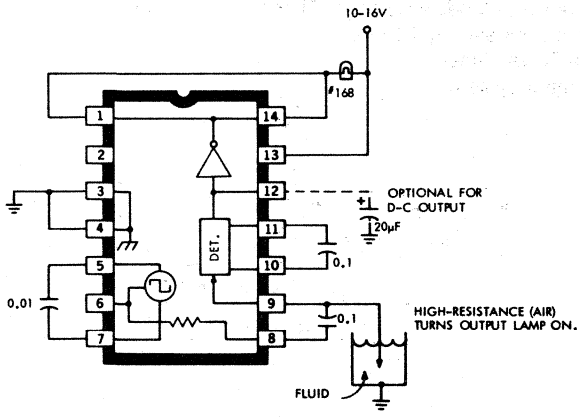
2429
FLUID DETECTOR

TEST CIRCUIT

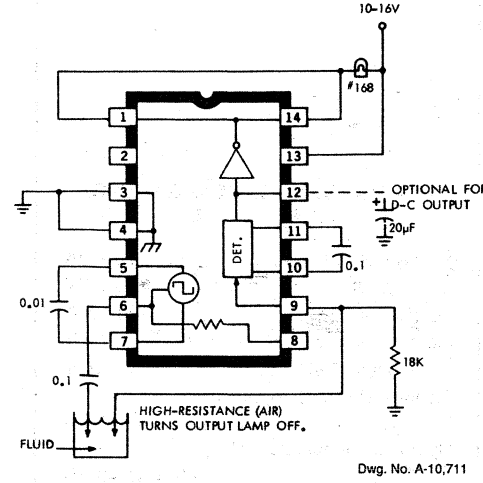


Dwg. No. A-10,707

TYPICAL APPLICATIONS



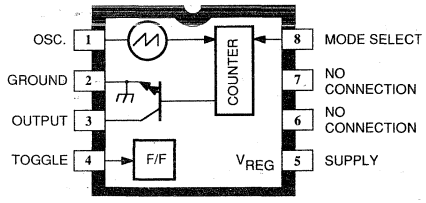
Dwg. No. A-10,706



Dwg. No. A-10,711

2436 AND 2437

COUNTDOWN POWER TIMERS



Dwg. PS-016

The ULQ2436M and ULQ2437M are rugged, long-duration countdown timers specifically designed to operate in an automotive or industrial environment. Both devices use an internal RC oscillator to drive a digital countdown circuit for timing periods of typically 2-1/2 to 5 minutes. The ULQ2436M multiplies the oscillator period by 4064 while the ULQ2437M multiplies the oscillator period by 992, otherwise the two devices are identical. Internal logic can automatically cause the timeout to be halved for successive timeouts. I^2L technology is used for the countdown and logic circuitry and conventional linear bipolar devices for the oscillator and output power functions. This combination, together with the low-cost 8-pin mini-DIP plastic package, results in a very economical power timer suitable for a wide variety of applications.

The Darlington-connected output driver is capable of switching loads up to 400 mA.

FEATURES

- 28 V/400 mA Output Switch
- Low-Cost Ceramic Timing Capacitor
- Dual-Mode Timing Operation
- -40°C to +85°C Operation
- 10 V to 16 V Operation
- Internal Stabilizing Regulator
- Low-Cost 8-Pin Mini-DIP

APPLICATIONS

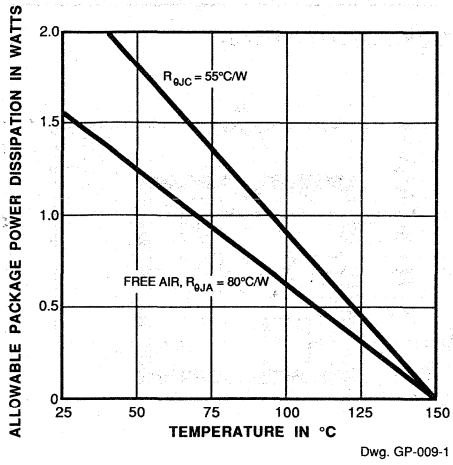
- Automotive Rear-Window Defogger Timer
- Automotive Courtesy Light Timer
- Appliance Power Timer
- Power Control System

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

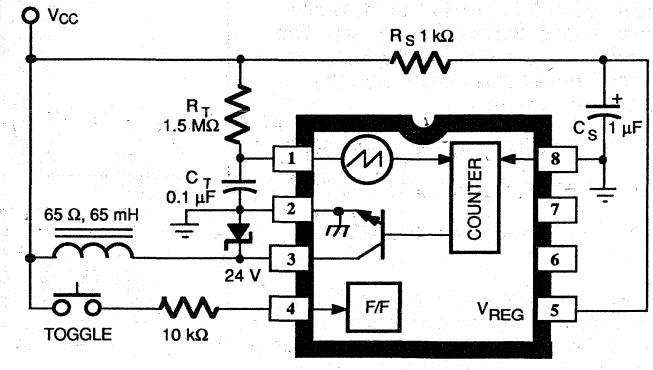
Supply Current, I_{REG} . . . . . **15 mA**
Output Voltage, V_{OUT} . . . . . **28 V**
Output Current, I_{OUT} . . . . . **400 mA**
Input Voltage, V_1 or V_4 (2 min.) . . . . . **24 V**
(continuous) . . . . . **16 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Always order by complete part number:

ULQ2436M	**Countdown by 4064**
ULQ2437M	**Countdown by 992**



TEST CIRCUIT AND TYPICAL REAR-WINDOW DEFOGGER APPLICATION



ELECTRICAL SPECIFICATIONS at T_A = -40°C to +85°C, V_{CC} = 12 V (unless otherwise specified).

Characteristic	Test Conditions	Limits		
		Min.	Max.	Units
Regulator Voltage	I_{REG} = 12 mA, Output Off	7.0	9.0	V
Output Saturation Voltage	I_{OUT} = 400 mA, T_A = +25°C	—	2.5	V
	I_{OUT} = 250 mA, T_A = +25°C	—	1.35	V
Output Leakage Current	V_{OUT} = 28 V, V_{CC} = 12 V	—	100	µA
	V_{OUT} = 22 V, V_{CC} = Open Circuit	—	100	µA
Input Threshold Voltage	10 kΩ Series Resistor	1.0	5.0	V
Oscillator Tolerance	T_A = +25°C	—	±3.0	%
	T_A = -40°C to +85°C	—	±6.0	%
Divider Count (V_{CC} = 10 V to 16 V)	Initial Timeout, ULQ2436M	4064	4064	—
	Subsequent Timeouts, ULQ2436M	2032	2032	—
	Initial Timeout, ULQ2437M	992	992	—
	Subsequent Timeouts, ULQ2437M	496	496	—

CIRCUIT DESCRIPTION

OSC. An external resistor in the range of 200 kΩ to 2 MΩ and an external capacitor in the range of 0.001 µF to 1 µF determine the frequency of the internal oscillator. The period of oscillation is nominally R_TC_T with the overall output time period (after the digital countdown) of

$t = 4064\ R_TC_T$ for the ULQ2436M

$t = 992\ R_TC_T$ for the ULQ2437M

where t is in seconds. See also MODE SELECT.

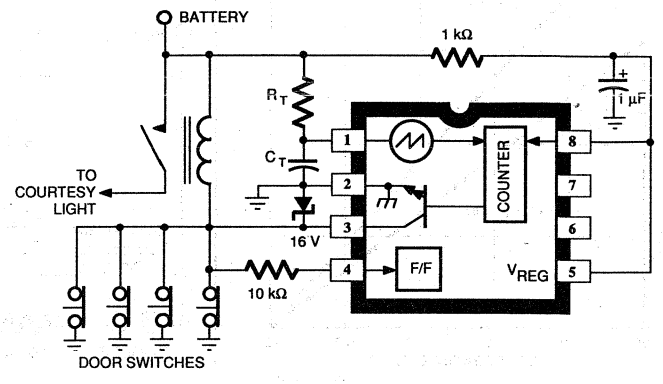
OUTPUT. The output is an open-collector of a Darlington-connected transistor. The output is ON (low) during the timing period. An external Zener diode is used to protect the output against inductive-load switching transients and automotive "load dump".

TOGGLE. A push-button, momentary-action switch at this input toggles the timer between the ON and OFF states (push-ON/push-OFF). If the timer is OFF, the oscillator and countdown circuitry are started on the falling edge of the input pulse. If the timer is ON and timing, it will be turned OFF on the rising edge of the TOGGLE input signal before the time delay has elapsed. Internal de-bounce circuitry is included.

SUPPLY. The timer requires a supply current applied to this pin through a current-limiting resistor (R_S). An internal 8 volt Zener diode shunt regulator provides a stable supply to the device over wide supply voltage variations. Capacitor C_S is used to provide decoupling.

MODE SELECT. With MODE SELECT connected to GROUND, the first activation will run for the preset time delay. All activations after the first will time out at half of the initial preset time. This sequence is reset each time the supply is interrupted. With MODE SELECT connected to SUPPLY (V_{REG}), the timer will repeat the preset time delay each time it is activated.

COURTESY LIGHT TIMER

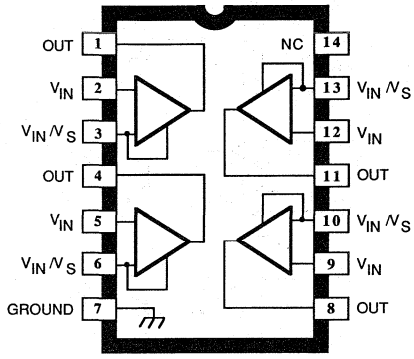


Dwg. ES-013

2453, 2454, 2455

AUTOMOTIVE LAMP MONITORS

ULN2455A



Dwg. PS-013

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Supply Voltage, V_{CC} . . . . . **30 V**
Peak Supply Voltage, V_{CC}(100 ms) . . . **80 V**
Peak Reverse Voltage, V_R . . . . . **30 V**
Output Current, I_{OUT} . . . . . **35 mA**
Package Power Dissipation, P_D . **See Graph**
Operating Temperature Range,
T_A . . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Capable of monitoring all types of automotive lamps, the ULQ2453M, ULN2454L, ULN2454M, ULN2455A, and ULN2455L lamp monitors provide multiple LED outputs to pinpoint the area in which a lamp has failed. The ULN2455A/L are quad comparators capable of monitoring eight individual lamps or groups of lamps. The ULQ2453M and ULN2454L/M are dual comparators with the latter featuring an additional output to trigger an alarm if either of the comparators detects a lamp failure. This output can be used to drive an audible signaling device or centrally located warning indicator. All devices can be used to monitor lamps, multiple low-voltage power supplies, or, with appropriate sensors, industrial processes.

Installation and operation of these lamp monitors has no effect on normal lamp operation. Comparators sense the normal voltage drop in the lamp wiring (approximately 20 mV) for each of the monitored lamp circuits. Little additional wiring is necessary for installation because the system can be completely integral to the wiring assembly. No standby power is required...the operating voltage is obtained from the sense leads; the system is energized only when the lamps are turned ON.

All devices are designed for use in the severe automotive environment. Lateral PNP transistors provide high-frequency noise immunity and differential transient-voltage protection. Reverse voltage protection, internal regulators, and temperature compensation are all embodied in the circuit designs. A failure within a device will not affect lamp operation.

These versatile lamp monitors are packaged in 14-pin plastic DIPs (suffix A), 8- or 14-lead surface-mountable SOICs (suffix L), or 8-pin mini-DIPs (suffix M) and are rated for operation over the temperature range of -40°C to +85°C.

FEATURES

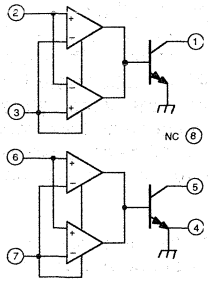
- No Standby Power
- Integral to Wiring Assembly
- Fail-Safe
- Reverse Voltage Protected
- Internal Transient Protection
- DIP or SOIC Plastic Packages

Always order by complete part number:

Part Number	Function	Style
ULQ2453M	Dual Comparator	8-Pin Mini-DIP
ULN2454L	Dual Comparator with OR Output	8-Lead SOIC
ULN2454M	Dual Comparator with OR Output	8-Pin Mini-DIP
ULN2455A	Quad Comparator	14-Pin DIP
ULN2455L	Quad Comparator	14-Lead SOIC

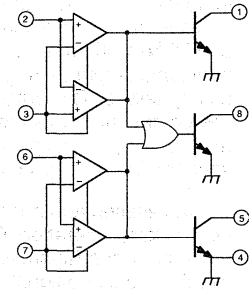
PIN OUT & FUNCTIONAL BLOCK DIAGRAMS

ULQ2453M



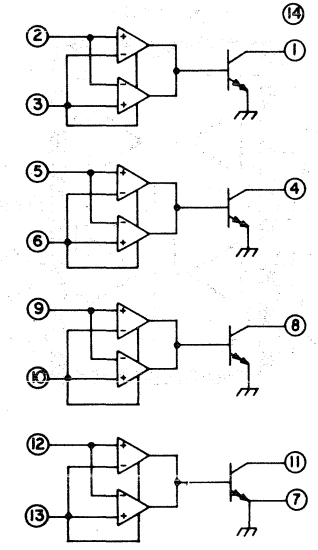
Dwg. FS-009A

ULN2454L and ULN2454M



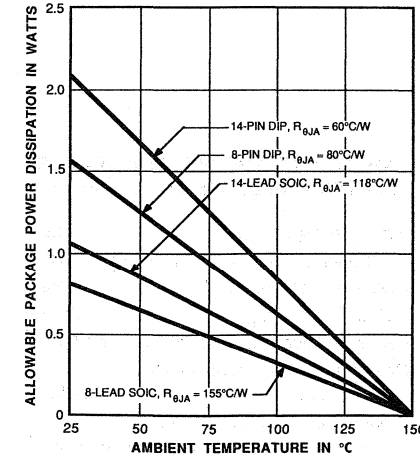
Dwg. FS-010

ULN2455A and ULN2455L



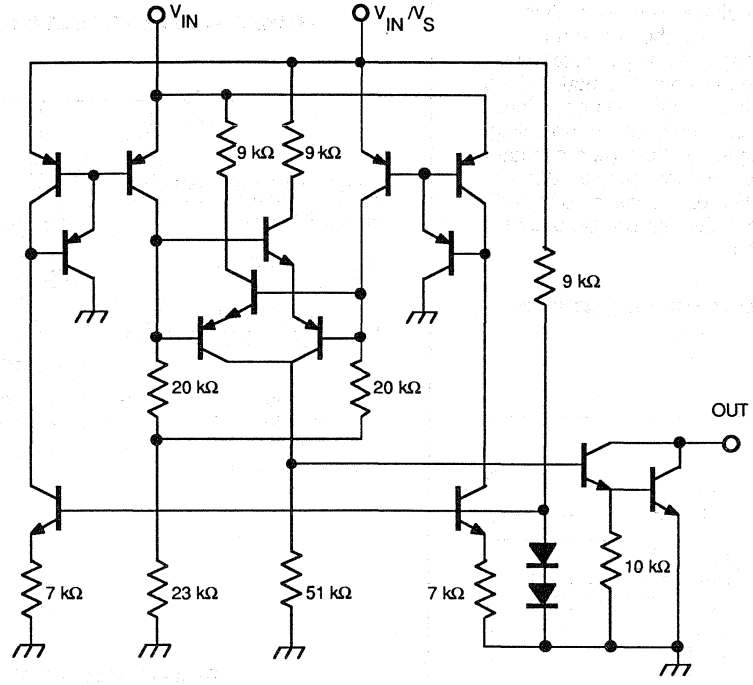
Dwg. No. A-12,033A

Note that the dual in-line package and the small-outline IC package are electrically identical and share a common pin number assignment.



Dwg. GS-008

SIMPLIFIED SCHEMATIC
(SINGLE DIFFERENTIAL SENSE AMPLIFIER)



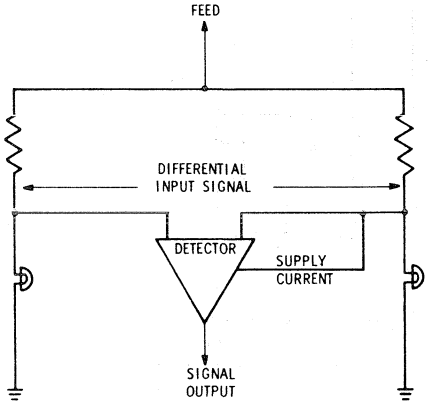
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{IN} = 10 to 16 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 80 V, ΔV_{IN} < 7 mV	—	—	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 5 mA, ΔV_{IN} > 20 mV	—	0.8	1.0	V
		I_{OUT} = 30 mA, ΔV_{IN} > 20 mV	—	1.4	2.0	V
Differential Switch Voltage	ΔV_{IN}	V_{IN}-V_{IN}/V_S	7.0	13	20	mV
Input Current	I_{IN}	ΔV_{IN} = V_{IN}-V_{IN}/V_S = +30 mV	150	300	800	µA
	I_{IN}/I_S	ΔV_{IN} = V_{IN}-V_{IN}/V_S = -30 mV	0.5	1.7	3.5	mA

PRINCIPLE OF OPERATION

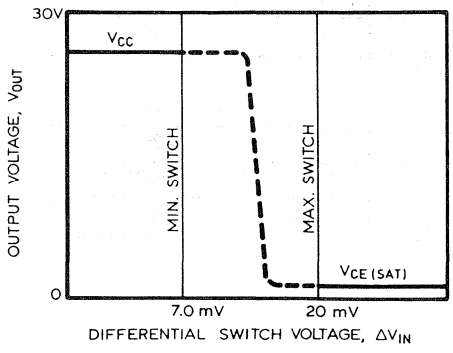
Operation of these lamp monitors is similar to that of a simple bridge circuit in which the top two legs of the bridge are formed by the wiring assembly resistance or discrete low-value resistors. The bottom legs of the bridge are the monitored lamps. These differential amplifier circuits sense the voltage drops in the wiring assemblies (approximately 20 mV) for each of the lamp circuits. When the system detects a difference in voltage due to an open filament, the appropriate output driver is turned ON.

BASIC BRIDGE MONITORING SYSTEM



Dwg. No. A-11,473A

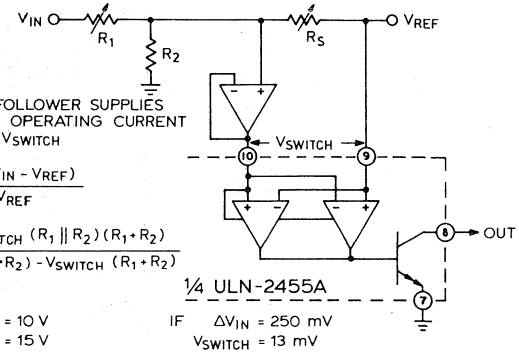
TYPICAL SWITCH CHARACTERISTICS



Dwg. No. A-12,187

TYPICAL APPLICATIONS

POWER SUPPLY SUPERVISORY CIRCUIT



$$R_1 = \frac{R_2\,(V_{IN} - V_{REF})}{V_{REF}}$$

$$R_S = \frac{V_{SWITCH}\,(R_1 \parallel R_2)\,(R_1 + R_2)}{(\Delta V_{IN} \cdot R_2) - V_{SWITCH}\,(R_1 + R_2)}$$

IF V_{REF} = 10 V, V_{IN} = 15 V, R_2 = 15 kΩ

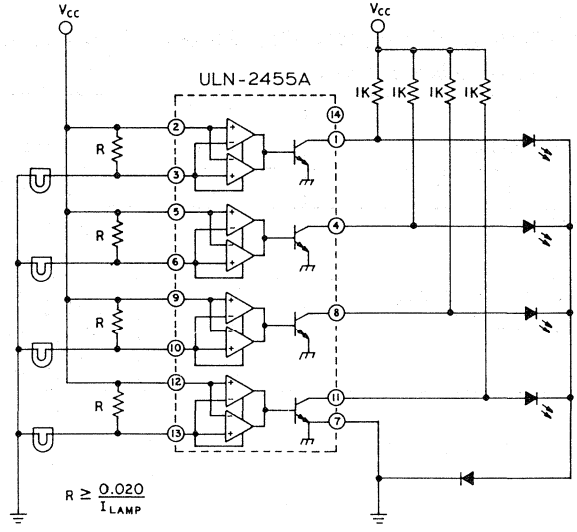
THEN R_1 = 7.5 kΩ

IF ΔV_{IN} = 250 mV, V_{SWITCH} = 13 mV

THEN R_S = 423 Ω

Dwg. No. B-1524

QUAD LAMP MONITOR



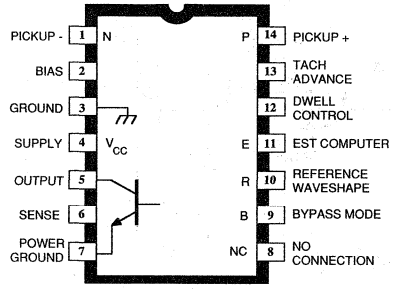
$$R \geq \frac{0.020}{I_{LAMP}}$$

Dwg. No. A-12,035A

2460

ELECTRONIC SPARK TIMING

ULQ2460A



Dwg. PS-014

ABSOLUTE MAXIMUM RATINGS in Typical Application

Supply Voltage, V_{CC} (100 ms) ..... **80 V**
(5 min.) ..... **25 V**
(continuous) ..... **16 V**
Peak Reverse Voltage, V_R ..... **-5.0 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-40°C to +125°C**
Storage Temperature Range,
T_S ..... **-65°C to +150°C**

The ULQ2460A and ULQ2460LW electronic spark timing circuits are intended to interface between conventional electromagnetic pick-ups, a computer-controlled electronic spark timing (EST) computer, and a high-efficiency ignition coil.

In application, the devices are designed to withstand various load dump and battery supply transients and to protect their output. They provide a positive shut down feature if battery supply voltages exceed 35 V. In the event of an open or shorted signal input, they provide a fail-safe mode that shuts off the output. If the EST computer fails or is disconnected, the ULQ2460A/LW will continue to process the pickup signal and thus allow the engine to continue to operate in a "limp" or soft-failure mode. For additional reliability improvement, a constant-current ignition coil drive eliminates the need for the usual ballast resistor.

The ULQ2460A is furnished in a 14-pin dual in-line plastic package. The ULQ2460LW is supplied in a surface-mountable 16-lead wide-body SOIC. Both devices are rated for operation over the automotive temperature range of -40°C to +125°C.

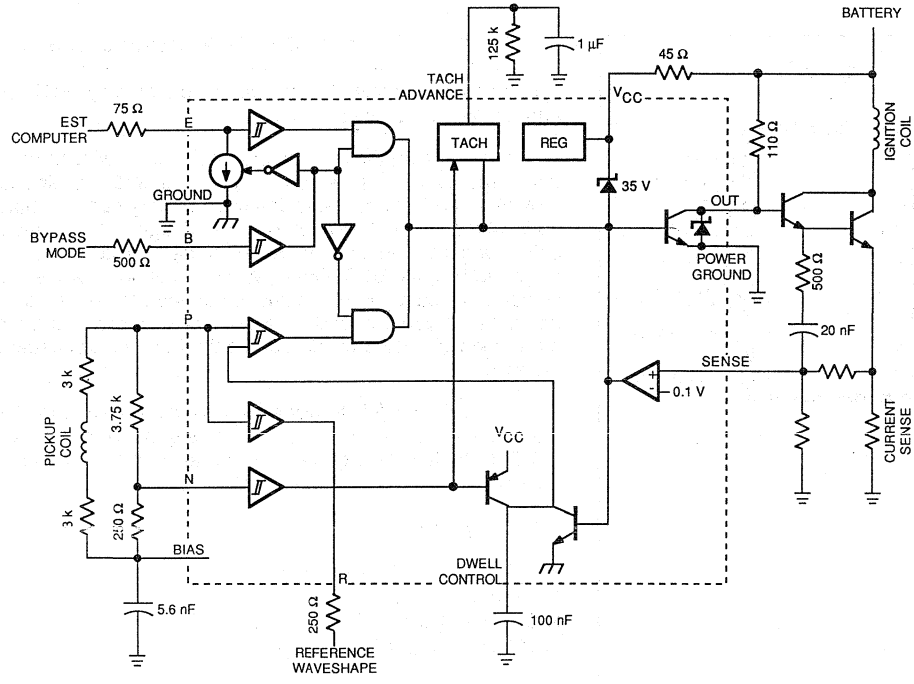
FEATURES

- Improved System Reliability
- Internal Bypass Mode
- Constant-Current Drive to Ignition Coil
- 180 mJ Primary Coil Energy

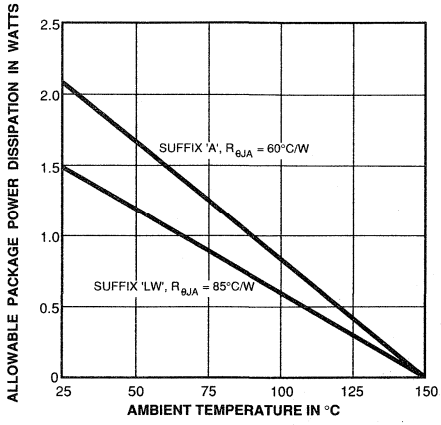
Always order by complete part number:

ULQ2460A	**14-Pin DIP**
ULQ2460LW	**16-Lead Wide-Body SOIC**

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL APPLICATIONS

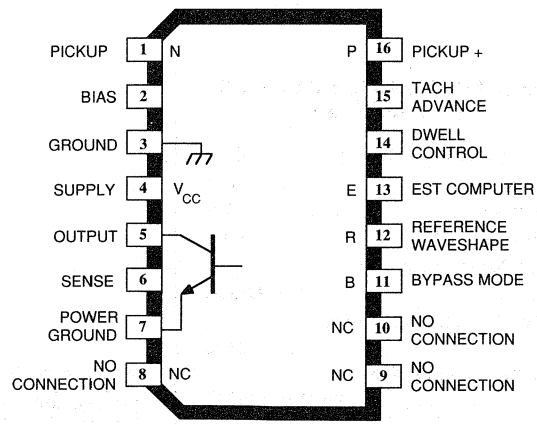


Dwg. FS-011



Dwg. GS-009

ULQ2460LW



Dwg. PS-015

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 16 V, in typical application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	Operating	4.0	—	16	V
Bypass Threshold	$V_{B(ON)}$	V_{11} = 2.3 V, 160 µA ≤ I_{11} ≤ 360 µA	1.4	1.8	2.3	V
	$V_{B(OFF)}$	V_{11} = 2.3 V, 3 mA ≤ I_{11} ≤ 15 mA	0.7	1.0	1.3	V
Bypass Hysteresis	ΔV_B		0.45	1.0	—	V
Bypass Input Current	I_B	V_9 = 2.3 V	160	—	360	µA
EST Threshold	$V_{E(ON)}$	V_9 = 2.3 V, Output HIGH	1.4	1.8	2.3	V
	$V_{E(OFF)}$	V_9 = 2.3 V, Output LOW	0.7	1.0	1.3	V
EST Hysteresis	ΔV_E		0.45	1.0	—	V
EST Input Current	I_E	V_{11} = 2.3 V, V_9 = 2.3 V	160	—	360	µA
		V_{11} = 2.3 V, V_9 = 0 V	3.0	—	15	mA
Reference Output	$V_{R(HI)}$	I_{10} = -10 µA, V_9 = 0 V, V_{PN} = 700 mV	—	—	6.0	V
		I_{10} = -1 mA, V_{PN} = 700 mV	2.4	—	—	V
	$V_{R(LO)}$	I_{10} = 1 mA, V_{PN} = 30 mV	—	—	0.75	V
Input Threshold	$V_{PN(ON)}$	V_{CC} = 4 V, V_6 = 0 V, Output HIGH	70	250	500	mV
		V_{10} ≥ 2.4 V, V_9 = 0 V	130	275	650	mV
		V_{10} ≥ 2.4 V, V_9 = 5 V	275	900	1500	mV
	$V_{PN(OFF)}$	V_{CC} = 4 V, V_6 = 0 V, Output LOW	5.0	100	—	mV
		V_{10} ≤ 0.75 V	40	100	—	mV
Input Hysteresis	ΔV_{PN}	V_6 = 0 V, V_{CC} = 4 V	30	150	—	mV
		V_9 = 0 V	75	150	—	mV
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 150 mA	—	200	500	mV
		Load Dump, I_{OUT} = 750 mA	—	—	1.0	V
Output Leakage Current	I_{OUT}	V_{OUT} = 3 V	—	—	2.0	µA
Output Current Limit Threshold Voltage	V_{SENSE}	4 V ≤ V_{CC} ≤ 26 V	65	100	135	mV
Output Current Temperature Coefficient	I_{OUT}	V_{CC} = 14.5 V, V_{PN} = 2 V	—	—	±2000	ppm/°C
Dwell Control Charge Current	I_{DWELL}	V_{PN} = 7 V, V_6 = 0 V, V_9 = 0 V, V_{12} = 4 V	15	—	70	µA
Dwell Control Discharge Current	I_{DWELL}	V_{PN} = 2.5 V, V_6 = 200 mV, V_B = 0 V, V_{12} = 4 V	30	—	80	µA

NOTE: Pin numbers apply to ULQ2460A.

Continued next page...

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Dwell ON Threshold Control	V_{PN}	V_6 = 0 V, V_{12} = 4 V, Output HIGH	-0.8	—	-2.4	V
Dwell Threshold Control Clamp	V_{PN}	V_6 = 0 V, V_{12} = 7.5 V, Output HIGH	-3.5	—	-5.7	V
Advance Control Charge	V_P	V_{PN} = 7 V ⎣ 2.5 V, V_{12} = 0 V	1.7	—	3.0	V
Advance Control Discharge	V_P	V_{PN} = 2.5 V ⎣ 0 V, V_{12} = 0 V	—	—	100	mV
Advance Control Comparator Enabled	$V_{P(ON)}$	V_{PN} = 8 V, Output LOW	—	—	1.3	V
Advance Control Comparator Disabled	$V_{P(OFF)}$	V_{PN} = 8 V, Output HIGH	0.5	—	—	V
Advance Control Differential Voltage	ΔV_P		1.2	—	1.7	V
Sense Input Clamp	i_{SENSE}	V_{14} = -0.5 V	-0.5	—	-3.5	mA
Zener Clamp Current	I_{CC}	V_{CC} = 35 V, pulse test	29	—	77	mA

NOTE: Pin numbers apply to ULQ2460A.

2460
ELECTRONIC SPARK TIMING

CIRCUIT DESCRIPTION & TYPICAL APPLICATION

The ULQ2460A or ULQ2460LW electronic spark timing circuit is connected to the electronic spark timing computer at three points:

REFERENCE WAVESHAPE (R). Sends engine crankshaft position and speed information to the electronic spark timing computer as determined by the state of the bypass control input.

ELECTRONIC SPARK TIMING (E). Receives dwell and timing information from the electronic spark timing computer for the initiation of primary coil current and spark timing. When the EST computer is in control (input B pulled high), a constant-current sink at this input turns ON as confirmation back to the computer.

BYPASS MODE (B). With an active-low signal from the electronic spark timing computer or open circuit at this input (either is indicative of a computer failure), the device senses and processes the input signal received from the pickup coil, thereby generating and controlling dwell, spark timing, and spark advance without the aid of the computer (bypass mode). With a high signal input from the computer, the ULQ2460A/LW processes the input signal received from the pickup coil, generating a modified pulse train at the reference waveshape output which, after processing by the EST computer, is returned to the device through the EST terminal thereby allowing the computer to determine dwell, spark timing, and spark advance (EST mode).

The floating, ground-isolated signal generated by the electromagnetic pick-up is connected to the circuit through the P (positive) and N (negative) inputs.

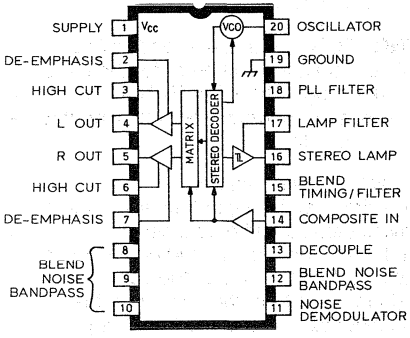
The output of the circuit is connected through an external Darlington-connected power driver and the primary winding of a high-efficiency ignition coil to the battery without the need for ballast resistor protection and provides the following functions:

1. Stores energy in the magnetic field of the ignition coil based on the available dwell time.
2. Limits the maximum energy stored in the magnetic field of the ignition coil by limiting the maximum current that can be achieved (typically 5.5 A).
3. At the required time, it rapidly shuts off the coil current causing a collapse of the magnetic field and dumping the stored energy through the secondary winding at a very-high voltage into the spark plug.

In the EST mode of operation, the output is totally under the control of the computer.

3827

FM STEREO DECODER



Dwg PS-011

The ULN3827A FM stereo decoder utilizes advanced demodulation techniques for improved performance under adverse receiving conditions. This is particularly important in automotive receivers where the signal strength and multipath effects are continuously changing. It is designed to provide the best possible performance under the widest range of signal conditions while also reducing the cost and complexity of standard FM multiplex receivers. This is accomplished through the use of a dual-bandwidth phase-locked loop and a Walsh function for the regenerated carrier. These two improvements to the carrier recovery system produce the best possible immunity to noise and interference of any modern PLL stereo decoder under poor signal conditions.

The dual-bandwidth phase-locked loop switches to a very narrow bandwidth to assure optimal phase stability under noisy reception conditions. Noise-actuated blending adjusts the stereo separation as a function of signal-to-noise ratio to reduce the background noise for low-signal levels and eliminate transition problems at the stereo/mono switch point. The regenerated 19 kHz reference and 38 kHz carrier are free from 3rd and 5th harmonics to improve adjacent channel rejection and signal-to-noise ratio as well as providing good rejection of ARI (Auto Radio Information), RDS (Radio Data System), and other data tones.

The ULN3827A is supplied in a 20-pin dual in-line plastic package with a copper lead frame that eliminates many decoupling problems.

FEATURES

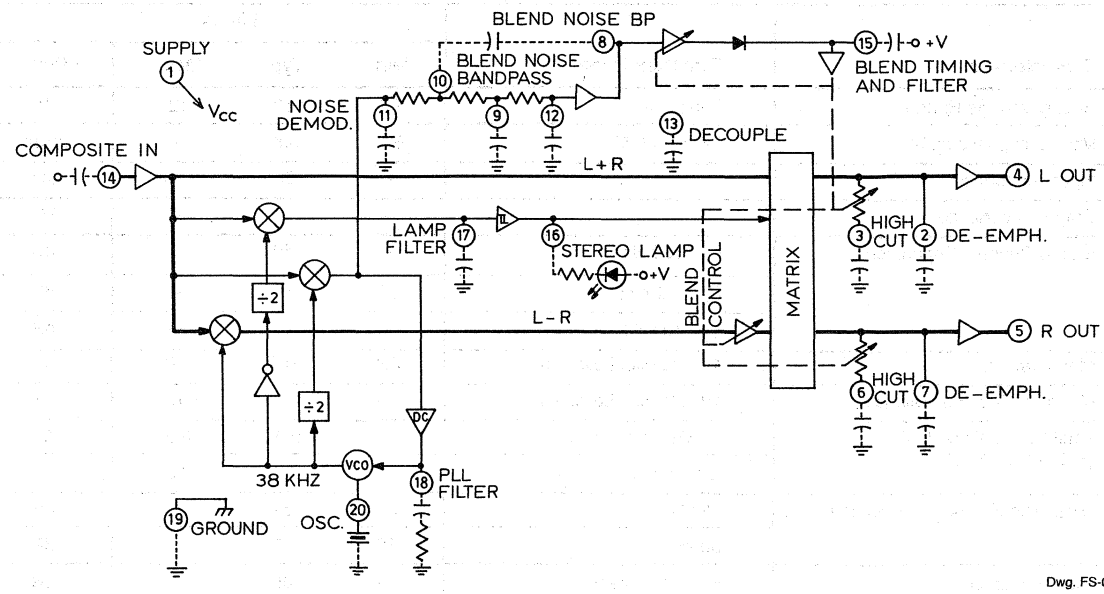
- Reduced Automotive Stereo Multi-Path Effects
- Dual Bandwidth Phase-Locked Loop
- No Adjustments Required
- Improved Adjacent-Channel Rejection
- Good ARI/RDS Rejection
- 19 kHz Pilot Canceling
- Noise-Actuated Blending and High Cut
- Ceramic Resonator Controlled Oscillator
- Automatic Stereo/Mono Switching

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **12 V**
Package Power Dissipation, P_D . . . . . **1.0 W**
Operating Temperature Range,
T_A . . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to+150°C**

Always order by complete part number: **ULN3827A**.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 10 V, Composite Input = 400 mVrms (L = R, pilot OFF), Pilot Level = 40 mVrms, f_m = 1 kHz, unless otherwise specified.

Characteristic	Test Conditions	Limits			
		Min.	Typ.	Max.	Units
Supply Voltage Range	Functional	8.5	10	12	V
Max. Composite Input	THD = 1.0 %	600	800	—	mVrms
Input Impedance		—	25	—	kΩ
Output Impedance		—	1.0	—	kΩ
Stereo Channel Separation	f_m = 100 Hz	—	50	—	dB
	f_m = 1.0 kHz	30	50	—	dB
	f_m = 10 kHz	—	40	—	dB
Monaural Gain	19 kHz Pilot Level = 0	0.4	0.6	1.6	dB
Monaural Channel Balance	19 kHz Pilot Level = 0	—	0	±1.0	dB
Total Harmonic Distortion (100 Hz to 1 kHz)	19 kHz Pilot = 0	—	0.05	0.5	%
	L or R only	—	0.1	0.5	%
Ultrasonic Frequency Rejection	19 kHz	36	51	—	dB
	38 kHz	35	45	—	dB
SCA Rejection	67 kHz (Note 2)	—	65	—	dB
Spurious Response	114 kHz, 10% modulation	—	65	—	dB
	190 kHz, 10% modulation	—	65	—	dB
PLL Bandwidth	Loop Locked	—	20	—	Hz
Stereo Switch Level	19 kHz Pilot Only, Lamp ON	10	15	22	mVrms
	19 kHz Pilot Only, Lamp OFF	6.0	11	16	mVrms
Stereo Lamp Hysteresis	Lamp OFF to Lamp ON	—	3.0	—	dB
Capture Range	Pilot = 6.0 mV	—	300	—	Hz
Lock Range	Pilot = 20 mV	—	300	—	Hz
Blend Threshold	$S+N/_N$	—	36	—	dB
Stereo Lamp Output Current	Short Circuit, Lamp ON	5.0	20	40	mA
	Lamp OFF, V_{CC} = 12 V	—	0	3.0	µA
Quiescent Supply Current	Lamp OFF	—	22	35	mA

NOTES: 1) Typical values are given for circuit design information only.
2) Measured with a stereo composite signal of 80% stereo, 10% pilot, and 10% SCA.

3827
FM STEREO DECODER

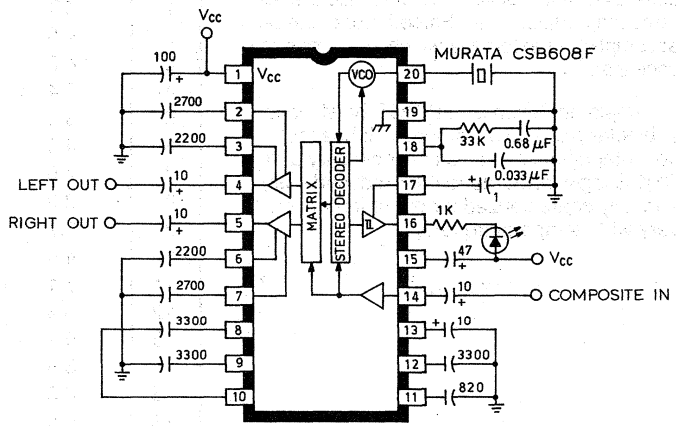
THE ALLEGRO FM STEREO SYSTEM

This new stereo decoder utilizes advanced demodulation techniques for improved performance under adverse receiving conditions. This is particularly important in automotive receivers where the signal strength and multipath effects are continuously changing. The ULN3827A FM stereo decoder also reduces the cost and complexity of FM multiplex receivers. It is designed to provide the best possible performance under the widest range of signal conditions. This is accomplished through the use of a variable-bandwidth phase-locked loop and the use of a Walsh function for the regenerated carrier.

Prior integrated stereo decoders utilized a loop bandwidth of typically 300 Hz, which was a compromise between acquisition performance and carrier recovery. Acquisition is generally satisfactory with this bandwidth, however, carrier recovery integrity often degrades under noisy conditions; in the worst case to complete loss of carrier. This is more apparent under multipath conditions. Although this is not the only noise observed under multipath events, it is a real source of disturbance. A secondary feature of the wider bandwidth is a peak in L – R distortion at the loop resonance frequency at 9.5 kHz. Clearly, to provide optimal performance, the loop bandwidth should be sub-audible. To provide reasonable acquisition times, the ULN3827A phase-locked loop is operated in a wide-band mode until carrier acquisition. Upon capture, the loop is then switched to a narrow-band mode (typically 20 Hz) to provide superior noise immunity under adverse signal conditions.

Currently available stereo decoders generate square waves for the regenerated 19 kHz pilot and 38 kHz carrier. Although this is convenient from the standpoint of circuit design, the spurious response of the receiver, as observed at RF, exhibits a sine n/n spurious response pattern centered about the received frequency and spaced at 38 kHz intervals. The most detrimental harmonic is the 5th, located at 190 kHz, since this spurious seriously degrades adjacent channel rejection. The preferred technique for eliminating these spurious responses would be the use of a pure sine-wave regenerated carrier.

TEST CIRCUIT AND TYPICAL APPLICATION



POLARIZED CAPACITANCE VALUES ARE IN µF, NON-POLARIZED CAPACITANCE VALUES ARE IN pF, UNLESS OTHERWISE INDICATED.

Dwg. ES-010A

The typical application and circuit constants herein are included only as an example and provide no guarantee for designing equipment to be mass-produced. The information herein is believed to be accurate and reliable. However, no responsibility is assumed by Allegro MicroSystems for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

However, this is impractical using digital carrier regeneration techniques. A more conveniently implemented method is the Walsh function which is a digital technique for generating the odd-ordered harmonics in a waveform that can be subtracted from the square wave to produce a sine-wave approximation. This avoids much of the previously described spurious responses. The implementation of this function is relatively easy in a modern stereo decoder employing a high-frequency ceramic resonator for the oscillator since the required divider can readily produce the Walsh function as a side product.

This stereo decoder also incorporates a noise-operated blending system that is completely contained within the chip. Other devices with signal-strength operated blending are frequently fooled into full stereo operation by strong but poor quality signals during multipath events. The noise-operated blending system is also actuated by environmentally generated and multipath-induced noise since the system is based exclusively on signal-to-noise ratio as observed at the FM detector output. Since the technique of blending on noise is inherently more repeatable than signal-strength based blending, production blend adjustments are not required.

3827
FM STEREO DECODER

In addition to the advanced features previously described, the ULN3827A decoder uses a ceramic oscillator to eliminate the last remaining adjustment. Forced mono can be accomplished externally which also stops the oscillator.

Implementation is in BiMOS IV which is a bipolar plus CMOS process. It has the advantages of low-noise linear circuitry and CMOS logic that is dense (for reduced cost) and fully characterized for operation over a very-wide temperature range.

PIN FUNCTIONS

Pin	DC Voltage	Function	Notes
1	10	Supply	—
2	4.0	Left De-Emphasis	R_S = 27.8 kΩ
3	4.3	Left High Cut	R_S = 20 kΩ
4	3.4	Left Output	R_S = 1 kΩ
5	3.4	Right Output	R_S = 1 kΩ
6	4.3	Right High Cut	R_S = 20 kΩ
7	4.0	Right De-Emphasis	R_S = 27.8 kΩ
8	3.0	Blend Capacitor	—
9	3.7	Blend Capacitor	—
10	4.4	Blend Capacitor	—
11	5.1	Blend Capacitor	—
12	5.4	Blend Capacitor	—
13	5.4	Blend Decouple	—
14	3.6	Composite Input	R_{IN} = 25 kΩ [1]
15	8.3	Blend Timing & Filter	[2]
16	9.0	Stereo Indicator	Locked = 0.1 V
17	5.0	Lock Detector Filter	Locked = 4.7 V
18	5.6	Loop Filter	Locked = 4.7 [3]
19	0.0	Ground	—
20	9.0	608 kHz Resonator	—

NOTES: 1) The decoder matrix does not account for FM detector frequency roll-off. An input RC network can be used to correct for this if separation is not sufficient.

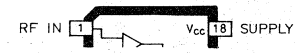
2) Blend threshold can be increased to about 42 dB (but separation will be reduced at lower levels) by adding 470 kΩ to V_{cc}. Smaller values will cause blending when it is not desired.

3) The loop filter capacitor should be low-leakage current because the phase detector output current is very low.

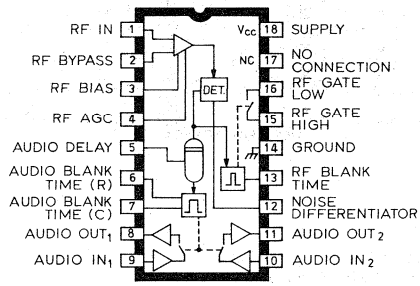
3845 AND 3846

AM NOISE BLANKERS

ULN3845LW



ULN3845A



Dwg. PS-003

The ULN3845A (dual in-line package) and ULN3845LW (small-outline IC package) are electrically identical and share a common pin number assignment.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **12 V**
Package Power Dissipation,
P_D . . . . . **880 mW**
Operating Temperature Range,
T_A . . . . . **-40°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +125°C**

These noise blanker integrated circuits contain all of the necessary circuitry for adding an extremely efficient noise blanking technique (patents pending) to any type of AM tuner or receiver with RF input frequencies (or a first IF) to 30 MHz. The ULN3845A/LW features dual audio channels and is intended for AM-stereo or independent sideband applications. The ULN3846A/LW has only a single audio channel but is electrically identical to the ULN3845A/LW in all other respects.

A high input impedance, high-gain, broadband RF amplifier permits these devices to be directly connected to the RF stage of a tuner. The internal automatic gain control circuitry insures that the noise detection threshold remains constant with changes in input signal level. The AGC circuitry is identical to that of the ULN3841A/LW AM signal processors and is especially recommended for use with those devices. The response time of the RF gate is sufficiently fast to blank the noise pulse at the output of the mixer before the IF filter. Very-short blanking times will effectively suppress most of the interfering noise. Residual audio noise is removed by an audio sample-and-hold gate. The RF blanking time, audio gate delay time, and audio gate blanking time can all be independently adjusted to suit the particular application.

These AM noise blankers are packaged in plastic DIPs (suffix A) or surface-mountable wide-body SOICs (suffix LW), and are rated for operation over the temperature range of -40°C to +85°C.

FEATURES

- RF Blanking to 30 MHz
- Single-Channel or Stereo Audio Blanking
- Adjustable RF and Audio Blanking Time
- Adjustable Audio Blanking Delay
- Sample-and-Hold MOS Audio Gates
- Internal Voltage Regulation
- Minimum External Components

APPLICATIONS

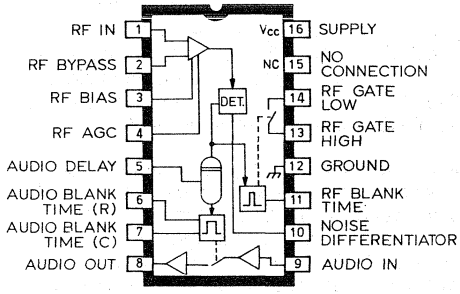
- AM and AM-Stereo Automotive Radios
- CB Transmitter/Receivers
- Short-Wave Receivers
- Mobile Communications Equipment

Always order by complete part number:

Part Number	Function	Package
ULN3845A ULN3845LW	Stereo Noise Blanker	18-Pin DIP 18-Lead SOIC
UNL3846A ULN3846LW	Mono Noise Blanker	18-Pin DIP 18-Lead SOIC

ULN3846LW

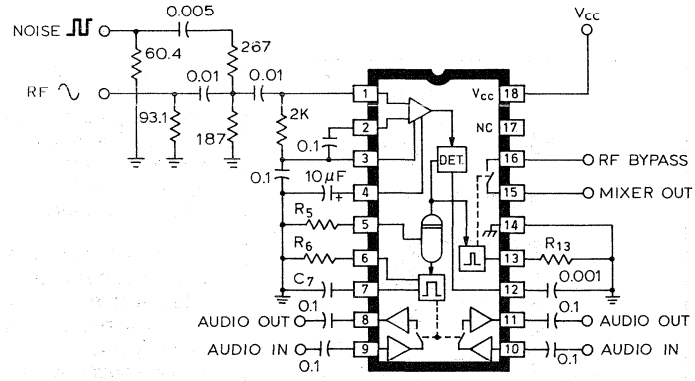
ULN3646A



Dwg. PS-004

The ULN3846A (dual in-line package) and the ULN3846LW (small-outline IC package) are electrically identical and share a common pin number assignment.

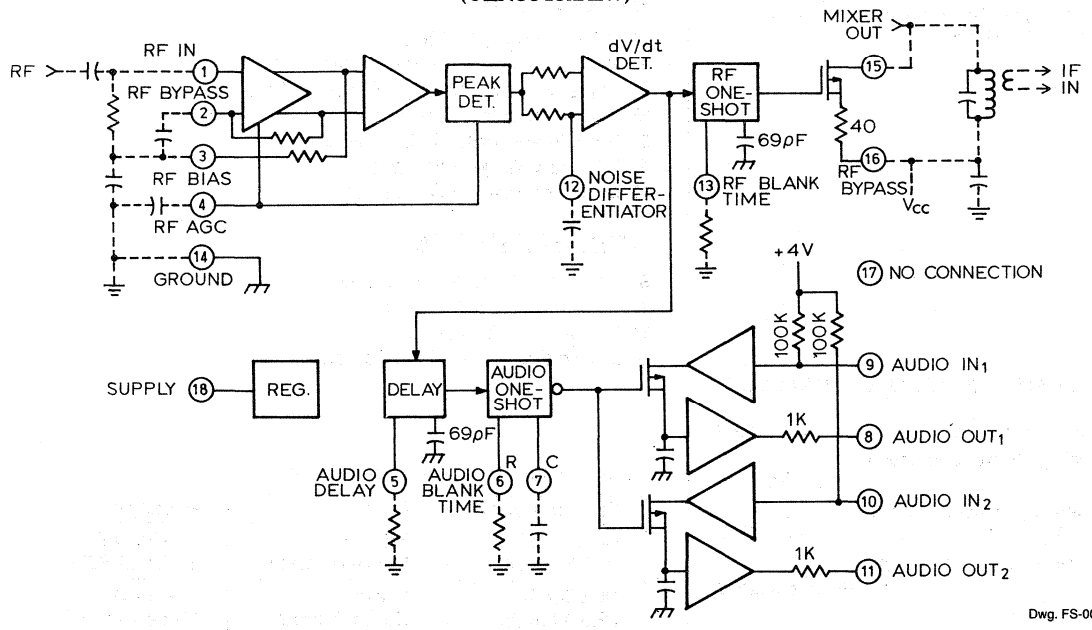
TEST CIRCUIT
FIGURE 1



Dwg. ES-007

Note that the noise-pulse input is attenuated 20 dB by the test circuit.

FUNCTIONAL BLOCK DIAGRAM
(ULN3845A/LW)



Dwg. FS-004

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 9 V, f_{rf} = 1 MHz, Noise (f_{noise}) = 500 Hz Square Wave, f_{af} = 1 kHz, Test Figure 1.

Characteristic	Test Pins*	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	18	Operating	7.5	9.0	12	V
Quiescent Supply Current	18	V_{RF} = 0	—	12	20	mA
RF INPUT AMPLIFIER:						
Trigger Threshold	1	Noise Pulse Amplitude for V_{RF} = 0	—	100	—	µV
Modulation Threshold	1	Noise Pulse Modulation for V_{RF} = 1 mV	—	85	—	%
Detector Rise Time	12	C_{12} = 0	—	500	—	ns
RF SWITCH:						
ON Resistance	15-16		—	50	70	Ω
OFF Resistance	15-16		—	100	—	kΩ
Time Delay	1-15	From Beginning of RF Pulse to Beginning of RF Blanking	—	1.5	3.0	µs
AUDIO SWITCHES:						
Attenuation	9-8, 10-11		60	80	_	dB
Noise	8, 11		—	1.5	6.0	mVpp
Crosstalk	8, 11	ULN3845A/LW Only	—	60	—	dB
Gain	9-8, 10-11		-1.0	-0.5	0	dB
Total Harmonic Distortion	8, 11	V_{af} = 300 mV, V_{noise} = 0	—	<0.1	0.5	%
Input Impedance	9, 10		—	100	—	kΩ
Output Impedance	8, 11		—	1.0	—	kΩ
BLANKING TIMERS:						
RF Blanking	15	R_{13} = 350 kΩ	45	55	65	µs
Audio Delay	8	R_5 = 350 kΩ	40	50	62	µs
Audio Blanking	8	R_6 = 110 kΩ, C_7 = 0.0012 µF	220	290	360	µs

*Pin numbers are for ULN3845A/LW.

3845 AND 3846
AM NOISE BLANKERS

CIRCUIT DESCRIPTION

Previous attempts at suppression of impulse noise in AM receivers have used a variety of approaches ranging from gating the signal OFF at the antenna to simply clipping (limiting) any signal that was larger than the average modulation. Unfortunately, the former can generate as much noise as it removes while the latter only reduces the level of noise impulses and does not remove them.

A major problem in attempting to suppress impulse noise in an AM receiver can best be described by looking at the shape of a noise pulse as it passes through a typical tuner as shown in Figure 2. Here, a typical 0.5 µs pulse is applied to the antenna input. The resulting waveforms are essentially the impulse response of the different selectivity sections as limited only by the dynamic range of the individual sections. Note that the signal remains quite narrow until the IF filter is reached. Because of the relatively narrow bandwidth of the IF filter, the limiting of the IF amplifier, and the filtering effect of the detector, the audio output resulting from the impulse is much wider than the original input pulse and is therefore much more objectionable.

One blanking scheme currently in use senses the noise pulse in the IF amplifier and blanks the audio output. This results in a long blanking time and poor performance at the higher frequencies where a short blanking time is needed most.

The ULN3845A/LW and ULN3846A/LW take a different approach to the noise suppression problem by sensing the noise pulse in the receiver's RF section and blanking the pulse before it reaches the IF. This requires a noise amplifier with a minimum propagation delay and high-speed gating.

Blanking the noise pulse in this way is very effective, but some of the interference can still reach the audio output due to the loss of carrier during the blanking interval. For this purpose, an additional delay, blanking interval, and audio gate (or gates in the case of the ULN3845A/LW) are included to further suppress any residual signal. The result is almost 100% suppression of impulse noise including that from ignition systems and from sources producing interference at a power line rate such as light dimmers and fluorescent lamps.

QUIESCENT DC VOLTAGES
(FOR CIRCUIT DESIGN INFORMATION ONLY)

Pin Number			Typical
ULN3845A/LW	ULN3846A/LW	Pin Function	DC Voltage
1	1	RF In	3.1
2	2	RF Bypass	3.1
3	3	RFBias	3.1
4	4	RF AGC	0.9
5	5	Audio Delay	4.8
6	6	Audio Blank Time (R)	4.8
7	7	Audio BlankTime (C)	4.8
8	8	Audio Out_x	4.75
9	9	Audio In_x	4.0
10	—	Audio In_2	4.75
11	—	Audio Out_2	4.0
12	10	Noise Differentiator	4.9
13	11	RF Blank Time	4.8
14	12	Ground	Reference
15	13	RF Gate High	—
16	14	RF Gate Low	—
17	15	No Connection	0
18	16	Supply	V_{CC}

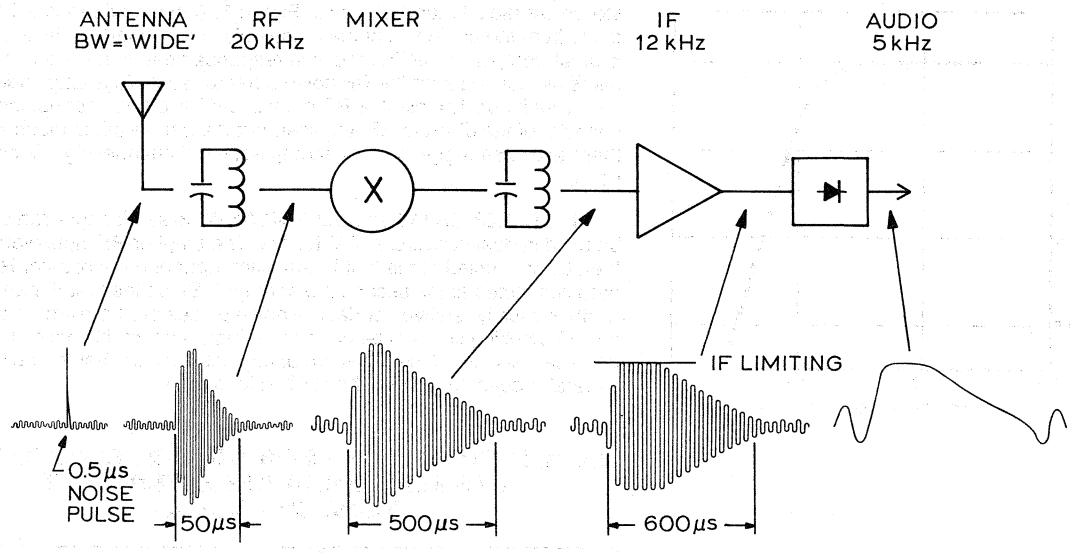
Referring to the Functional Block Diagram, the RF input stage is a differential amplifier, so that the input impedance is high. The triggering threshold at the RF amplifier input is about 15 µV at 1 MHz. This means that a pulsed RF input signal of 15 µV will exceed the threshold and trigger the blanker. The external capacitor at the dV/dt detector circuit (C_{12}) is selected so that audio signals do not cause triggering. At high input levels, the threshold is internally set so that an RF burst of 50% modulation triggers the blanker. A resistor in parallel with C_{13} will increase the detection threshold level.

The RF-switching MOSFET (pins 15-16) is controlled by the RF one-shot whose gate time is determined by the value of R_{13}.

$$\text{RF Gate Time } (\mu s) = 157 \times 10^{-12} \times R_{13}$$

where R_{13} should be greater than 33 kΩ. Smaller values for C_{12} will reduce the sensitivity to RF input pulses. The MOSFET turns ON within approximately 1.5 µs (shunting the RF signal to ground) after a noise pulse is detected and then turns OFF over a 15 µs period after the end of the RF gate time. The ON resistance of the MOSFET is about 40 Ω. The slow turn-OFF prevents any additional transients from being introduced into the receiver by the RF gate. The internal gate circuit also includes charge-balancing circuits so that switching transients are canceled and do not appear at the output. These features ensure transient-free switching even when the RF gate is connected to the low-level input stages of a receiver. Note that the RF gate must be

TYPICAL PULSE RESPONSE
FIGURE 2



Dwg. OS-001

connected to a supply to obtain the minimum ON-resistance of the MOSFET gate. This makes it convenient to connect the RF gate in parallel with the receiver mixer output transformer primary.

Blanking in the RF or mixer sections of the receiver removes most of the noise pulse but a small amount still remains due to the hole punched in the carrier. This residual noise is theoretically somewhere between the peak audio and 100% negative modulation but is significantly smaller and narrower than that which the impulse would normally produce without blanking. An audio delay, one-shot, and audio gate(s) are included to eliminate this residual signal.

The audio delay is determined by the value of R_5:

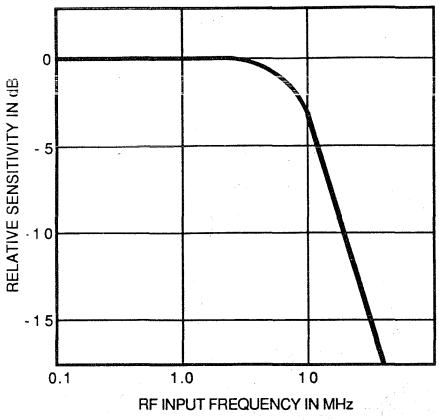
Audio Gate Delay (μs) = $143 \times 10^{-12} \times R_5$

where R_5 should be greater than 33 kΩ. The amount of delay required will depend on the IF filtering characteristics of the particular receiver design. After the audio delay time, the audio one-shot is triggered. The audio switching MOSFETs (pins 8-9 and pins 10-11) are controlled by the audio one-shot whose gate time is determined by the values of R_5 and C_7:

Audio Gate Time (μs) = $2.2 \times R_6 \times C_7$

The MOSFET audio gates also include charge-balancing circuits to eliminate switching transients.

TYPICAL RF FREQUENCY RESPONSE



Dwg. GS-006

TYPICAL APPLICATION

A typical application using the ULN3845A in a C-QUAM® AM stereo car radio tuner is shown in Figure 3. Although there is a 1.5 µs delay from the beginning of the noise pulse to the start of blanking, this is small compared with the impulse response time of the receiver. It takes almost 10 µs for the RF noise burst to reach 70% amplitude at the mixer input. The blanker RF input could have been connected to the collector of the discrete RF amplifier, but the bandwidth is much wider there and false triggering from strong adjacent channel signals could occur.

The ULN3845A/LW and ULN3846A/LW noise blankers can also be used in dual-conversion AM tuners. The blanker RF input would then be connected at the first IF amplifier input and the blanker RF gate connected at the second mixer output. Since the first IF bandwidth is usually relatively wide, the noise pulses are narrower, and the RF blanking time will be correspondingly less. In this case, it may be necessary to reduce the value of capacitor C_{12} so that the noise separator does not extend the RF blanking time.

COIL INFORMATION FOR HIGH-PERFORMANCE ETR AM STEREO RECEIVER WITH NOISE BLANKING

	Symbol	Q	N1:N2	N1:N3	Toko Part Number
Antenna	T_1		1:1.6		7HN-60064CY
RF	T_2, T_3	120		10:1	RWOS-6A7894AO, L = 178 µH
Local Osc.	T_4	120		5:1	7TRS-A5609AO
Mixer	T_5		2:1	8.9:1	7LC-502112N4, C_T = 180 pF
Detector	L_2	100			A7BRS-T1041Z, C_T = 1000 pF

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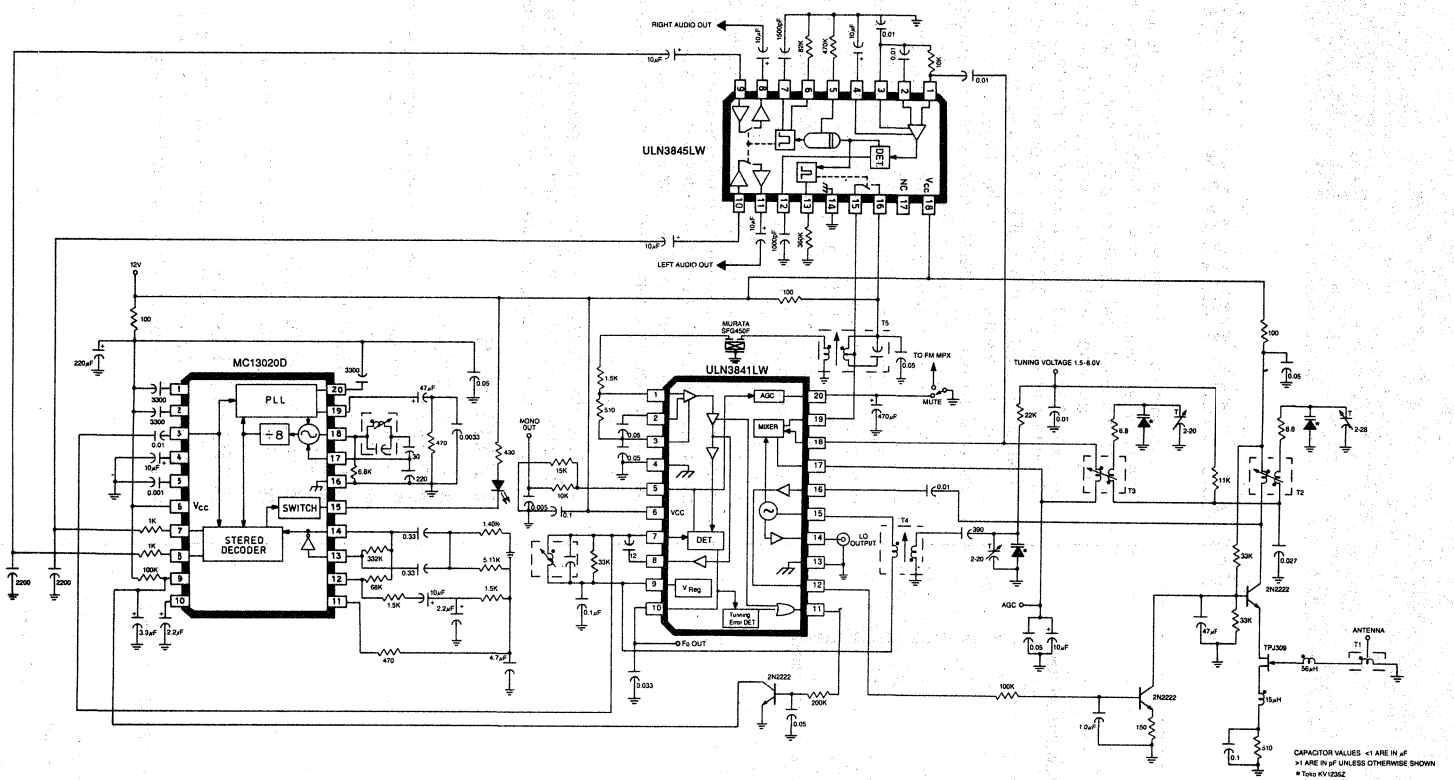
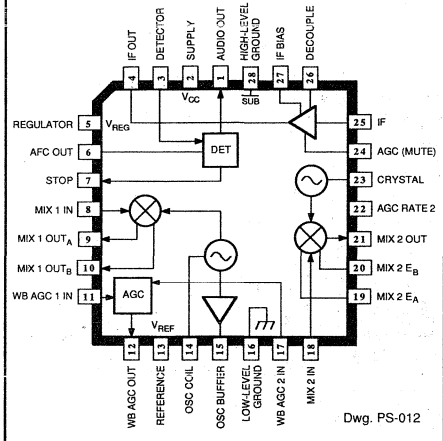
ETR AM STEREO RECEIVER WITH NOISE BLANKING



3847

DUAL-CONVERSION AM RECEIVER



Dwg. PS-012

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . **12 V**
Package Power Dissipation, P_D . . . . **1.2 W**
Operating Temperature Range,
T_A . . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

Providing the AM signal processing functions for an electronically tuned AM receiver (ETR), the ULN3847EP includes two balanced mixers, a crystal local oscillator, an L/C-tuned local oscillator, oscillator buffer, IF amplifier, AM detector, scan control detectors, and a switchable voltage regulator. This dual-conversion device mixes the incoming RF up to a first IF of 10.7 MHz, then down to 450 kHz, and then detects the audio. The addition of a JFET matched to a whip antenna, RF low-pass filter, IF selectivity, and audio stages gives a complete AM radio which can be used in automotive receivers. The frequency-detecting stop circuit is also capable of recovering narrow-band FM, making it useful for scanners or weatherband radio applications.

The ULN3847EP has a greatly improved stop detection system over other existing devices. It uses the dual criteria of frequency and amplitude for establishing a valid stop. Tuning accuracy (frequency criteria) is established by evaluating phase shift across the detector coil. The circuitry is similar to that used in FM discriminators. Since this detection system is phase operated, it remains effective even in the presence of strong signals, which can cause false stops in systems using narrow-band filters. The amplitude criterion for stop is determined by evaluating the IF level. It includes a unique circuit that removes the effect of the AGC action. This allows the AGC tuning components to be selected for low-frequency audio performance without compromising scanning speed.

This AM signal processor is packaged in a 28-lead plastic leaded chip carrier (PLCC) for surface-mount applications and is rated for operation over the temperature range of -40°C to +85°C.

FEATURES

- Low Noise Figure
- Balanced Mixers
- Buffered Oscillators
- Very Effective Stop Detector
- Dual Wide-Band AGC
- Delayed AGC
- Narrow-Band FM Output
- 6.5 V to 12 V Operating Range

APPLICATIONS

- Automobile Radios
- High-Quality Home Entertainment Receivers

Always order by complete part number: **ULN3847EP** .

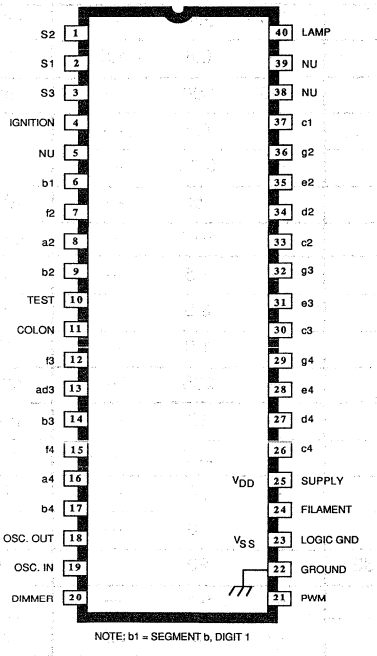
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 10 V

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Current	I_{CC}	I_2, V_{in} = 0	—	45	65	mA
Sensitivity	V_{in}	V_{out} = 50 mV	—	6.0	—	µV
Recovered Audio	V_{out}	V_{in} = 1 mV	200	250	—	mV
Total Harmonic Dist.	THD	V_{in} = 1 mV, Mod = 80%	—	0.4	1.5	%
Oscillator Output	V_o	V_{15}	180	300	—	mV
Stop Output Voltage	V_{STP}	V_7, V_{in} = 0	—	4.8	—	V
		V_7, V_{in} = 1 mV	—	0.05	—	V
Stop Sensitivity	V_{stp}	V_{11} = 2.5 V, Mod = 0%	—	100	—	µV
Stop Bandwidth	BW_{STP}	V_{in} = 1 mV, V_{11} = 1.5 V, Mod = 0%	—	10.2	—	kHz
Wide-Band AGC	V_{AGC}	V_{in} = 0	—	7.5	—	V
		V_{in} = 18 mV	—	6.5	—	V
		V_{in} = 60 mV	—	1.0	—	V
Overload	V_{in}	V_{out} = 10% THD, Mod = 80%	—	200	—	mV
-3dB Limiting	V_{in}	Mod = 3 kHz peak deviation	—	12	—	µV
FM Recovered Audio	V_{out}	V_6, Mod = 3 kHz peak deviation	—	380	—	mV
Signal to Noise Ratio	S+N/N	V_{in} = 250 µV	—	50	—	dB
		V_{in} = 10 mV	—	60	—	dB
AGC Figure of Merit	FOM	Ref. at V_{in} = 5 mV, V_{in} or V_{out} = -10 dB	—	20	—	µV
Regulator Voltage	V_{REG}	V_5	—	5.1	—	V
		V_5, V_{24} = 0 (Muted)	—	0	0.2	V
Reference Voltage	V_{REF}	V_{13}	—	3.7	—	V

5233/38, 5458/63/74, 5604

2-FUNCTION, 4-DIGIT VF AUTOMOTIVE CLOCKS

SCL5604E



NOTE: b1 = SEGMENT b, DIGIT 1

Dwg. PC-002

ABSOLUTE MAXIMUM RATINGS

Logic Supply Current, I_{SS} ..... **-7.0 mA**
Total Supply Current, I_{DD} ..... **20 mA**
Input Voltage Range (Ref. V_{SS}),
V_{IN} ..... **-0.5 V to V_{DD} + 0.5 V**
Input Current, I_{IN} ..... **±10 mA**
Package Power Dissipation, P_D ... **300 mW**
Operating Temperature Range,
T_A ..... **-40°C to +85°C**
Storage Temperature Range,
T_S ..... **-65°C to +150°C**

Caution: These CMOS devices have static protection but are susceptible to damage if exposed to extremely high static electrical charges.

These devices are 2-function digital automotive clock circuits fabricated on a single monolithic chip using CMOS technology. They feature low cost, low power, and high reliability. The six devices in this series offer a variety of display and setting options and provide all of the functions normally desired in a 4-digit automotive clock.

All versions provide a push-button "time tone" setting that will zero the minutes and seconds counters if the displayed time is within two minutes of the hour. This feature allows the user to instantly set the clock according to the time tone commonly provided on radio stations.

The display driver outputs will directly drive standard vacuum fluorescent displays. A dimmer input controls the display intensity by varying the pulse width rather than by lowering the output voltage. This technique results in a more uniform display intensity. The rise and fall times of the output drivers are optimized to reduce RF interference.

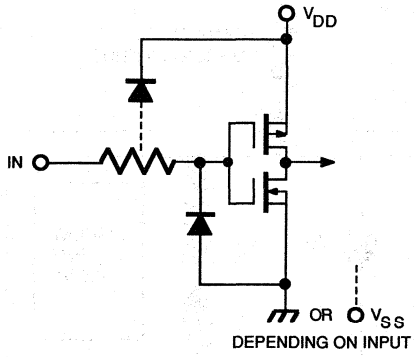
All devices are supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row centers and are rated for continuous operation over the automotive temperature range of -40°C to +85°C. Other packages are available on special order.

FEATURES

- Push-Button "Time Tone" Setting
- Variable Pulse-Width Display Dimming
- 12- or 24-Hour Timekeeping Option
- Rollover Protection on Minutes Set
- High Noise Immunity
- Diode Protection on all Inputs
- RFI/EMI Minimized

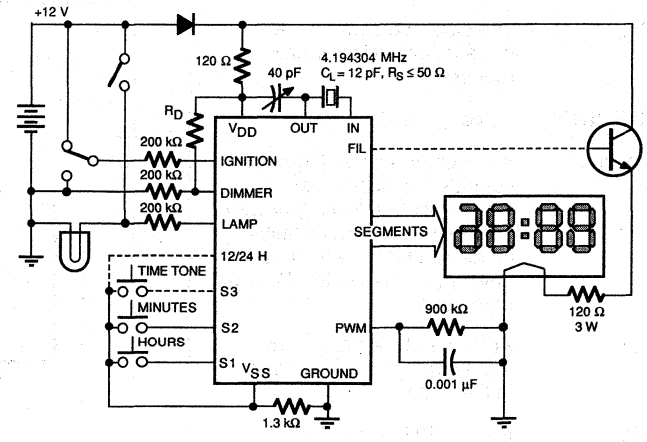
Always order by complete part number, e.g. **SCL5233E** .

TYPICAL INPUT CIRCUITRY



Dwg. EP-010-8

TYPICAL APPLICATION



Dwg. EC-003

ELECTRICAL CHARACTERISTICS at T_A = -40°C to +85°C, V_{SS} = 0 V, in Typical Application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Min. Operating Voltage	V_{DD}	T_A = +25°C	4.5	—	—	V
		T_A = -40°C to +85°C	5.0	—	—	V
Zener Voltage	V_{Z1}	I_{SS} = -6.0 mA, T_A = +25°C	6.2	6.9	7.5	V
	V_{Z2}	I_{GND} = -17 mA, T_A = +25°C	15	16.5	18	V
Output Breakdown Voltage	$V_{(BR)DS}$	I_{OUT} = -5 µA, T_A = +25°C	15	—	—	V
Segment Output Current	I_{OUT}	V_{DD} = 6.0 V, V_{OUT} = 5.5 V	-150	—	—	µA
Filament Output Current	I_{FIL}	V_{DD} = 6.0 V, V_{FIL} = 5.0 V	-2.0	—	—	mA
Oscillator Frequency	f_{OSC}	T_A = +25°C	—	4.194304	—	MHz
Input Resistance	R_{IN}	S1, S2, or S3 only	300	—	—	kΩ
Switch Debounce Time	t_{DB}		0	31	62.5	ms
Segment Switching Time	t_r	ΔV_{OUT} = 5.0 V	1.0	—	—	µs
Zener Temperature Coefficient	ΔV_{Z1}	T_A = +25°C	—	+6.0	—	mV/°C
Supply Current	I_{DD}	V_{DD} = 5.0 V, T_A = +25°C	—	—	1.0	mA

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

FUNCTIONAL DESCRIPTION

V_{DD} The positive supply.

V_{SS} The clock logic reference; current limiting is normally required.

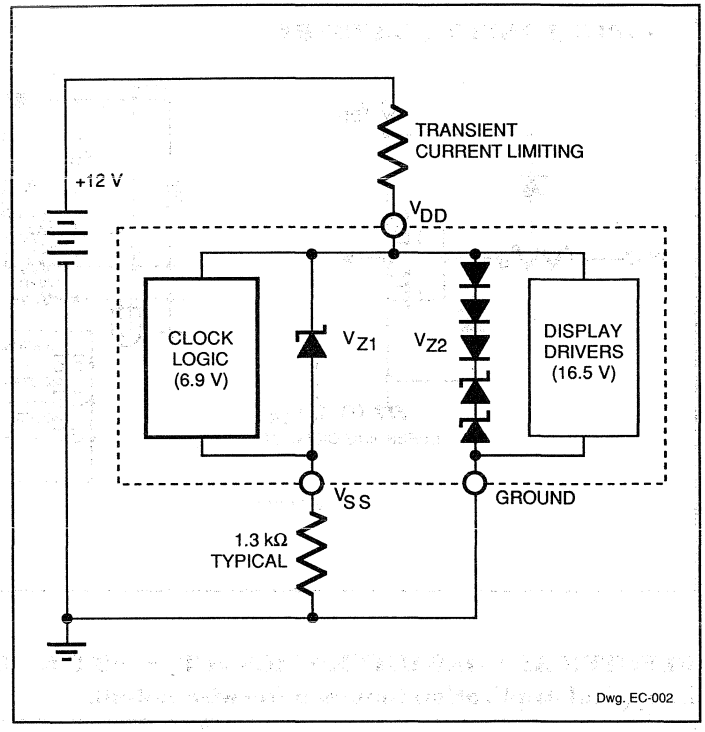
GROUND Power ground.

12/24 H A switch or hard wiring here controls the clock timebase: Open = 24 h, Low (V_{SS}) = 12 h. This function is not available in the SCL5604E and that device operates in the 12-hour mode only.

S1 Pulling S1 Low (V_{SS}) increments the hours as shown in the table.

S2 Pulling S2 Low (V_{SS}) increments the minutes as shown in the table.

S3 Momentary switch for time tone, to start clock, and display command. This switch is required for the A5238EA, optional for all other devices.



Clock Version	S1 (Set Hours)	S2 (Set Minutes)	S3	Colon
SCL5233E	one increment per depression	one increment per depression, start clock	optional ... time tone and display command*	steady
SCL5238E	one increment per depression	one increment per depression	time tone, display command*, start clock	steady
SCL5458E	one increment per depression	one increment per depression, start clock	optional ... time tone and display command*	one second flashing
SCL5463E	one increment per second while depressed	one increment per second while depressed, start clock	optional ... time tone and display command*	one second flashing
SCL5474E SCL5604E	two increments per second while depressed	two increments per second while depressed, start clock	optional ... time tone and display command*	steady

* See IGNITION

For all devices except the SCL5238E, the first depression of S2 stops the clock and resets the seconds. Simultaneous depressions of S1 and S2 reset the clock to the 1:00:00 state; the clock restarts when S2 is released. With the SCL5238E, after the first depression of S2, if more than four seconds elapse between S1 or S2 depressions, the entire display flashes at a one-second rate to indicate that the clock has been reset. Simultaneous depressions of S1 and S2 reset the clock to the 1:00:00 state; the clock restarts when S3 is operated.

If the clock is running and the time is within two minutes after the hour, depressing S3 causes seconds and minutes to reset, and the hour to remain the same. If the time is within two minutes before the hour, depressing S3 causes seconds and minutes to reset and the hour to increment by one. The clock resumes operation in the real time mode when S3 is released. Any operation outside the ±2 minute window will not affect the clock.

LAMP Controls display brightness in conjunction with IGNITION.

IGNITION Controls display brightness in conjunction with LAMP.

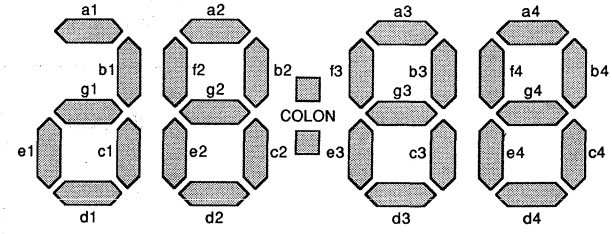
IGNITION Input	LAMP Input	
	12 V (ON)	Ground (OFF)
12 V (ON)	50% brightness†, dimmer enabled, S1, S2, S3 enabled	100% brightness, dimmer disabled, S1, S2, S3 enabled
Ground (OFF)	50% brightness†, display command enabled, dimmer enabled	display OFF, display command enabled

† 25% for SCL5604E

With IGNITION at ground (OFF), a depression of S3 will turn ON the display for 4 ±1 seconds at 100% brightness. The time tone function is disabled when the IGNITION input is ground.

FILAMENT The enable output for the VF display filament. If S3 is omitted, the discrete transistor can also be omitted if the display filament is connected directly to the 12 V supply through the accessory switch.

SEGMENTS The output drives for the VF display segments.

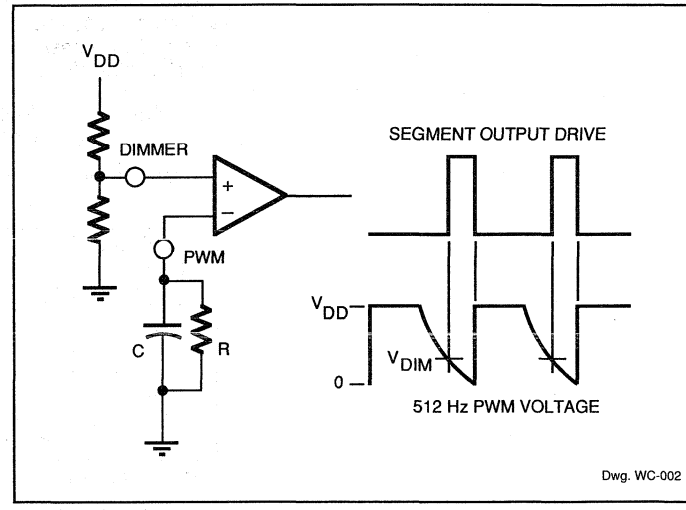


Dwg. OC-001-1

COLON The output drive for the VF display colon. For the SCL5233E, SCL5238E, SCL5474E, and SCL5604E the colon is steady; for the SCL5458E and SCL5463E the colon is in a one-second flashing mode.

DIMMER A voltage input to control the display brightness.This can be from a fixed (R_D) or light-dependent resistor divider, or a linear voltage control signal.

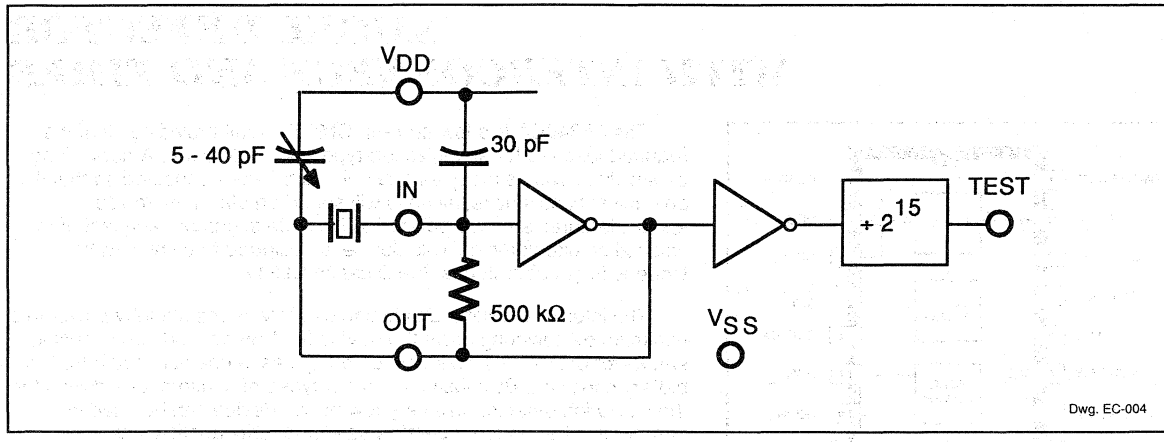
PWM An RC network for controlling the display duty cycle (dimming).



R_D or	V_{DIM}/V_{DD}	Per Cent Duty Cycle (at T_A = +25°C) RC = 0.9 ms	RC = 1.72 ms
370 kΩ	0.35	1	0
245 kΩ	0.45	10	0
165 kΩ	0.55	20	0
108 kΩ	0.65	29	4
67 kΩ	0.75	36	20
35 kΩ	0.85	42	33
10.5 kΩ	0.95	48	45

IN & OUT These are the oscillator connections for the external crystal and frequency adjustment.

TEST This is a test point for adjustment of the crystal oscillator frequency. When properly aligned, the output at this terminal is a 128 Hz square-wave signal.



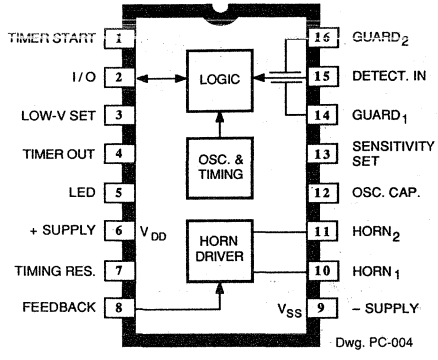
PIN DESIGNATIONS

Pin	SCL5604E	All Other Devices	Pin	SCL5604E	All Other Devices
1	S2	S2	21	PWM	PWM
2	S1	LAMP	22	GROUND	DIMMER
3	S3	adeg1	23	V_{SS}	OSC. IN
4	IGNITION	12/24 H	24	FILAMENT	OSC. OUT
5	NU	c1	25	V_{DD}	b4
6	b1	g2	26	c4	a4
7	f2	e2	27	d4	f4
8	a2	d2	28	e4	b3
9	b2	c2	29	g4	ad3
10	TEST	g3	30	c3	f3
11	COLON	e3	31	e3	COLON
12	f3	c3	32	g3	TEST
13	ad3	g4	33	c2	b2
14	b3	e4	34	d2	a2
15	f4	d4	35	e2	f2
16	a4	c4	36	g2	b1
17	b4	V_{DD}	37	c1	NU
18	OSC. OUT	FILAMENT	38	NU	IGNITION
19	OSC. IN	V_{SS}	39	NU	S3
20	DIMMER	GROUND	40	LAMP	S1

NU = Internal connection, do not use.

5348

SMOKE DETECTOR WITH INTERCONNECT AND TIMER



Dwg. PC-004

The A5348CA is a low-current, CMOS circuit providing all of the required features for an ionization-type smoke detector. A networking capability allows as many as 125 units to be interconnected so that if any unit senses smoke, all units will sound an alarm. In addition, special features are incorporated to facilitate alignment and test of the finished smoke detector. This device is designed to comply with Underwriters Laboratories Specification UL217.

The internal oscillator and timing circuitry keeps standby power to a minimum by powering down the device for 1.66 seconds and sensing smoke for only 10 ms. Every 24 on/off cycles, a check is made for low battery condition. By substituting other types of sensors, or a switch for the ionization detector, this very-low power device can be used in numerous other battery-operated safety/security applications.

The A5348CA is supplied in a low-cost, 16-pin dual in-line plastic package. It is rated for continuous operation over the temperature range of 0°C to +50°C.

FEATURES

- Interconnect Up to 125 Detectors
- Piezoelectric Horn Driver
- Guard Outputs for Detector Input
- Pulse Testing for Low Battery
- Power-ON Reset
- Internal Reverse Battery Protection
- Internal Timer & Control for Reduced Sensitivity
- Built-In Hysteresis Reduces False Triggering

ABSOLUTE MAXIMUM RATINGS
(Voltages are referenced to V_{SS})

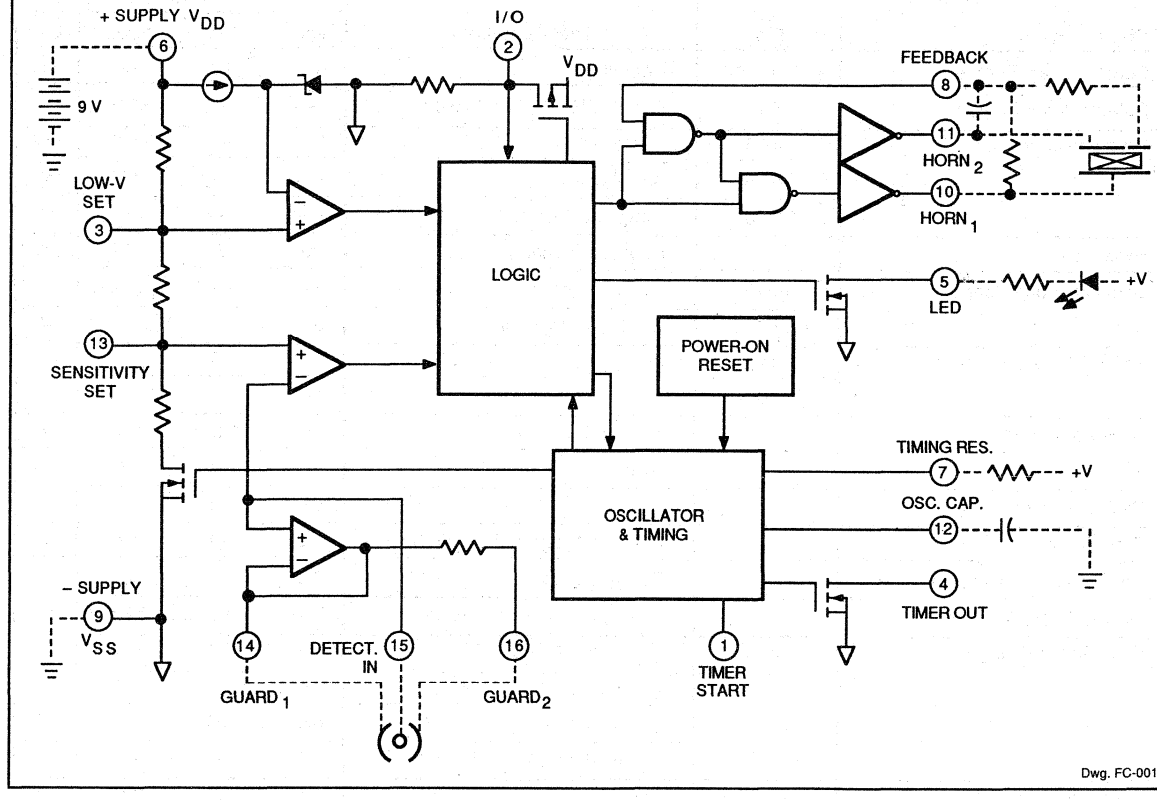
Supply Voltage Range,
V_{DD} ..... **-0.5 V to +15 V**
Reverse Battery (10.5 V) ..... **20 s**
Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
Input Current, I_{IN} ..... **10 mA**
Operating Temperature Range,
T_A ..... **0°C to +50°C**
Storage Temperature Range,
T_S ..... **-55°C to +125°C**

CAUTION: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Always order by complete part number: **A5348CA**

5348
SMOKE DETECTOR WITH INTERCONNECT AND TIMER

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 9.0 V, V_{SS} = 0 V, C_{12} = 0.1 µF, R_7 = 8.2 MΩ (unless otherwise noted).

Characteristic	Test Pin	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	6	Operating	6.0	9.0	12	V
Detector Input Current	15	0 to 40% RH, V_{IN} = 0 to 9.0 V	—	—	±1.0	pA
Input Offset Voltage	14-15	Active Guard	—	—	±100	mV
	16-15	Active Guard	—	—	±100	mV
	15-13	Detect Comparator	—	—	±50	mV
Hysteresis	13	No Alarm to Alarm	90	130	170	mV
Common Mode Range	14-15	Guard Amplifier	2.0	—	V_{DD} - 0.5	V
	13-15	Smoke Comparator	0.5	—	V_{DD} - 2.0	V
Active Guard Impedance	14	to V_{SS}	—	10	—	kΩ
	16	to V_{SS}	—	500	—	kΩ
Oscillator Period	12	No Alarm	1.34	1.67	2.00	s
		Alarm	32	40	48	ms
Oscillator Pulse Width	4		8.0	10	12	ms
Timer Period	4	After Pin 1 High-to-Low, No Smoke	8.0	10	12	min
Low Voltage Threshold	6	T_A = 0 to 50°C	7.2	—	7.8	V
Sensitivity Adj. Voltage	13	V_{13}/V_{DD}, pin 13 open circuit	48.5	50	51.5	%
Horn Output Voltage	10-11	I_{OUT} = 16 mA, V_{DD} = 9.0 V	—	0.1	0.5	V
		I_{OUT} = 16 mA, V_{DD} = 7.2 V	—	—	0.9	V
		I_{OUT} = -16 mA, V_{DD} = 9.0 V	8.5	8.8	—	V
		I_{OUT} = -16 mA, V_{DD} = 7.2 V	6.3	—	—	V
Horn Output ON Time	10-11	Alarm	120	160	208	ms
		Low Battery	8.0	10	12	ms
Horn Output OFF Time	10-11	Alarm	60	80	104	ms
		Low Battery	32	40	48	s
Timer Start Logic Levels	1	V_{IH}	3.5	—	—	V
		V_{IL}	—	—	1.5	V
Timer Start Input Current	1	V_{IN} = 9.0 V	20	—	80	µA

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.

Continued next page . . .

NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} < V_{13}$; No Alarm (No Smoke) Condition as $V_{15} > V_{13}$.

ELECTRICAL CHARACTERISTICS continued

Characteristic	Test Pin	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Timer Out Output Current	4	V_{OUT} = 0.5 V	500	—	—	µA
LED Output ON Current	5	V_{DD} = 7.2 V, V_{OUT} = 1.0 V	10	—	—	mA
LED Output ON Time	5		8.0	10	12	ms
LED Output OFF Time	5	No Alarm, In Standby	32	40	48	s
		No Alarm, Timer Mode After Pin 1 High-to-Low	8.0	10	12	s
I/O Current	2	No Alarm, $V_{I/O} = V_{DD}$ - 2.0 V	25	—	60	µA
		Alarm, $V_{I/O} = V_{DD}$ - 2.0 V	-7.5	—	—	mA
I/O Alarm Voltage	2	External "Alarm" In	3.0	—	—	V
I/O Delay	2	"Alarm" Out	—	3.0	—	s
Supply Current	6	V_{DD} = 9.0 V, No Alarm, No Loads	—	5.0	9.0	µA
		V_{DD} = 12 V, No Alarm, No Loads	—	—	12	µA

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.

NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} < V_{13}$; No Alarm (No Smoke) Condition as $V_{15} > V_{13}$.

CIRCUIT DESCRIPTION

The A5348CA is a low-current CMOS circuit providing all of the required features for an ionization-type smoke detector.

Oscillator. An internal oscillator operates with a period of 1.67 seconds during no-smoke conditions. Every 1.67 seconds, internal power is applied to the entire circuit and a check is made for smoke. Every 24 clock cycles (40 seconds), the LED is pulsed and a check is made for low battery by comparing V_{DD} to an internal reference. Since very-low currents are used in the device, the oscillator capacitor at pin 12 should be a low-leakage type (PTFE, polystyrene, or polypropylene).

Detector Circuitry. When smoke is detected, the resistor divider network that sets the sensitivity (smoke trip point) is altered to increase the sensitivity set voltage (pin 13) by typically 130 mV with no external connections to pins 3 or 13. This provides hysteresis and reduces false triggering. An active guard is provided on both pins adjacent to the detector input (pin 15). The voltage at pins 14 and 16 will be within 100 mV of the input. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard amplifier is not power strobed and thus provides constant protection from surface leakage currents. The detector input has internal diode protection against static damage.

Alarm Circuitry. If smoke is detected, the oscillator period changes to 40 ms and the horn is enabled. The horn output is typically 160 ms ON, 80 ms OFF. During the OFF time, smoke is again checked and

5348
SMOKE DETECTOR WITH INTERCONNECT AND TIMER

will inhibit further alarm output if smoke is not sensed. During smoke conditions the low battery alarm is inhibited and the LED is driven at a 1 Hz rate.

Sensitivity Adjust. The detector sensitivity to smoke is set internally by a voltage divider connected between V_{DD} and V_{SS}. The sensitivity can be externally adjusted to the individual characteristics of the ionization chamber by connecting a resistor between pin 13 and V_{DD}, or between pin 13 and V_{SS}.

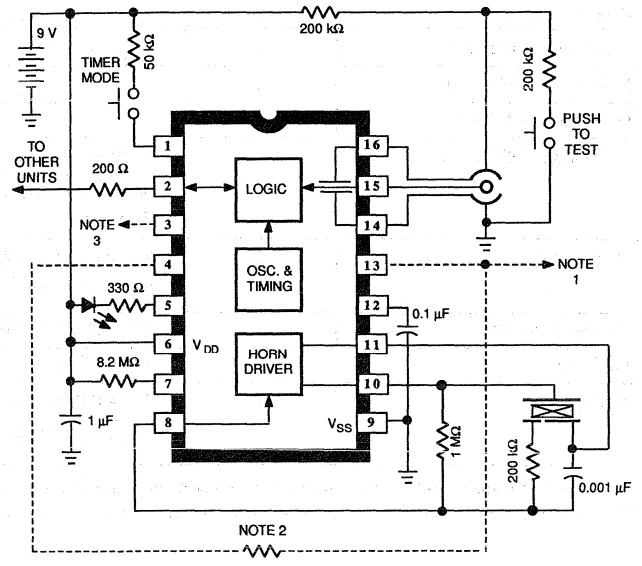
Low Battery. The low battery threshold is set internally by a voltage divider connected between V_{DD} and V_{SS}. The threshold can be increased by connecting a resistor between pin 3 and V_{DD}. The threshold can be decreased by connecting a resistor between pin 3 and V_{SS}. The battery voltage level is checked every 40 seconds during the 10 mA, 10 ms LED pulse. If an LED is not used, it should be replaced with an equivalent resistor (typically 500 Ω to 1000 Ω) such that the battery loading remains at 10 mA.

Timer. An internal timer is provided that can be used in various configurations to allow for a period of reduced smoke detector sensitivity. When a high-to-low transition occurs at pin 1, the internal timer is reset, the timer mode enabled, and the circuit reset to a no alarm condition. The LED will flash at a 10 second rate. If the level of smoke is increased such that the reduced sensitivity level is reached, the device will go into the alarm condition. The timer, however, will continue to completion of the nominal 10-1/4 minute period (368 clock cycles).

I/O. A connection is provided at pin 2 to allow multiple smoke detectors to be commoned. If any single unit detects smoke (I/O is driven high), all connected units will sound their associated horns after a nominal 3 second delay. The LED is suppressed when an alarm is signaled from an interconnected unit.

Testing. On power up, all internal counters are reset. Internal test circuitry allows for low battery check by holding pins 8 and 12 low during power up, then reducing V_{DD} and monitoring $HORN_1$ (pin 10). All functional tests can be accelerated by driving pin 12 with a 2 kHz square wave. The 10 ms strobe period must be maintained for proper operation of the comparator circuitry.

TYPICAL APPLICATION



Dwg. EC-005

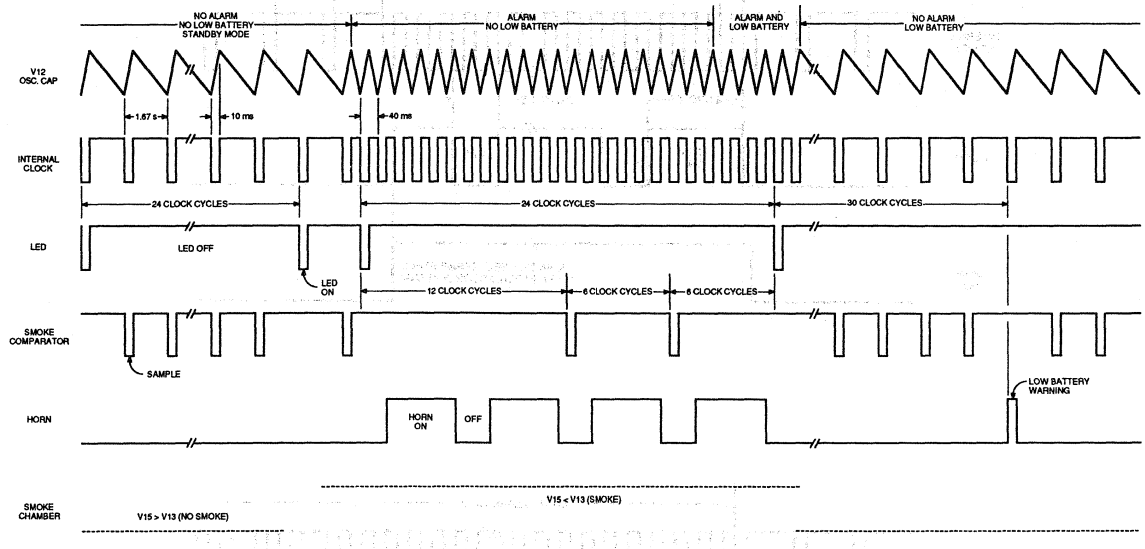
NOTE 1: Use an external resistor to adjust sensitivity for a particular smoke chamber.

NOTE 2: Select resistor to reduce sensitivity during timer mode.

NOTE 3: A resistor to ground or V_{DD} may be added to this pin to modify low battery voltage threshold.

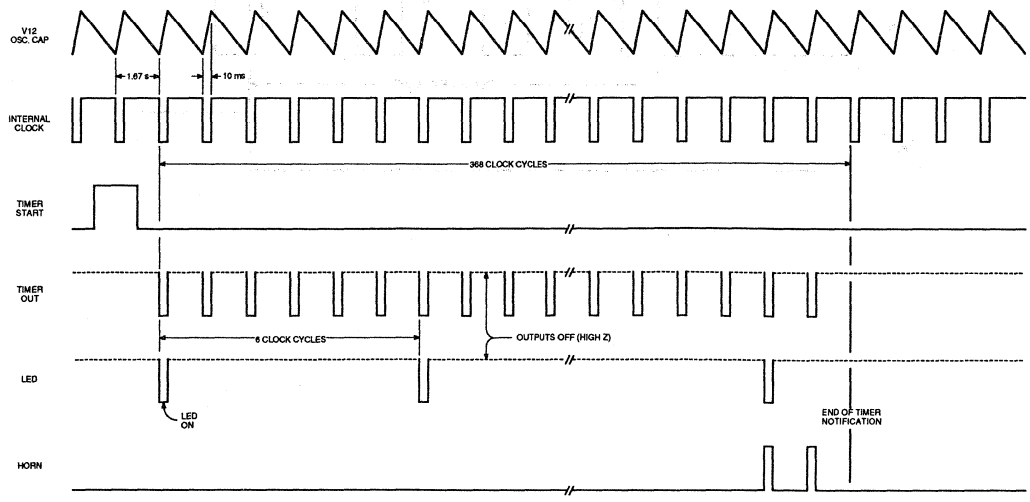
TIMING DIAGRAMS IN TYPICAL APPLICATION

NON-TIMER MODE



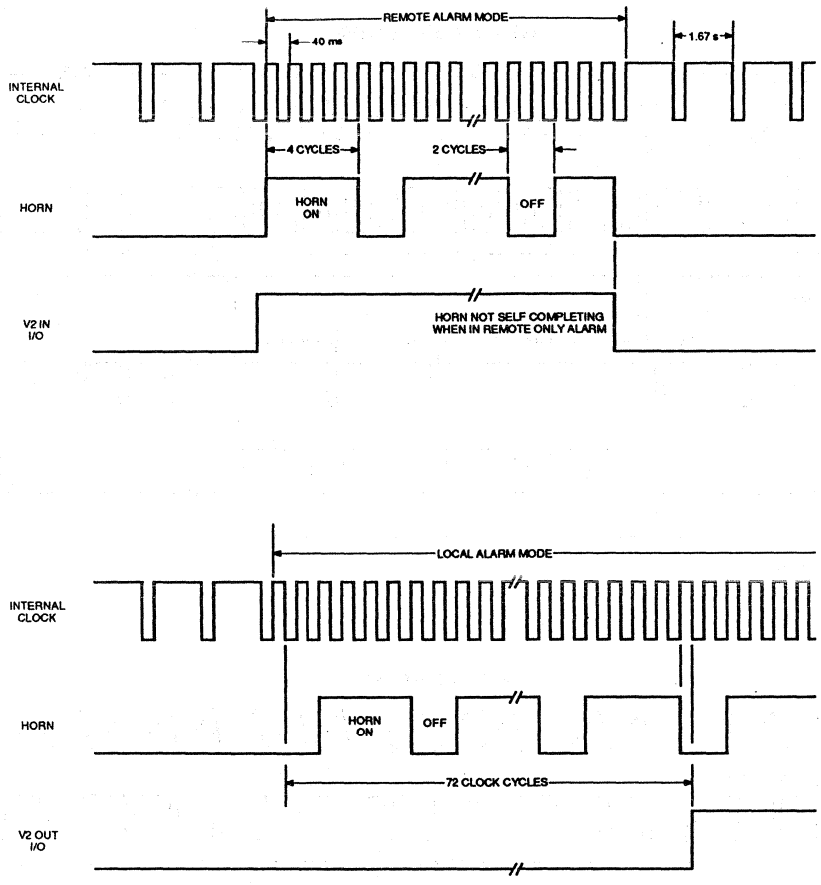
Dwg. WC-003

TIMER MODE



Dwg. WC-005

I/O OPERATION

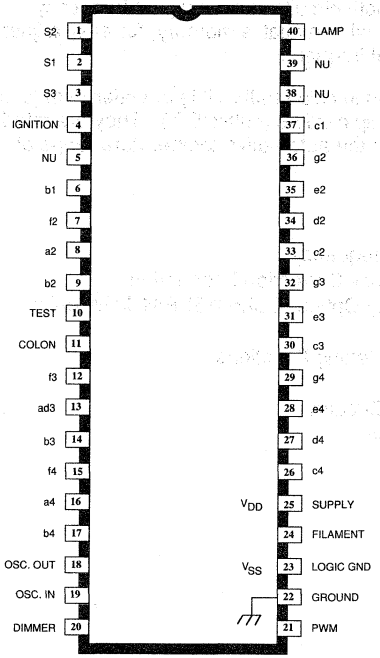


Dwg. WC-004

5458/63/74, 5604

2-FUNCTION, 4-DIGIT VF AUTOMOTIVE CLOCKS

SCL5604E



NOTE: b1 = SEGMENT b, DIGIT 1

Dwg. PC-002

ABSOLUTE MAXIMUM RATINGS

Logic Supply Current, I_{SS} ..... **-7.0 mA**
Total Supply Current, I_{DD} ..... **20 mA**
Input Voltage Range (Ref. V_{SS}),
V_{IN} ..... **-0.5 V to V_{DD} + 0.5 V**
Input Current, I_{IN} ..... **±10 mA**
Package Power Dissipation, P_D ... **300 mW**
Operating Temperature Range,
T_A ..... **-40°C to +85°C**
Storage Temperature Range,
T_S ..... **-65°C to +150°C**

Caution: These CMOS devices have static protection but are susceptible to damage if exposed to extremely high static electrical charges.

These devices are 2-function digital automotive clock circuits fabricated on a single monolithic chip using CMOS technology. They feature low cost, low power, and high reliability. The six devices in this series offer a variety of display and setting options and provide all of the functions normally desired in a 4-digit automotive clock.

All versions provide a push-button "time tone" setting that will zero the minutes and seconds counters if the displayed time is within two minutes of the hour. This feature allows the user to instantly set the clock according to the time tone commonly provided on radio stations.

The display driver outputs will directly drive standard vacuum fluorescent displays. A dimmer input controls the display intensity by varying the pulse width rather than by lowering the output voltage. This technique results in a more uniform display intensity. The rise and fall times of the output drivers are optimized to reduce RF interference.

All devices are supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row centers and are rated for continuous operation over the automotive temperature range of -40°C to +85°C. Other packages are available on special order.

Complete technical information on these devices is included with the SCL5233/38E.

FEATURES

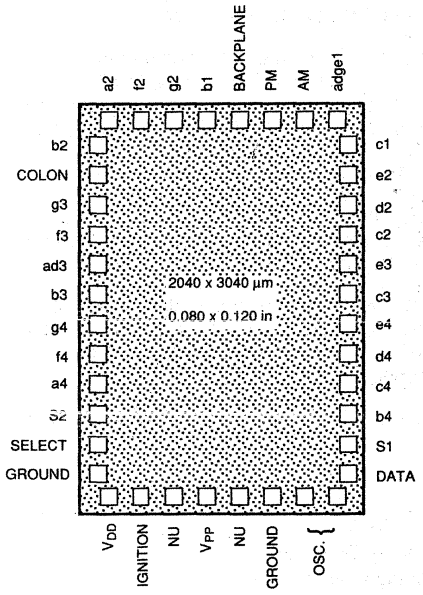
- Push-Button "Time Tone" Setting
- Variable Pulse-Width Display Dimming
- 12- or 24-Hour Timekeeping Option
- Rollover Protection on Minutes Set
- High Noise Immunity
- Diode Protection on all Inputs
- RFI/EMI Minimized

Always order by complete part number, e.g. **SCL5458E** .

5615 AND 5616

2-FUNCTION, 4-DIGIT LCD AUTOMOTIVE CLOCKS—PROGRAMMABLE

SCL5615HN/HW or SCL5616HN/HW



Dwg. PC-001

ABSOLUTE MAXIMUM RATINGS

Supply Current, I_{DD} ..... **2.0 mA**
Input Voltage Range, V_{IN}
(except V_{PP}) .....**-0.3 V to V_{DD}**
(Programming
Power Voltage, V_{PP}) ..... **18.5 V**
Input Current (except V_{PP}), I_{IN} .....**±10 mA**
Power Dissipation, P_D ..... **300 mW**
Operating Temperature Range,
T_A .....**-40°C to +85°C**
Storage Temperature Range,
T_S .....**-65°C to +150°C**

Caution: These CMOS devices have static protection, but are susceptible to damage if exposed to extremely high static electrical charges.

The SCL5615EP/HN/HW and SCL5616EP/HN/HW are 2-function digital automotive clock circuits. Fabricated on a single monolithic chip using silicon-gate CMOS PROM technology, they offer low cost, low power, and high reliability. Both circuits include digital frequency correction, stored in the internal nonvolatile memory, for easy adjustment of the oscillator nominal frequency.

Both devices are supplied in chip (suffix 'HN') or wafer form (suffix 'HW'), or in 40-lead plastic chip carriers (suffix 'EP'). They are rated for continuous operation over the automotive temperature range of -40°C to +85°C.

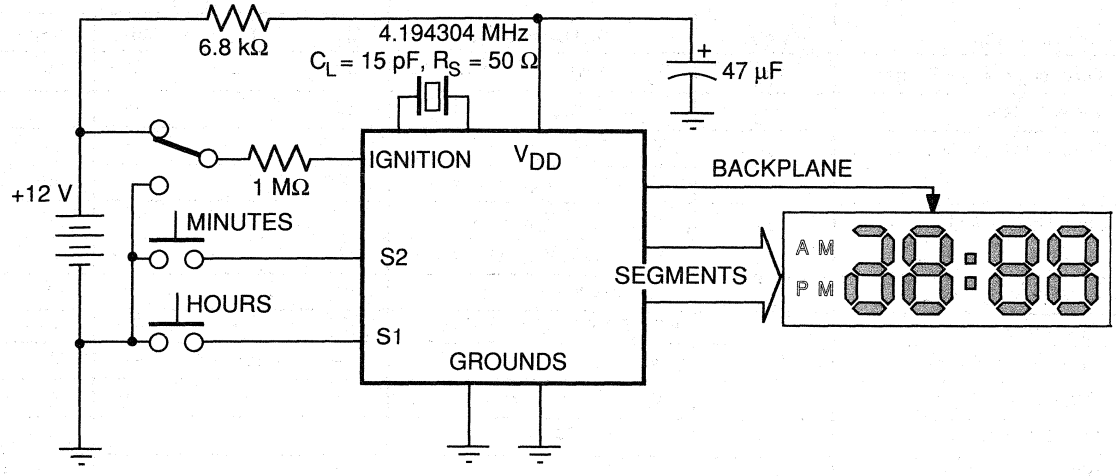
FEATURES

- Digital Tuning of Crystal Frequency
- PROM for Storing Frequency Correction Information
- 12 or 24 Hour Timekeeping Option (SCL5616EP/HN/HW only)
- Flashing Colon
- Two Switches Control All Setting Functions
- High Noise Immunity
- Internal Power-Up Reset Circuitry
- Internal Voltage Regulation

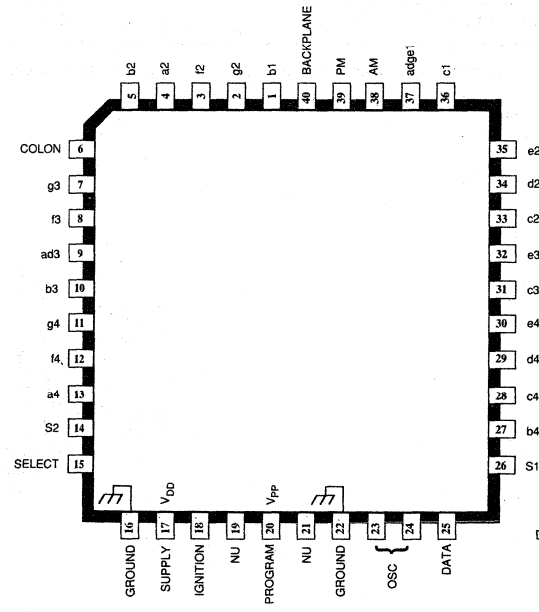
Always order by complete part number:

Part Number	Function	Style
SCL5615EP	12 Hour mode	40-Lead PLCC
SCL5615HN		Dice in Waffle Pack
SCL5615HW		Dice in Wafer Form
SCL5616EP	12 or 24 Hour mode	40-Lead PLCC
SCL5616HN		Dice in Waffle Pack
SCL5616HW		Dice in Wafer Form

TYPICAL APPLICATION



SCL5615EP or SCL5616EP

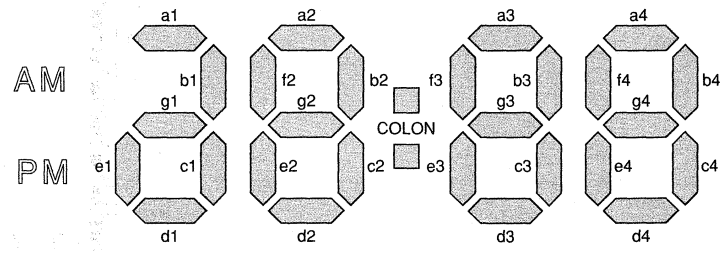


ELECTRICAL CHARACTERISTICS at T_A = -40°C to +85°C, in Typical Application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operating Voltage Range	V_{DD}	T_A = +25°C	4.5	—	—	V
Zener Voltage	V_{DD}	I_{DD} = 1.0 mA	5.5	—	6.8	V
Segment Output Current	I_{OUT}	V_{DD} = 5.0 V, V_{OUT} = 4.8 V	-20	—	—	µA
		V_{DD} = 5.0 V, V_{OUT} = 0.2 V	120	—	—	µA
Backplane Output Current	I_{OUT}	V_{DD} = 5.0 V, V_{OUT} = 4.8 V	-80	—	—	µA
		V_{DD} = 5.0 V, V_{OUT} = 0.2 V	240	—	—	µA
LCD Drive Signal	V_{DISP}	V_{DD} ≥5.0 V	4.0	—	—	V
Input Current	I_{IN}	S1, S2, DATA, or SELECT	-55	—	-700	µA
Oscillator Frequency	f_{OSC}		—	4.194 304	—	MHz
Oscillator Starting Time	t_{OSC}	V_{DD} = Zener voltage	—	—	200	ms
Oscillator Stability	Δf_{OSC}	ΔV_{DD} = ±100 mV	—	—	±1.0	ppM
Backplane Frequency	f_{BP}		—	64	—	Hz
Switch Debounce Time	t_{DB}		0	—	62.5	ms
Osc. Feedback Resistance	R_{OSC}		—	16	—	MΩ
Osc. Input Capacitance	C_{OSCI}		—	15	—	pF
Osc. Output Capacitance	C_{OSCO}		—	30	—	pF
Supply Current	I_{DD}	V_{DD} = 5.0 V	—	—	1.0	mA

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

DISPLAY FORMAT



Dwg. OC-001

FUNCTIONAL DESCRIPTION

DATA Logic Levels are V_{DD} and Ground

Power-Up Reset. When power up occurs, the hours and minutes counters are reset, and the clock starts running:

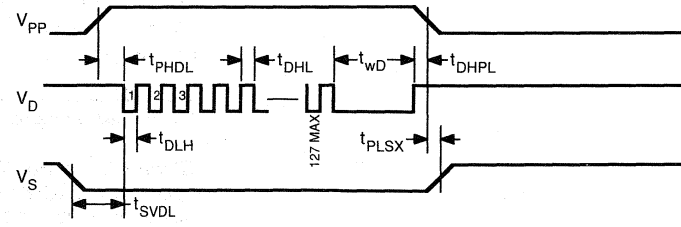
Device	Operation
SCL5615EP/HN/HW	24-Hour mode and counting starts from 0:00
SCL5616EP/HN/HW	12-Hour mode and counting starts from 1:00 AM

Programming Modes. Data is loaded by pulling DATA low (1 µs pulse duration) n times to set the desired bits for frequency correction into the data input register. This information is latched in the RAM, thus allowing the testing of the oscillator frequency adjustment without storing the selected pattern in the PROM cells. The data latched in the RAM is stored in the PROM cells when DATA is held low for a minimum of 10 ms.

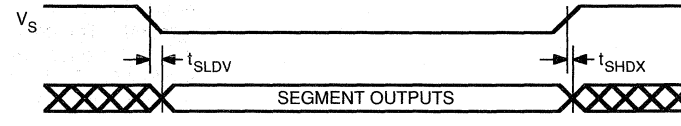
The data stored in the data input register is cleared on any SELECT transition (low to high or high to low). It is also cleared when the program power voltage (V_{PP}) is reduced from 18 V to V_{DD}. Clearing the data input register does not affect the data latched in the RAM.

Program V_{PP}	DATA V_D	SELECT V_S	Operation
18 V	Pulse	Ground	DATA load for frequency correction
18 V	Ground	V_{DD}	DATA store
V_{DD}	V_{DD}	Ground	Verify stored data

FREQUENCY CORRECTION



VERIFY CYCLE ($V_{PP} = V_{DD}$)



Dwg. WC-001-1

Frequency Correction. The on-chip oscillator circuit increases the crystal frequency approximately 40 ppm. This ensures that the typical crystal will operate within the tuning range. With V_S at ground, data pulses are then used to trim the internal clock frequency by 2 to 254 ppm to the required value. The quantity of data pulses needed (1 to 127) is

$$n = \frac{f_{BP} - 64}{128 \times 10^{-6}}$$

where f_{BP} is the measured frequency at BACKPLANE. Prior to trimming, it must be between 64.000 128 Hz and 64.016 256 Hz.

Operating Modes. The operating modes of the clock are controlled by the voltages applied to V_{PP}, SELECT, IGNITION, and switches S1 and S2.

Program V_{PP}	SELECT V_S	S1	S2	IGNITION	Mode
V_{DD}	V_{DD}	Open	Open	X	Clock running
V_{DD}	V_{DD}	Ground	Ground	12 V	Diagnostic
18 V	Ground	Open	Open	X	Programming

X = Irrelevant, ground or 12 V

Clock Running Mode. During the clock running mode, setting functions are achieved by either momentary or continuous operation of switches S1 and S2, which are enabled by IGNITION. Hours or minutes are incremented on S1 or S2 (respectively) depression and continue at a 1 Hz rate while the switch is depressed.

S1	S2	IGNITION	Operation
Open	Open	X	Clock running
X	X	Ground	Setting disabled
Ground	Open	12 V	Set hours
Open	Ground	12 V	Set Minutes
Ground	Ground	12 V	Change counting sequence (12 to 24 hour or 24 to 12 hour; SCL5616EP/HN/HW only)

X = Irrelevant, ground or 12 V for IGNITION, ground or open for S1 and S2

Diagnostic Mode. To enter the diagnostic mode, S1 and S2 are operated with IGNITION connected to 12 V. All segments are displayed for as long as S1 and S2 are depressed. On opening S1 and S2, the clock will leave the diagnostic mode and go through a power-up sequence. In the SCL5616EP/HN/HW, the counting sequence will change (from 12 hour to 24 hour or from 24 hour to 12 hour). To inhibit the power-up reset, hold the DATA input low (ground). The counting mode will change without resetting the hours or minutes counters. The counting sequence is forced to 12 hour in the SCL5615EP/HN/HW. In that case, operation of S1 or S2 will not affect the counting sequence.

Stored Data Verification. In the verify mode, the complement value of the information stored in the PROM cells is brought out directly to the segment output terminals for easy verification of the stored data. If a bit is programmed (high), the appropriate segment output is turned ON (low). The segments represent the binary equivalent of the number of frequency correction data pulses entered.

Frequency Selection Pulses	64	32	16	8	4	2	1
Segment	b4	c4	d4	e4	c3	e3	c2

RECOMMENDED FLASH PROGRAMMING CHARACTERISTICS
at T_A = +25°C, Logic Levels are V_{DD} and Ground (except PROGRAM High)

Characteristic	Symbol	Min.	Max.	Units
PROGRAM High (18 V) to DATA Low	t_{PHDL}	1.0	—	µs
SELECT Valid to DATA Low	t_{SVDL}	25	—	µs
DATA Low to DATA High	t_{DLH}	1.0	1.5	µs
DATA High to DATA Low	t_{DHL}	1.0	—	µs
DATA Store Pulse Duration	t_{wD}	10	—	ms
DATA High to PROGRAM Low	t_{DHPL}	1.0	—	µs
PROGRAM Low to SELECT Change	t_{PLSX}	1.0	—	µs
SELECT Low (Verify) to DATA Valid	t_{SLDV}	—	1.0	µs
DATA Hold from End of Verify	t_{SHDX}	—	10	ns

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HALL-EFFECT & OPTOELECTRONIC SENSOR ICs 4

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PACKAGE INFORMATION 9

SECTION 7. TECHNICAL DATA
for Discrete Transistors, Diodes, and Arrays

Quick Guide to Discrete Devices 7-1
Discrete Semiconductors Index and Cross Reference 7-2
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- PNP Bipolar Transistors 7-19
- N-Channel Junction Field-Effect Transistors 7-21
- P-Channel Junction Field-Effect Transistors 7-27
- General-Purpose and Schottky Diodes 7-29
- Zener Diodes 7-30

Transistor and Diode Arrays 7-33
Chips-In-DIPs (Custom Arrays) 7-41
See Also:
- High-Current Darlington Transistor Arrays ..... Section 3
- Discrete and Integrated Circuit Semiconductor Chips ..... Brochure CN-193

QUICK GUIDE

TO ALLEGRO DISCRETE DEVICES

Series 1N	JEDEC-registered general-purpose and Zener diodes. See Series TMPD and TMPZ.
Series 2N	JEDEC-registered general-purpose, small-signal, switching, and field-effect transistors in TO-92/TO-226AA plastic packages. See also Series TMPF, TMPT, and TP.
Series BA	Pro-Electron registered diodes in SOT-23/TO-236AB surface-mount packages.
Series BC	Pro-Electron registered general-purpose transistors.
Series BF	Pro-Electron registered general-purpose, N-channel JFETs in TO-92/TO-226AA plastic packages.
Series BZX84	Pro-Electron registered Zener diodes in SOT-23/TO-236AB surface-mount packages. Nominal voltage ratings from 3.9 volts to 56 volts are available.
Series J	General-purpose, JFETs in TO-92/TO-226AA plastic packages.
Series MPS	General-purpose transistors in TO-92/TO-226AA plastic packages; generally with E-B-C pinning.
Series TH-	Discrete semiconductors in unpackaged, chip form. See Brochure CN-193 for additional information.
Series TMPD	General-purpose, Schottky, and dual diodes in SOT-23/TO-236AB surface-mount packages.
Series TMPF	General-purpose, JFETs in SOT-23/TO-236AB surface-mount packages.
Series TMPT	General-purpose, small-signal, and switching transistors in SOT-23/TO-236AB surface-mount packages.
Series TMPZ	Zener diodes in SOT-23/TO-236AB surface-mount packages. Nominal voltage ratings from 4.3 volts to 33 volts are available. Also temperature-compensated 6.2 V and 6.4 V Zener diodes with temperature coefficients to less than +128 μV/°C.
Series TND	Diode arrays in 14- or 16-pin dual in-line plastic packages. Eight isolated diodes or arrays of 8 to 15 diodes in common-anode or common-cathode configurations are available .
TND8000	Three pairs of Schottky diodes in a 16-lead surface-mount package specifically for clamping three-phase brushless dc motors.
Series TP	General-purpose, small-signal, switching, and field-effect transistors in TO-92/TO-226AA plastic packages. Interchangeable with JEDEC-registered and industry-standard devices in TO-98/TO-226AD plastic packages.
TPP4000	Four isolated NPN Darlington transistors in a 14-pin dual in-line plastic package.
Series TPQ	Four isolated transistors in 14-pin dual in-line plastic packages. Quad NPN, quad PNP, and dual complementary pairs are available.
	See also, high-current multiple Darlington arrays in Section 3.

DISCRETE SEMICONDUCTORS

INDEX AND CROSS REFERENCE

Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	2	3	Ratings (Page)
1N914	Diode	TMPD914	TO-236AB	A	NC	K	7-29
1N4148	Diode	TMPD4148	TO-236AB	A	NC	K	7-29
1N4150	Diode	TMPD4150	TO-236AB	A	NC	K	7-29
1N4565	TC Zener	TMPZ4565	TO-236AB	A	K	NC	7-32
1N4565A	TC Zener	TMPZ4565A	TO-236AB	A	K	NC	7-32
1N4566	TC Zener	TMPZ4566	TO-236AB	A	K	NC	7-32
1N4566A	TC Zener	TMPZ4566A	TO-236AB	A	K	NC	7-32
1N4570	TC Zener	TMPZ4570	TO-236AB	A	K	NC	7-32
1N4570A	TC Zener	TMPZ4570A	TO-236AB	A	K	NC	7-32
1N4571	TC Zener	TMPZ4571	TO-236AB	A	K	NC	7-32
1N4571A	TC Zener	TMPZ4571A	TO-236AB	A	K	NC	7-32
1N4575	TC Zener	TMPZ4575	TO-236AB	A	K	NC	7-32
1N4575A	TC Zener	TMPZ4575A	TO-236AB	A	K	NC	7-32
1N4576	TC Zener	TMPZ4576	TO-236AB	A	K	NC	7-32
1N4576A	TC Zener	TMPZ4576A	TO-236AB	A	K	NC	7-32
1N5229	Zener	TMPZ5229	TO-236AB	A	NC	K	7-30
1N5230	Zener	TMPZ5230	TO-236AB	A	NC	K	7-30
1N5231	Zener	TMPZ5231	TO-236AB	A	NC	K	7-30
1N5232	Zener	TMPZ5232	TO-236AB	A	NC	K	7-30
1N5233	Zener	TMPZ5233	TO-236AB	A	NC	K	7-30
1N5234	Zener	TMPZ5234	TO-236AB	A	NC	K	7-30
1N5235	Zener	TMPZ5235	TO-236AB	A	NC	K	7-30
1N5236	Zener	TMPZ5236	TO-236AB	A	NC	K	7-30
1N5237	Zener	TMPZ5237	TO-236AB	A	NC	K	7-30
1N5238	Zener	TMPZ5238	TO-236AB	A	NC	K	7-30
1N5239	Zener	TMPZ5239	TO-236AB	A	NC	K	7-30
1N5240	Zener	TMPZ5240	TO-236AB	A	NC	K	7-30
1N5241	Zener	TMPZ5241	TO-236AB	A	NC	K	7-30
1N5242	Zener	TMPZ5242	TO-236AB	A	NC	K	7-30
1N5243	Zener	TMPZ5243	TO-236AB	A	NC	K	7-30

All devices are available in unpackaged, chip form. See Brochure CN-193.

DISCRETE SEMICONDUCTORS
INDEX AND CROSS REFERENCE

Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	2	3	Ratings (Page)
1N5244	Zener	TMPZ5244	TO-236AB	A	NC	K	7-30
1N5245	Zener	TMPZ5245	TO-236AB	A	NC	K	7-30
1N5246	Zener	TMPZ5246	TO-236AB	A	NC	K	7-30
1N5247	Zener	TMPZ5247	TO-236AB	A	NC	K	7-30
1N5248	Zener	TMPZ5248	TO-236AB	A	NC	K	7-30
1N5249	Zener	TMPZ5249	TO-236AB	A	NC	K	7-30
1N5250	Zener	TMPZ5250	TO-236AB	A	NC	K	7-30
1N5251	Zener	TMPZ5251	TO-236AB	A	NC	K	7-30
1N5252	Zener	TMPZ5252	TO-236AB	A	NC	K	7-30
1N5253	Zener	TMPZ5253	TO-236AB	A	NC	K	7-30
1N5254	Zener	TMPZ5254	TO-236AB	A	NC	K	7-30
1N5255	Zener	TMPZ5255	TO-236AB	A	NC	K	7-30
1N5256	Zener	TMPZ5256	TO-236AB	A	NC	K	7-30
1N5257	Zener	TMPZ5257	TO-236AB	A	NC	K	7-30
1N5711	Schottky	TMPD5711	TO-236AB	A	NC	K	7-29
2N918	NPN	TMPT918	TO-236AB	B	E	C*	7-17
		TP918	TO-226AA	E	B	C	7-15
2N2221	NPN	TMPT2221	TO-236AB	B	E	C*	7-17
		TP2221	TO-226AA	E	B	C	7-15
2N2221A	NPN	TMPT2221A	TO-236AB	B	E	C*	7-17
		TP2221A	TO-226AA	E	B	C	7-15
2N2222	NPN	TMPT2222	TO-236AB	B	E	C*	7-17
		TP2222	TO-226AA	E	B	C	7-15
		TPQ2222	14-Pin DIP	Quad Transistor Array			7-38
		TPQ6002	14-Pin DIP	Dual Complementary Pair			7-38
		TPQ6502	14-Pin DIP	Dual Complementary Pair			7-38
2N2222A	NPN	TMPT2222A	TO-236AB	B	E	C*	7-17
		TP2222A	TO-226AA	E	B	C	7-15
		TPQ2222A	14-Pin DIP	Quad Transistor Array			7-38
2N2369		TPQ2369	14-Pin DIP	Quad Transistor Array			7-38
2N2907	PNP	TMPT2907	TO-236AB	B	E	C*	7-20
		TP2907	TO-226AA	E	B	C	7-19
		TPQ2907	14-Pin DIP	Quad Transistor Array			7-38
		TPQ6002	14-Pin DIP	Dual Complementary Pair			7-38
		TPQ6502	14-Pin DIP	Dual Complementary Pair			7-38

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

DISCRETE SEMICONDUCTORS
INDEX AND CROSS REFERENCE

Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	2	3	Ratings (Page)
2N2907A	PNP	TMPT2907A	TO-236AB	B	E	C*	7-20
		TP2907A	TO-226AA	E	B	C	7-19
		TPQ2907A	14-Pin DIP	Quad Transistor Array			7-38
2N3414	NPN	2N3414	TO-226AA	E	C	B	7-15
2N3415	NPN	2N3415	TO-226AA	E	C	B	7-15
2N3416	NPN	2N3416	TO-226AA	E	C	B	7-15
2N3417	NPN	2N3417	TO-226AA	E	C	B	7-15
2N3819	N Channel	2N3819	TO-226AA	D	G	S†	7-21
		TMPF3819	TO-236AB	D	S	G	7-24
2N3820	P Channel	TMPF3820	TO-236AB	D	S	G	7-28
		2N3820	TO-226AA	D	G	S†	7-27
2N3821	N Channel	TMPF3821	TO-236AB	D	S	G	7-24
		TP3821	TO-226AA	D	S	G‡	7-21
2N3822	N Channel	TMPF3822	TO-236AB	D	S	G	7-24
		TP3822	TO-226AA	D	S	G‡	7-21
2N3823	N Channel	TMPF3823	TO-236AB	D	S	G	7-24
		TP3823	TO-226AA	D	S	G‡	7-21
2N3824	N Channel	TMPF3824	TO-236AB	D	S	G	7-24
		TP3824	TO-226AA	D	S	G‡	7-21
2N3904	NPN	2N3904	TO-226AA	E	B	C	7-15
		TMPT3904	TO-236AB	B	E	C*	7-18
		TPQ3904	14-Pin DIP	Quad Transistor Array			7-38
		TPQ6700	14-Pin DIP	Dual Complementary Pair			7-38
2N3906	PNP	2N3906	TO-226AA	E	B	C	7-19
		TMPT3906	TO-236AB	B	E	C*	7-20
		TPQ3906	14-Pin DIP	Quad Transistor Array			7-38
		TPQ6700	14-Pin DIP	Quad Transistor Array			7-38
2N3993	P Channel	TMPF3993	TO-236AB	D	S	G	7-28
		TP3993	TO-226AA	D	S	G‡	7-27
2N3994	P Channel	TMPF3994	TO-236AB	D	S	G	7-28
		TP3994	TO-226AA	D	S	G‡	7-27
2N4091	N Channel	TMPF4091	TO-236AB	D	S	G	7-24
		TP4091	TO-226AA	D	S	G‡	7-21
2N4092	N Channel	TMPF4092	TO-236AB	D	S	G	7-24
		TP4092	TO-226AA	D	S	G‡	7-21

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

† Reversed pinning (S-G-D) available on special order—add suffix letter 'R' to part number.

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

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2N4093	N Channel	TMPF4093	TO-236AB	D	S	G	7-24
		TP4093	TO-226AA	D	S	G‡	7-21
2N4117	N Channel	TMPF4117	TO-236AB	D	S	G	7-24
		TP4117	TO-226AA	D	S	G‡	7-21
2N4118	N Channel	TMPF4118	TO-236AB	D	S	G	7-24
		TP4118	TO-226AA	D	S	G‡	7-21
2N4119	N Channel	TMPF4119	TO-236AB	D	S	G	7-24
		TP4119	TO-226AA	D	S	G‡	7-21
2N4220	N Channel	TMPF4220	TO-236AB	D	S	G	7-24
		TP4220	TO-226AA	D	S	G‡	7-21
2N4221	N Channel	TMPF4221	TO-236AB	D	S	G	7-24
		TP4221	TO-226AA	D	S	G‡	7-21
2N4222	N Channel	TMPF4222	TO-236AB	D	S	G	7-24
		TP4222	TO-226AA	D	S	G‡	7-21
2N4223	N Channel	TMPF4223	TO-236AB	D	S	G	7-24
		TP4223	TO-226AA	D	S	G‡	7-21
2N4224	N Channel	TMPF4224	TO-236AB	D	S	G	7-24
		TP4224	TO-226AA	D	S	G‡	7-21
2N4381	P Channel	TMPF4381	TO-236AB	D	S	G	7-28
		TP4381	TO-226AA	D	S	G‡	7-27
2N4391	N Channel	TMPF4391	TO-236AB	D	S	G	7-24
		TP4391	TO-226AA	D	S	G‡	7-21
2N4392	N Channel	TMPF4392	TO-236AB	D	S	G	7-24
		TP4392	TO-226AA	D	S	G‡	7-21
2N4393	N Channel	TMPF4393	TO-236AB	D	S	G	7-24
		TP4393	TO-226AA	D	S	G‡	7-21
2N4401	NPN	2N4401	TO-226AA	E	B	C	7-15
		TMPT4401	TO-236AB	B	E	C*	7-18
2N4402	PNP	2N4402	TO-226AA	E	B	C	7-19
		TMPT4402	TO-236AB	B	E	C*	7-20
2N4403	PNP	2N4403	TO-226AA	E	B	C	7-19
		TMPT4403	TO-236AB	B	E	C*	7-20
2N4413	PNP	TP4413	TO-226AA	E	B	C	7-19
2N4415	PNP	TP4415	TO-226AA	E	B	C	7-19

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

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2N4416	N Channel	TMPF4416	TO-236AB	D	S	G	7-24
		TP4416	TO-226AA	D	S	G‡	7-21
2N4416A	N Channel	TMPF4416A	TO-236AB	D	S	G	7-24
		TP4416A	TO-226AA	D	S	G‡	7-21
2N4424	NPN	2N4424	TO-226AA	E	C	B	7-15
2N4856	N Channel	TMPF4856	TO-236AB	D	S	G	7-24
		TP4856	TO-226AA	D	S	G‡	7-21
2N4857	N Channel	TMPF4857	TO-236AB	D	S	G	7-24
		TP4857	TO-226AA	D	S	G‡	7-21
2N4858	N Channel	TMPF4858	TO-236AB	D	S	G	7-24
		TP4858	TO-226AA	D	S	G‡	7-21
2N4859	N Channel	TMPF4859	TO-236AB	D	S	G	7-24
		TP4859	TO-226AA	D	S	G‡	7-21
2N4860	N Channel	TMPF4860	TO-236AB	D	S	G	7-24
		TP4860	TO-226AA	D	S	G‡	7-21
2N4861	N Channel	TMPF4861	TO-236AB	D	S	G	7-24
		TP4861	TO-226AA	D	S	G‡	7-21
2N5086	PNP	2N5086	TO-226AA	E	B	C	7-19
		TMPT5086	TO-236AB	B	E	C*	7-20
2N5087	PNP	2N5087	TO-226AA	E	B	C	7-19
		TMPT5087	TO-236AB	B	E	C*	7-20
2N5088	NPN	2N5088	TO-226AA	E	B	C	7-15
		TMPT5088	TO-236AB	B	E	C*	7-18
2N5089	NPN	2N5089	TO-226AA	E	B	C	7-15
		TMPT5089	TO-236AB	B	E	C*	7-18
2N5163	N Channel	TMPF5163	TO-236AB	D	S	G	7-24
		TP5163	TO-226AA	D	S	G‡	7-21
2N5172	NPN	2N5172	TO-226AA	E	C	B	7-15
2N5245	N Channel	TMPF5245	TO-236AB	D	S	G	7-24
		TP5245	TO-226AA	D	S	G‡	7-21
2N5246	N Channel	TMPF5246	TO-236AB	D	S	G	7-24
		TP5246	TO-226AA	D	S	G‡	7-21
2N5247	N Channel	TMPF5247	TO-236AB	D	S	G	7-24
		TP5247	TO-226AA	D	S	G‡	7-21

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

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2N5248	N Channel	TMPF5248	TO-236AB	D	S	G	7-24
		TP5248	TO-226AA	D	S	G‡	7-21
2N5307	NPN	2N5307	TO-226AA	E	C	B	7-15
2N5308	NPN	2N5308	TO-226AA	E	C	B	7-15
2N5358	N Channel	TMPF5358	TO-236AB	D	S	G	7-24
		TP5358	TO-226AA	D	S	G‡	7-21
2N5359	N Channel	TMPF5359	TO-236AB	D	S	G	7-24
		TP5359	TO-226AA	D	S	G‡	7-21
2N5360	N Channel	TMPF5360	TO-236AB	D	S	G	7-24
		TP5360	TO-226AA	D	S	G‡	7-21
2N5361	N Channel	TMPF5361	TO-236AB	D	S	G	7-25
		TP5361	TO-226AA	D	S	G‡	7-21
2N5362	N Channel	TMPF5362	TO-236AB	D	S	G	7-25
		TP5362	TO-226AA	D	S	G‡	7-21
2N5363	N Channel	TMPF5363	TO-236AB	D	S	G	7-25
		TP5363	TO-226AA	D	S	G‡	7-21
2N5364	N Channel	TMPF5364	TO-236AB	D	S	G	7-25
		TP5364	TO-226AA	D	S	G‡	7-21
2N5376	NPN	TP5376	TO-226AA	E	B	C	7-15
2N5400	PNP	2N5400	TO-226AA	E	B	C	7-19
2N5401	PNP	2N5401	TO-226AA	E	B	C	7-19
		TMPT5401	TO-236AB	B	E	C*	7-20
		TPQ5401	14-Pin DIP	Quad Transistor Array			7-38
2N5457	N Channel	2N5457	TO-226AA	D	S	G‡	7-21
		TMPF5457	TO-236AB	D	S	G	7-25
2N5458	N Channel	2N5458	TO-226AA	D	S	G‡	7-22
		TMPF5458	TO-236AB	D	S	G	7-25
2N5459	N Channel	2N5459	TO-226AA	D	S	G‡	7-22
		TMPF5459	TO-236AB	D	S	G	7-25
2N5460	P Channel	2N5460	TO-226AA	D	S	G‡	7-27
		TMPF5460	TO-236AB	D	S	G	7-28
2N5461	P Channel	2N5461	TO-226AA	D	S	G‡	7-27
		TMPF5461	TO-236AB	D	S	G	7-28

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

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2N5462	P Channel	2N5462	TO-226AA	D	S	G‡	7-27
		TMPF5462	TO-236AB	D	S	G	7-28
2N5484	N Channel	2N5484	TO-226AA	D	S	G‡	7-22
		TMPF5484	TO-236AB	D	S	G	7-25
2N5485	N Channel	2N5485	TO-226AA	D	S	G‡	7-22
		TMPF5485	TO-236AB	D	S	G	7-25
2N5486	N Channel	2N5486	TO-226AA	D	S	G‡	7-22
		TMPF5486	TO-236AB	D	S	G	7-25
2N5638	N Channel	2N5638	TO-226AA	D	S	G‡	7-22
		TMPF5638	TO-236AB	D	S	G	7-25
2N5639	N Channel	2N5639	TO-226AA	D	S	G‡	7-22
		TMPF5639	TO-236AB	D	S	G	7-25
2N5640	N Channel	2N5640	TO-226AA	D	S	G‡	7-22
		TMPF5640	TO-236AB	D	S	G	7-25
2N5653	N Channel	2N5653	TO-226AA	D	S	G‡	7-22
		TMPF5653	TO-236AB	D	S	G	7-25
2N5654	N Channel	2N5654	TO-226AA	D	S	G‡	7-22
		TMPF5654	TO-236AB	D	S	G	7-25
2N5668	N Channel	TMPF5668	TO-236AB	D	S	G	7-25
		TP5668	TO-226AA	D	S	G‡	7-22
2N5669	N Channel	TMPF5669	TO-236AB	D	S	G	7-25
		TP5669	TO-226AA	D	S	G‡	7-22
2N5670	N Channel	TMPF5670	TO-236AB	D	S	G	7-25
		TP5670	TO-226AA	D	S	G‡	7-22
2N5949	N Channel	TMPF5949	TO-236AB	D	S	G	7-25
		TP5949	TO-266AA	D	S	G‡	7-22
2N5950	N Channel	TMPF5950	TO-236AB	D	S	G	7-25
		TP5950	TO-226AA	D	S	G‡	7-22
2N5951	N Channel	TMPF5951	TO-236AB	D	S	G	7-25
		TP5951	TO-226AA	D	S	G‡	7-22
2N5952	N Channel	TMPF5952	TO-236AB	D	S	G	7-25
		TP5952	TO-226AA	D	S	G‡	7-22
2N5953	N Channel	TMPF5953	TO-236AB	D	S	G	7-25
		TP5953	TO-226AA	D	S	G‡	7-22

All devices are available in unpackaged, chip form. See Brochure CN-193

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

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Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	2	3	Ratings (Page)
2N6427	NPN	2N6427	TO-226AA	E	B	C	7-15
		TMPT6427	TO-236AB	B	E	C*	7-18
		TPQ6427	14-Pin DIP	Quad Transistor Array			7-38
BAR18	Schottky	BAR18	TO-236AB	A	NC	K	7-29
BAS16	Diode	BAS16	TO-236AB	A	NC	K	7-29
BAS19	Diode	BAS19	TO-236AB	A	NC	K	7-29
BAS21	Diode	BAS21	TO-236AB	A	NC	K	7-29
BAV70	Dual Diode	BAV70	TO-236AB	A1	A2	K	7-29
BAV74	Dual Diode	BAV74	TO-236AB	A1	A2	K	7-29
BAV99	Dual Diode	BAV99	TO-236AB	A1	K2	AK	7-29
BAW56	Dual Diode	BAW56	TO-236AB	K1	K2	A	7-29
BC264A	N Channel	TMPFBC264A	TO-236AB	D	S	G	7-25
BC264B	N Channel	TMPFBC264B	TO-236AB	D	S	G	7-25
BC264C	N Channel	TMPFBC264C	TO-236AB	D	S	G	7-25
BC264D	N Channel	TMPFBC264D	TO-236AB	D	S	G	7-25
BCW29	PNP	BCW29	TO-236AB	B	E	C*	7-20
BCW30	PNP	BCW30	TO-236AB	B	E	C*	7-20
BCW31	NPN	BCW31	TO-236AB	B	E	C*	7-17
BCW32	NPN	BCW32	TO-236AB	B	E	C*	7-17
BCW33	NPN	BCW33	TO-236AB	B	E	C*	7-17
BCW60A	NPN	BCW60A	TO-236AB	B	E	C*	7-17
BCW60B	NPN	BCW60B	TO-236AB	B	E	C*	7-17
BCW60C	NPN	BCW60C	TO-236AB	B	E	C*	7-17
BCW60D	NPN	BCW60D	TO-236AB	B	E	C*	7-17
BCW61A	PNP	BCW61A	TO-236AB	B	E	C*	7-20
BCW61B	PNP	BCW61B	TO-236AB	B	E	C*	7-20
BCW61C	PNP	BCW61C	TO-236AB	B	E	C*	7-20
BCW61D	PNP	BCW61D	TO-236AB	B	E	C*	7-20
BCW65A	NPN	BCW65A	TO-236AB	B	E	C*	7-17
BCW65B	NPN	BCW65B	TO-236AB	B	E	C*	7-17
BCW66F	NPN	BCW66F	TO-236AB	B	E	C*	7-17
BCW66G	NPN	BCW66G	TO-236AB	B	E	C*	7-17
BCW67A	PNP	BCW67A	TO-236AB	B	E	C*	7-20
BCW67B	PNP	BCW67B	TO-236AB	B	E	C*	7-20
BCW68F	PNP	BCW68F	TO-236AB	B	E	C*	7-20

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

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Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	2	3	Ratings (Page)
BCW68G	PNP	BCW68G	TO-236AB	B	E	C*	7-20
BCW69	PNP	BCW69	TO-236AB	B	E	C*	7-20
BCW70	PNP	BCW70	TO-236AB	B	E	C*	7-20
BCW71	NPN	BCW71	TO-236AB	B	E	C*	7-17
BCW72	NPN	BCW72	TO-236AB	B	E	C*	7-17
BCX17	PNP	BCX17	TO-236AB	B	E	C*	7-20
BCX18	PNP	BCX18	TO-236AB	B	E	C*	7-20
BCX19	NPN	BCX19	TO-236AB	B	E	C*	7-17
BCX20	NPN	BCX20	TO-236AB	B	E	C*	7-17
BCX70G	NPN	BCX70G	TO-236AB	B	E	C*	7-17
BCX70H	NPN	BCX70H	TO-236AB	B	E	C*	7-17
BCX70J	NPN	BCX70J	TO-236AB	B	E	C*	7-17
BCX70K	NPN	BCX70K	TO-236AB	B	E	C*	7-17
BCX71G	PNP	BCX71G	TO-236AB	B	E	C*	7-20
BCX71H	PNP	BCX71H	TO-236AB	B	E	C*	7-20
BCX71J	PNP	BCX71J	TO-236AB	B	E	C*	7-20
BCX71K	PNP	BCX71K	TO-236AB	B	E	C*	7-20
BF244A	N Channel	BF244A	TO-226AA	D	G	S†	7-22
		TMPFBF244A	TO-236AB	D	S	G	7-25
BF244B	N Channel	BF244B	TO-226AA	D	G	S†	7-22
		TMPFBF244B	TO-236AB	D	S	G	7-25
BF244C	N Channel	BF244C	TO-226AA	D	G	S†	7-22
		TMPFBF244C	TO-236AB	D	S	G	7-25
BF246A	N Channel	BF246A	TO-226AA	D	G	S†	7-22
		TMPFBF246A	TO-236AB	D	S	G	7-25
BF246B	N Channel	BF246B	TO-226AA	D	G	S†	7-22
		TMPFBF246B	TO-236AB	D	S	G	7-25
BF246C	N Channel	BF246C	TO-226AA	D	G	S†	7-22
		TMPFBF246C	TO-236AB	D	S	G	7-25
BF256A	N Channel	BF256A	TO-226AA	D	G	S†	7-22
		TMPFBF256A	TO-236AB	D	S	G	7-25
BF256B	N Channel	BF256B	TO-226AA	D	G	S†	7-22
		TMPFBF256B	TO-236AB	D	S	G	7-25
BF256C	N Channel	BF256C	TO-226AA	D	G	S†	7-22
		TMPFBF256C	TO-236AB	D	S	G	7-25

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

† Reversed pinning (S-G-D) available on special order—add suffix letter 'R' to part number.

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BFR30	N Channel	BFR30	TO-226AA	D	S	G‡	7-22
BFR31	N Channel	BFR31	TO-226AA	D	S	G‡	7-22
BZX84C4V7	Zener	BZX84C4V7	TO-236AB	A	NC	K	7-31
BZX84C5V1	Zener	BZX84C5V1	TO-236AB	A	NC	K	7-31
BZX84C5V6	Zener	BZX84C5V6	TO-236AB	A	NC	K	7-31
BZX84C6V2	Zener	BZX84C6V2	TO-236AB	A	NC	K	7-31
BZX84C6V8	Zener	BZX84C6V8	TO-236AB	A	NC	K	7-31
BZX84C7V5	Zener	BZX84C7V5	TO-236AB	A	NC	K	7-31
BZX84C8V2	Zener	BZX84C8V2	TO-236AB	A	NC	K	7-31
BZX84C9V1	Zener	BZX84C9V1	TO-236AB	A	NC	K	7-31
BZX84C10	Zener	BZX84C10	TO-236AB	A	NC	K	7-31
BZX84C11	Zener	BZX84C11	TO-236AB	A	NC	K	7-31
BZX84C12	Zener	BZX84C12	TO-236AB	A	NC	K	7-31
BZX84C13	Zener	BZX84C13	TO-236AB	A	NC	K	7-31
BZX84C15	Zener	BZX84C15	TO-236AB	A	NC	K	7-31
BZX84C16	Zener	BZX84C16	TO-236AB	A	NC	K	7-31
BZX84C18	Zener	BZX84C18	TO-236AB	A	NC	K	7-31
BZX84C20	Zener	BZX84C20	TO-236AB	A	NC	K	7-31
BZX84C22	Zener	BZX84C22	TO-236AB	A	NC	K	7-31
BZX84C24	Zener	BZX84C24	TO-236AB	A	NC	K	7-31
BZX84C27	Zener	BZX84C27	TO-236AB	A	NC	K	7-31
BZX84C30	Zener	BZX84C30	TO-236AB	A	NC	K	7-31
BZX84C33	Zener	BZX84C33	TO-236AB	A	NC	K	7-31
J111	N Channel	J111	TO-226AA	D	S	G‡	7-22
		TMPFJ111	TO-236AB	D	S	G	7-25
J112	N Channel	J112	TO-226AA	D	S	G‡	7-22
		TMPFJ112	TO-236AB	D	S	G	7-25
J112A	N Channel	J112A	TO-226AA	D	S	G‡	7-22
		TMPFJ112A	TO-236AB	D	S	G	7-25
J113	N Channel	J113	TO-226AA	D	S	G‡	7-22
		TMPFJ113	TO-236AB	D	S	G	7-25
J113A	N Channel	J113A	TO-226AA	D	S	G‡	7-22
		TMPFJ113A	TO-236AB	D	S	G	7-26
J174	P Channel	J174	TO-226AA	D	G	S†	7-27
		TMPFJ174	TO-236AB	D	S	G	7-28
J175	P Channel	J175	TO-226AA	D	G	S†	7-27
		TMPFJ175	TO-236AB	D	S	G	7-28

All devices are available in unpackaged, chip form. See Brochure CN-193.

† Reversed pinning (S-G-D) available on special order—add suffix letter 'R' to part number.

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

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J176	P Channel	J176	TO-226AA	D	G	S†	7-27
		TMPFJ176	TO-236AB	D	S	G	7-28
J177	P Channel	J177	TO-226AA	D	G	S†	7-27
		TMPFJ177	TO-236AB	D	S	G	7-28
J201	N Channel	J201	TO-226AA	D	S	G	7-22
		TMPFJ201	TO-236AB	D	S	G	7-26
J202	N Channel	J202	TO-226AA	D	S	G	7-22
		TMPFJ202	TO-236AB	D	S	G	7-26
J203	N Channel	J203	TO-226AA	D	S	G	7-22
		TMPFJ203	TO-236AB	D	S	G	7-26
J230	N Channel	J230	TO-226AA	D	S	G	7-22
		TMPFJ230	TO-236AB	D	S	G	7-26
J231	N Channel	J231	TO-226AA	D	S	G	7-22
		TMPFJ231	TO-2M36AB	D	S	G	7-26
J232	N Channel	J232	TO-226AA	D	S	G	7-22
		TMPFJ232	TO-236AB	D	S	G	7-26
J304	N Channel	J304	TO-226AA	D	S	G	7-22
		TMPFJ304	TO-236AB	D	S	G	7-26
J305	N Channel	J305	TO-226AA	D	S	G‡	7-23
		TMPFJ305	TO-236AB	D	S	G	7-26
J308	N Channel	TMPFJ308	TO-236AB	D	S	G	7-26
		TPJ308	TO-226AA	D	S	G‡	7-23
J309	N Channel	TMPFJ309	TO-236AB	D	S	G	7-26
		TPJ309	TO-226AA	D	S	G‡	7-23
J310	N Channel	TMPFJ310	TO-236AB	D	S	G	7-26
		TPJ310	TO-226AA	D	S	G‡	7-23
MPS6520	NPN	MPS6520	TO-226AA	E	B	C	7-16
MPS6521	NPN	MPS6521	TO-226AA	E	B	C	7-16
MPSA05	NPN	MPSA05	TO-226AA	E	B	C	7-16
		TMPTA05	TO-236AB	B	E	C*	7-18
		TPQA05	14-Pin DIP	Quad Transistor Array			7-38
MPSA06	NPN	MPSA06	TO-226AA	E	B	C	7-16
		TMPTA06	TO-236AB	B	E	C*	7-18
		TPQA06	14-Pin DIP	Quad Transistor Array			7-38
MPSA14	NPN	MPSA14	TO-226AA	E	B	C	7-16
		TMPTA14	TO-236AB	B	E	C*	7-18

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

† Reversed pinning (S-G-D) available on special order—add suffix letter 'R' to part number.

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

DISCRETE SEMICONDUCTORS
INDEX AND CROSS REFERENCE

Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	2	3	Ratings (Page)
MPSA42	NPN	MPSA42	TO-226AA	E	B	C	7-16
		TMPTA42	TO-236AB	B	E	C*	7-18
MPSA43	NPN	MPSA43	TO-226AA	E	B	C	7-16
		TMPTA43	TO-236AB	B	E	C*	7-18
MPSA55	PNP	MPSA55	TO-226AA	E	B	C	7-19
		TMPTA55	TO-236AB	B	E	C*	7-20
		TPQA55	14-Pin DIP	Quad Transistor Array			7-38
MPSA56	PNP	MPSA56	TO-226AA	E	B	C	7-19
		TMPTA56	TO-236AB	B	E	C*	7-20
		TPQA56	14-Pin DIP	Quad Transistor Array			7-38
MPSA70	PNP	MPSA70	TO-226AA	E	B	C	7-19
		TMPTA70	TO-236AB	B	E	C*	7-20
TMPD...	Diode	Various	TO-236AB	A	NC	K	7-29
TMPD6916	Schottky	TMPD6916	TO-236AB	A	NC	K	7-29
TMPD6919	Schottky	TMPD6919	TO-236AB	A	NC	K	7-29
TMPD6924	Schottky	TMPD6924	TO-236AB	A	NC	K	7-29
TMPF...	JFET	See 2N...	TO-236AB	Various			See 2N...
TMPFBC...	JFET	See BC...	TO-236AB	Various			See BC...
TMPFBF...	JFET	See BC...	TO-236AB	Various			See BC...
TMPFJ...	JFET	See J...	TO-236AB	Various			See J...
TMPFU...	JFET	See U...	TO-236AB	Various			See U...
TMPT...	Transistor	See 2N...	TO-236AB	Various			See 2N...
TMPTA...	Transistor	See MPSA...	TO-236AB	Various			See MPSA...
TMPZ...	Zener	See 1N...	TO-236AB	Various			See 1N...
TND...	Array	TND...	14 or 16-Pin DIP	6-to-15 Diode Array			7-33
TND8000	Schottky	TND8000	16-Lead SOIC	6-Diode Array			7-34
TP...	Transistor	See 2N...	TO-226AA	Various			See 2N...
TPBC...	Transistor	See BC...	TO-226AA	Various			See BC...
TPJ...	JFET	See J...	TO-226AA	Various			See J...

All devices are available in unpackaged, chip form. See Brochure CN-193.

* Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

DISCRETE SEMICONDUCTORS
INDEX AND CROSS REFERENCE

Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	2	3	Ratings (Page)
TPP4000	Array	TPP4000	14-Pin DIP	Quad Darlington Array			7-36
TPQ...	Array	TPQ...	14-Pin DIP	Quad Darlington Array			7-38
TPU...	JFET	See U...	TO-226AA	Various			See U...
U304	P Channel	TMPFU304	TO-236AB	D	S	G	7-28
		TPU304	TO-226AA	D	S	G‡	7-27
U305	P Channel	TMPFU305	TO-236AB	D	S	G	7-28
		TPU305	TO-226AA	D	S	G‡	7-27
U306	P Channel	TMPFU306	TO-236AB	D	S	G	7-28
		TPU306	TO-226AA	D	S	G‡	7-27
U308	N Channel	TMPFU308	TO-236AB	D	S	G	7-26
		TPU308	TO-226AA	D	S	G‡	7-23
U309	N Channel	TMPFU309	TO-236AB	D	S	G	7-26
		TPU309	TO-226AA	D	S	G‡	7-23
U310	N Channel	TMPFU310	TO-236AB	D	S	G	7-26
		TPU310	TO-226AA	D	S	G‡	7-23
U1897	N Channel	TMPFU1897	TO-236AB	D	S	G	7-26
		TPU1897	TO-226AA	D	S	G‡	7-23
U1898	N Channel	TMPFU1898	TO-236AB	D	S	G	7-26
		TPU1898	TO-226AA	D	S	G‡	7-23
U1899	N Channel	TMPFU1899	TO-236AB	D	S	G	7-26
		TPU1899	TO-226AA	D	S	G‡	7-23

All devices are available in unpackaged, chip form. See Brochure CN-193

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

NPN TRANSISTORS

TO-92/TO-226AA

'2N' and 'TP' DEVICE TYPES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_C Max. (mA)	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain h_{FE} Max.	DC Current Gain @ I_C (mA)	DC Current Gain @ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
TP918	50	30	15	3.0	10	15	20	—	3.0	1.0	0.4	10	600	4.0	1.7	—	—	EBC
TP2221	500	60	30	5.0	10	50	40	120	150	10	0.4	150	250	20	8.0	—	—	EBC
TP2221A	500	75	40	6.0	10	60	40	120	150	10	0.3	150	250	20	8.0	225	—	EBC
TP2222	500	60	30	5.0	10	50	100	300	150	10	0.4	150	250	20	8.0	—	—	EBC
TP2222A	500	75	40	6.0	10	60	100	300	150	10	0.3	150	250	20	8.0	225	—	EBC
2N3414	500	25	25	5.0	100	25	75	225	2.0	4.5	0.3	50	—	—	—	—	—	ECB
2N3415	500	25	25	5.0	100	25	180	540	2.0	4.5	0.3	50	—	—	—	—	—	ECB
2N3416	500	50	50	5.0	100	50	75	225	2.0	4.5	0.3	50	—	—	—	—	—	ECB
2N3417	500	50	50	5.0	100	50	180	540	2.0	4.5	0.3	50	—	—	—	—	—	ECB
2N3904	200	60	40	6.0	50	30	100	300	10	1.0	0.2	10	300	10	4.0	—	5.0	EBC
2N4401	500	60	40	6.0	100	30	100	300	150	1.0	0.4	150	250	20	6.5	225	—	EBC
2N4424	500	40	40	5.0	100	25	180	540	2.0	4.5	0.3	50	—	—	—	—	—	ECB
2N5088	100	35	30	—	50	20	300	900	0.1	5.0	0.5	10	—	—	4.0	—	3.0	EBC
2N5089	100	30	25	—	50	15	400	1200	0.1	5.0	0.5	10	—	—	4.0	—	2.0	EBC
2N5172	500	25	25	5.0	100	25	100	500	10	10	0.25	10	—	—	10	—	—	ECB
2N5307	500	40	40	12	100	40	2k	20k	2.0	5.0	1.4	200	60	2.0	10	—	—	ECB
2N5308	500	40	40	12	100	40	7k	70k	2.0	5.0	1.4	200	60	2.0	10	—	—	ECB
TP5376	500	60	30	5.0	10	30	120	—	1.0	5.0	—	—	—	—	8.0	—	—	EBC
2N6427	500	40	40	12	50	30	10k	100k	10	5.0	1.2	50	130	10	7.0	—	10	EBC

NOTES: 1) Maximum at typical JEDEC conditions.
2) µA.
3) $V_{(BR)CES}/I_{CES}$, as applicable.
4) mA.
5) $V_{(BR)CER}$ at R = 10Ω.

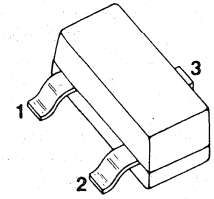
NPN TRANSISTORS
TO-92/TO-226AA

'MPS' DEVICE TYPES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_C Max. (mA)	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain h_{FE} Max.	DC Current Gain @ I_C (mA)	DC Current Gain @ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
MPS6520	200	40	25	4.0	50	30	200	400	2.0	10	0.5	50	—	—	3.5	—	3.0	EBC
MPS6521	200	40	25	4.0	50	30	300	600	2.0	10	0.5	50	—	—	3.5	—	3.0	EBC
MPSA05	800	60	60	4.0	100	60	50	—	100	1.0	0.25	100	100	10	—	—	—	EBC
MPSA06	800	80	80	4.0	100	80	50	—	100	1.0	0.25	100	100	10	—	—	—	EBC
MPSA14	500	30[3]	—	10	100	30	20k	—	100	5.0	1.5	100	125	10	—	—	—	EBC
MPSA42	500	300	300	6.0	100	200	40	—	30	10	0.5	20	50	10	3.0	—	—	EBC
MPSA43	500	200	200	6.0	100	160	40	—	30	10	0.5	20	50	10	4.0	—	—	EBC

NOTES: 1) Maximum at typical JEDEC conditions.
2) µA.
3) $V_{(BR)CES}/I_{CES}$, as applicable.
4) mA.
5) $V_{(BR)CER}$ at R = 10Ω.

NPN TRANSISTORS



SOT-23/TO-236AB

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Marking	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	h_{FE} Max.	@ I_C (mA)	@ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
BCW31	D1	30	20	5.0	100	20	110	220	2.0	5.0	0.25	10	—	—	4.0	—	10	BEC*
BCW32	D2	30	20	5.0	100	20	200	450	2.0	5.0	0.25	10	—	—	4.0	—	10	BEC*
BCW33	D3	30	20	5.0	100	20	420	800	2.0	5.0	0.25	10	—	—	4.0	—	10	BEC*
BCW60A	AA	32[3]	32	5.0	20	32	120	220	2.0	5.0	0.35	10	125	10	4.5	—	6.0	BEC*
BCW60B	AB	32[3]	32	5.0	20	32	180	310	2.0	5.0	0.35	10	125	10	4.5	—	6.0	BEC*
BCW60C	AC	32[3]	32	5.0	20	32	250	460	2.0	5.0	0.35	10	125	10	4.5	—	6.0	BEC*
BCW60D	AD	32[3]	32	5.0	20	32	380	630	2.0	5.0	0.35	10	125	10	4.5	—	6.0	BEC*
BCW65A	EA	60[3]	32	5.0	20	32	100	250	100	1.0	—	—	100	20	12	—	10	BEC*
BCW65B	EB	60[3]	32	5.0	20	32	160	400	100	1.0	—	—	100	20	12	—	10	BEC*
BCW66F	EF	75[3]	45	5.0	20	45	100	250	100	1.0	—	—	100	20	12	—	10	BEC*
BCW66G	EG	75[3]	45	5.0	20	45	160	400	100	1.0	—	—	100	20	12	—	10	BEC*
BCW71	K1	50	45	5.0	100	20	110	220	2.0	5.0	0.25	10	—	—	4.0	—	10	BEC*
BCW72	K2	50	45	5.0	100	20	200	450	2.0	5.0	0.25	10	—	—	4.0	—	10	BEC*
BCX19	U1	50[3]	45	5.0	100	20	100	600	100	1.0	0.62	500	—	—	5.0	—	—	BEC*
BCX20	U2	30[3]	25	5.0	100	20	100	600	100	1.0	0.62	500	—	—	5.0	—	—	BEC*
BCX70G	AG	45[3]	45	5.0	20	45	120	220	2.0	5.0	0.35	10	125	10	4.5	—	6.0	BEC*
BCX70H	AH	45[3]	45	5.0	20	45	180	310	2.0	5.0	0.35	10	125	10	4.5	—	6.0	BEC*
BCX70J	AJ	45[3]	45	5.0	20	45	250	460	2.0	5.0	0.35	10	125	10	4.5	—	6.0	BEC*
BCX70K	AK	45[3]	45	5.0	20	45	380	630	2.0	5.0	0.35	10	125	10	4.5	—	6.0	BEC*
TMPT918	3B	30	15	3.0	10	15	20	—	3.0	1.0	0.4	10	600	4.0	1.7	—	—	BEC*
TMPT2221	N12	60	30	5.0	10	50	40	120	150	10	0.4	150	250	20	8.0	—	—	BEC*
TMPT2221A	N54	75	40	6.0	10	60	40	120	150	10	0.3	150	250	20	8.0	225	—	BEC*
TMPT2222	1B	60	30	5.0	10	50	100	300	150	10	0.4	150	250	20	8.0	—	—	BEC*
TMPT2222A	1P	75	40	6.0	10	60	100	300	150	10	0.3	150	250	20	8.0	225	—	BEC*

NOTES: * Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

Continued next page...

1) Maximum at typical JEDEC conditions.
2) µA.
3) $V_{(BR)CES}/I_{CES}$, as applicable.
4) mA.
5) $V_{(BR)CER}$ at R = 10Ω.

NPN TRANSISTORS
SOT-23/TO-236AB

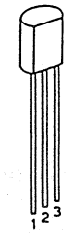
ELECTRICAL CHARACTERISTICS continued

Device Type	Marking	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	@ V_{CB} (V)	DC Current Gain h_{FE} Min.	h_{FE} Max.	@ I_C (mA)	@ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	@ I_C (mA)	f_T Min. (MHz)	@ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
TMPT3904	1A	60	40	6.0	50	30	100	300	10	1.0	0.2	10	300	10	4.0	200	5.0	BEC*
TMPT4401	2X	60	40	6.0	100	30	100	300	150	1.0	0.4	150	250	20	6.5	225	—	BEC*
TMPT5088	1Q	35	30	—	50	20	300	900	0.1	5.0	0.5	10	—	—	4.0	—	3.0	BEC*
TMPT5089	1R	30	25	—	50	15	400	1200	0.1	5.0	0.5	10	—	—	4.0	—	2.0	BEC*
TMPT6427	1V	40	40	12	50	30	10k	100k	10	5.0	1.2	50	130	10	7	—	10	BEC*
TMPTA05	1H	60	60	4.0	100	60	50	—	100	1.0	0.25	100	100	10	—	—	—	BEC*
TMPTA06	1G	80	80	4.0	100	80	50	—	100	1.0	0.25	100	100	10	—	—	—	BEC*
TMPTA14	1N	30[3]	—	10	100	30	20k	—	100	5.0	1.5	100	125	10	—	—	—	BEC*
TMPTA42	1D	300	300	6.0	100	200	40	—	30	10	0.5	20	50	10	3.0	—	—	BEC*
TMPTA43	1E	200	200	6.0	100	160	40	—	30	10	0.5	20	50	10	4.0	—	—	BEC*

NOTES: * Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

1) Maximum at typical JEDEC conditions.
2) µA.
3) $V_{(BR)CES}/I_{CES}$, as applicable.
4) mA.
5) $V_{(BR)CER}$ at R = 10Ω.

PNP TRANSISTORS



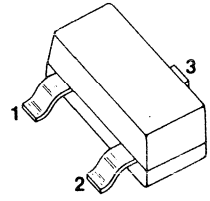
TO-92/TO-226AA

'2N' and 'TP' DEVICE TYPES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_C Max. (mA)	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	h_{FE} Max.	@ I_C (mA)	@ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
TP2907	500	60	40	5.0	20	50	100	300	150	10	0.4	150	200	50	8.0	100	—	EBC
TP2907A	500	60	60	5.0	10	50	100	300	150	10	0.4	150	200	50	8.0	100	—	EBC
2N3906	200	40	40	5.0	—	—	100	300	10	1.0	0.25	10	250	10	4.5	225	4.0	EBC
2N4402	500	40	40	5.0	—	—	50	150	150	2.0	0.4	150	150	20	10	225	—	EBC
2N4403	500	40	40	5.0	—	—	100	300	150	2.0	0.4	150	200	20	10	225	—	EBC
TP4413	500	40	30	5.0	10	30	120	—	1.0	5.0	0.2	1.0	20	—	8.0	—	—	EBC
TP4415	500	40	20	5.0	10	30	100	—	1.0	5.0	0.2	1.0	20	—	8.0	—	—	EBC
2N5086	100	50	50	—	50	35	150	500	0.1	5.0	0.3	10	40	0.5	4.0	—	3.0	EBC
2N5087	100	50	50	—	50	35	250	800	0.1	5.0	0.3	10	40	0.5	4.0	—	2.0	EBC
2N5400	300	130	120	5.0	50	100	40	180	10	5.0	0.2	10	100	10	6.0	—	8.0	EBC
2N5401	300	160	150	5.0	50	120	60	240	10	5.0	0.2	10	100	10	6.0	—	8.0	EBC
MPSA55	800	60	60	4.0	100	60	50	—	100	1.0	0.25	100	50	100	—	—	—	EBC
MPSA56	800	80	80	4.0	100	80	50	—	100	1.0	0.25	100	50	100	—	—	—	EBC
MPSA70	100	—	40	4.0	100	30	40	100	5.0	10	0.25	10	125	5.0	4.0	—	—	EBC

NOTES: 1) Maximum at typical JEDEC conditions.
2) µA.
3) $V_{(BR)CES}/I_{CES}$, as applicable.
4) mA.
5) $V_{(BR)CER}$ at R = 10Ω.

PNP TRANSISTORS



SOT-23/TO-236AB

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Marking	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain h_{FE} Max.	DC Current Gain @ I_C (mA)	DC Current Gain @ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
BCW29	C1	30[3]	32	5.0	100	20	120	260	2.0	5.0	0.3	10	—	—	7.0	—	10	BEC*
BCW30	C2	30[3]	32	5.0	100	20	215	500	2.0	5.0	0.3	10	—	—	7.0	—	10	BEC*
BCW61A	BA	32[3]	32	5.0	20	32	120	220	2.0	5.0	0.25	10	—	—	6.0	800	6.0	BEC*
BCW61B	BB	32[3]	32	5.0	20	32	180	310	2.0	5.0	0.25	10	—	—	6.0	800	6.0	BEC*
BCW61C	BC	32[3]	32	5.0	20	32	250	460	2.0	5.0	0.25	10	—	—	6.0	800	6.0	BEC*
BCW61D	BD	32[3]	32	5.0	20	32	380	630	2.0	5.0	0.25	10	—	—	6.0	800	6.0	BEC*
BCW67A	DA	45[3]	32	5.0	20	32	100	250	100	1.0	0.7	500	100	20	18	—	10	BEC*
BCW67B	DB	45[3]	32	5.0	20	32	160	400	100	1.0	0.7	500	100	20	18	—	10	BEC*
BCW68F	DF	60[3]	45	5.0	20	45	100	250	100	1.0	0.7	500	100	20	18	—	10	BEC*
BCW68G	DG	60[3]	45	5.0	20	45	160	400	100	1.0	0.7	500	100	20	18	—	10	BEC*
BCW69	H1	50[3]	45	5.0	100	20	120	260	2.0	5.0	0.3	10	—	—	7.0	—	10	BEC*
BCW70	H2	50[3]	45	5.0	100	20	215	500	2.0	5.0	0.3	10	—	—	7.0	—	10	BEC*
BCX17	T1	50[3]	45	5.0	100	20	100	600	100	1.0	0.62	500	—	—	8.0	—	—	BEC*
BCX18	T2	30[3]	25	5.0	100	20	100	600	100	1.0	0.62	500	—	—	8.0	—	—	BEC*
BCX71G	BG	453	45	5.0	20	45	120	220	2.0	5.0	0.25	10	—	—	6.0	—	—	BEC*
BCX71H	BH	45[3]	45	5.0	20	45	180	310	2.0	5.0	0.25	10	—	—	6.0	—	—	BEC*
BCX71J	BJ	45[3]	45	5.0	20	45	250	460	2.0	5.0	0.25	10	—	—	6.0	—	—	BEC*
BCX71K	BK	45[3]	45	5.0	20	45	380	630	2.0	5.0	0.25	10	—	—	6.0	—	—	BEC*
TMPT2907	2B	60	40	5.0	20	50	100	300	150	10	0.4	150	200	50	8.0	100	—	BEC*
TMPT2907A	2F	60	60	5.0	10	50	100	300	150	10	0.4	150	200	50	8.0	100	—	BEC*
TMPT3906	2A	40	40	5.0	—	—	100	300	10	1.0	0.25	10	250	10	4.5	225	4.0	BEC*
TMPT4402	2W	40	40	5.0	—	—	50	150	150	2.0	0.4	150	150	20	10	225	—	BEC*
TMPT4403	2T	40	40	5.0	—	—	100	300	150	2.0	0.4	150	200	20	10	225	—	BEC*
TMPT5086	2P	50	50	—	50	35	150	500	0.1	5.0	0.3	10	40	0.5	4.0	—	3.0	BEC*
TMPT5087	2Q	50	50	—	50	35	250	800	0.1	5.0	0.3	10	40	0.5	4.0	—	2.0	BEC*
TMPT5401	2L	160	150	5.0	50	120	60	240	10	5.0	0.2	10	100	10	6.0	—	8.0	BEC*
TMPTA55	2H	60	60	4.0	100	60	50	—	100	1.0	0.25	100	50	100	—	—	—	BEC*
TMPTA56	2G	80	80	4.0	100	80	50	—	100	1.0	0.25	100	50	100	—	—	—	BEC*
TMPTA70	2C	—	40	4.0	100	30	40	100	5.0	10	0.25	10	125	5.0	4.0	—	—	BEC*

NOTES: * Reversed pinning (E-B-C) available on special order—add suffix letter 'R' to part number.

1) Maximum at typical JEDEC conditions.
2) µA.
3) $V_{(BR)CES}/I_{CES}$, as applicable.
4)mA.
5)$V_{(BR)CER}$ at R = 10Ω.

N-CHANNEL JFETs

TO-92/TO-226AA

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	$V_{(BR)GSS}$		I_{GSS}		$V_{GS(off)}$ Limits		$V_{GS(off)}$ Conditions		I_{DSS}			g_{fs}			C_{ISS}[1]		C_{RSS}[1]		r_{DS}	Pin-ning
	Min. (V)	@I_G (μA)	Max. (nA)	@ V_{DS} (V)	Min. (V)	Max. (V)	V_{DS} (V)	I_D (nA)	Min. (mA)	Max. (mA)	@ V_{DS} (V)	Min. (mS)	Max. (mS)	@ V_{DS} (V)	Max. (pF)	@ V_{DS} (V)	Max. (pF)	@ V_{DS} (V)	Max. (Ω)	1, 2, 3
2N3819	-25	-1.0	-2.0	-15	—	-8.0	15	2.0	2.0	20	15	2.0	6.5	15	8.0	15	4.0	15	—	DGS†
TP3821	-50	-1.0	-1.0	-30	—	-4.0	10	1.0	0.5	2.5	15	1.5	4.5	15	6.0	15	2.0	15	—	DSG‡
TP3822	-50	-1.0	-1.0	-30	—	-6.0	10	1.0	2.0	10	15	3.0	6.5	15	6.0	15	2.0	15	—	DSG‡
TP3823	-30	-1.0	-1.0	-20	—	-8.0	10	1.0	4.0	20	15	3.5	6.5	15	6.0	15	2.0	15	—	DSG‡
TP3824	-50	-1.0	-1.0	-30	—	-8.0	15	0.5	4.0	20	15	3.5	6.5	15	6.0	15	2.0	15	250	DSG‡
TP4091	-40	-1.0	-1.0	-20	-5.0	-10	20	1.0	30	—	20	—	—	—	16	20	5.0	-20[3]	30	DSG‡
TP4092	-40	-1.0	-1.0	-20	-2.0	-7.0	20	1.0	15	—	20	—	—	—	16	20	5.0	-20[3]	50	DSG‡
TP4093	-40	-1.0	-1.0	-20	-1.0	-5.0	20	1.0	8.0	—	20	—	—	—	16	20	5.0	-20[3]	80	DSG‡
TP4117	-40	-1.0	-0.01	-20	-0.6	-1.8	10	1.0	0.03	0.09	10	0.07	0.21	10	3.0	10	1.5	10	—	DSG‡
TP4118	-40	-1.0	-0.01	-20	-1.0	-3.0	10	1.0	0.08	0.24	10	0.08	0.25	10	3.0	10	1.5	10	—	DSG‡
TP4119	-40	-1.0	-0.01	-20	-2.0	-6.0	10	1.0	0.2	0.6	10	0.10	0.33	10	3.0	10	1.5	10	—	DSG‡
TP4220	-30	-1.0	-10	-15	—	-4.0	15	1.0	0.5	3.0	15	1.0	4.0	15	6.0	15	2.0	15	—	DSG‡
TP4221	-30	-1.0	-10	-15	—	-6.0	15	1.0	2.0	6.0	15	2.0	5.0	15	6.0	15	2.0	15	—	DSG‡
TP4222	-30	-1.0	-10	-15	—	-8.0	15	1.0	5.0	15	15	2.5	6.0	15	6.0	15	2.0	15	—	DSG‡
TP4223	-30	-1.0	-10	-20	—	-8.0	15	1.0	3.0	18	15	3.0	7.0	15	6.0	15	2.0	15	—	DSG‡
TP4224	-30	-1.0	-10	-20	—	-8.0	15	1.0	2.0	20	15	2.0	7.5	15	6.0	15	2.0	15	—	DSG‡
TP4391	-40	-1.0	-1.0	-20	-4.0	-10	20	1.0	50	150	20	—	—	—	16	20	5.0	-12[3]	30	DSG‡
TP4392	-40	-1.0	-1.0	-20	-2.0	-5.0	20	1.0	25	100	20	—	—	—	16	20	5.0	-7.0[3]	60	DSG‡
TP4393	-40	-1.0	-1.0	-20	-0.5	-3.0	20	1.0	5.0	30	20	—	—	—	16	20	5.0	-5.0[3]	100	DSG‡
TP4416	-30	-1.0	-1.0	-20	—	-6.0	15	1.0	5.0	15	15	4.5	7.5	15	4.5	15	1.2	15	—	DSG‡
TP4416A	-35	-1.0	-1.0	-20	-2.5	-6.0	15	1.0	5.0	15	15	4.5	7.5	15	4.5	15	1.2	15	—	DSG‡
TP4856	-40	-1.0	-1.0	-20	-4.0	-10	15	1.0	50	—	15	—	—	—	18	-10[3]	8.0	-10[3]	25	DSG‡
TP4857	-40	-1.0	-1.0	-20	-2.0	-6.0	15	1.0	20	100	15	—	—	—	18	-10[3]	8.0	-10[3]	40	DSG‡
TP4858	-40	-1.0	-1.0	-20	-0.8	-4.0	15	1.0	8.0	80	15	—	—	—	18	-10[3]	8.0	-10[3]	60	DSG‡
TP4859	-30	-1.0	-1.0	-15	-4.0	-10	15	1.0	50	—	15	—	—	—	18	-10[3]	8.0	-10[3]	25	DSG‡
TP4860	-30	-1.0	-1.0	-15	-2.0	-6.0	15	1.0	20	100	15	—	—	—	18	-10[3]	8.0	-10[3]	40	DSG‡
TP4861	-30	-1.0	-1.0	-15	-0.8	-4.0	15	1.0	8.0	80	15	—	—	—	18	-10[3]	8.0	-10[3]	60	DSG‡
TP5163	-25	-1.0	-10	-15	-0.4	-8.0	15	-1.0[2]	1.0	40	15	2.0	9.0	15	12	15	3.0	15	—	DSG‡
TP5245	-30	-1.0	-1.0	-20	-1.0	-6.0	15	10	5.0	15	15	4.0	—	15	4.5	15	1.5	15	—	DSG‡
TP5246	-30	-1.0	-1.0	-20	-0.5	-4.0	15	10	1.5	7.0	15	2.5	—	15	4.5	15	1.5	15	—	DSG‡
TP5247	-30	-1.0	-1.0	-20	-1.5	-8.0	15	10	8.0	24	15	4.0	—	15	4.5	15	1.5	15	—	DSG‡
TP5248	-30	-1.0	-5.0	-20	-1.0	-8.0	15	10	4.0	20	15	3.0	—	15	6.0	15	2.0	15	—	DSG‡
TP5358	-40	-1.0	-1.0	-20	-0.5	-3.0	15	100	0.5	1.0	15	1.0	3.0	15	6.0	15	2.0	15	—	DSG‡
TP5359	-40	-1.0	-1.0	-20	-0.8	-4.0	15	100	0.6	1.6	15	1.2	3.6	15	6.0	15	2.0	15	—	DSG‡
TP5360	-40	-1.0	-1.0	-20	-0.8	-4.0	15	100	1.5	3.0	15	1.4	4.2	15	6.0	15	2.0	15	—	DSG‡
TP5361	-40	-1.0	-1.0	-20	-1.0	-6.0	15	100	2.5	5.0	15	1.5	4.5	15	6.0	15	2.0	15	—	DSG‡
TP5362	-40	-1.0	-1.0	-20	-2.0	-7.0	15	100	4.0	8.0	15	2.0	5.5	15	6.0	15	2.0	15	—	DSG‡
TP5363	-40	-1.0	-1.0	-20	-2.5	-8.0	15	100	7.0	14	15	2.5	6.0	15	6.0	15	2.0	15	—	DSG‡
TP5364	-40	-1.0	-1.0	-20	-2.5	-8.0	15	100	9.0	18	15	2.7	6.5	15	6.0	15	2.0	15	—	DSG‡
2N5457	-25	-10	-1.0	-15	-0.5	-6.0	15	10	1.0	5.0	15	1.0	5.0	15	7.0	15	3.0	15	—	DSG‡

NOTES: † Reversed pinning (S-G-D) available on special order—add suffix letter 'R' to part number.

Continued next page...

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

1) V_{GS} = 0 V.
2) I_D in μA.
3) V_{DS} = 0 V, V_{GS} in volts.
4) I_D = 10 mA.
5) I_D = 5.0 mA.
6) I_D = 1.0 mA.
7) I_D = 500 μA.
8) I_D = 200 μA.

N-CHANNEL JFETs
TO-92/TO-226AA

ELECTRICAL CHARACTERISTICS continued

Device Type	$V_{(BR)GSS}$		I_{GSS}		$V_{GS(off)}$ Limits		$V_{GS(off)}$ Conditions		I_{DSS}			g_{fs}			C_{iss}[1]		C_{rss}[1]		r_{DS}	Pin-ning
	Min.	@I_G	Max.	@ V_{DS}	Min.	Max.	V_{DS}	I_D	Min.	Max.	@ V_{DS}	Min.	Max.	@ V_{DS}	Max.	@ V_{DS}	Max.	@ V_{DS}	Max.	1, 2, 3
	(V)	(μA)	(nA)	(V)	(V)	(V)	(V)	(nA)	(mA)	(mA)	(V)	(mS)	(mS)	(V)	(pF)	(V)	(pF)	(V)	(Ω)	
2N5458	-25	-10	-1.0	-15	-1.0	-7.0	15	10	2.0	9.0	15	1.5	5.5	15	7.0	15	3.0	15	—	DSG‡
2N5459	-25	-10	-1.0	-15	-2.0	-8.0	15	10	4.0	16	15	2.0	6.0	15	7.0	15	3.0	15	—	DSG‡
2N5484	-25	-1.0	-1.0	-20	-0.3	-3.0	15	10	1.0	5.0	15	3.0	6.0	15	5.0	15	1.2	15	—	DSG‡
2N5485	-25	-1.0	-1.0	-20	-0.5	-4.0	15	10	4.0	10	15	3.5	7.0	15	5.0	15	1.2	15	—	DSG‡
2N5486	-25	-1.0	-1.0	-20	-2.0	-6.0	15	10	8.0	20	15	4.0	8.0	15	5.0	15	1.2	15	—	DSG‡
2N5638	-30	-1.0	-10	-15	—	-12	15	1.0	50	—	20	—	—	—	10	-12[3]	4.0	-12[3]	30	DSG‡
2N5639	-30	-1.0	-10	-15	—	-8.0	15	1.0	25	—	20	—	—	—	10	-12[3]	4.0	-12[3]	60	DSG‡
2N5640	-30	-1.0	-10	-15	—	-6.0	15	1.0	5.0	—	20	—	—	—	10	-12[3]	4.0	-12[3]	100	DSG‡
2N5653	-30	-1.0	-10	-15	—	-12	15	1.0	40	—	20	—	—	—	10	-12[3]	3.5	-12[3]	50	DSG‡
2N5654	-25	-1.0	-10	-15	—	-8.0	15	1.0	15	—	20	—	—	—	10	-8.0[3]	3.5	-8.0[3]	100	DSG‡
TP5668	-25	-10	-1.0	-15	-0.2	-4.0	15	10	1.0	5.0	15	1.0	—	15	7.0	15	3.0	15	—	DSG‡
TP5669	-25	-10	-1.0	-15	-1.0	-6.0	15	10	4.0	10	15	1.6	—	15	7.0	15	3.0	15	—	DSG‡
TP5670	-25	-10	-1.0	-15	-2.0	-8.0	15	10	8.0	20	15	2.0	—	15	7.0	15	3.0	15	—	DSG‡
TP5949	-30	-1.0	-1.0	-15	-3.0	-7.0	15	100	12	18	15	3.0	—	15	6.0	15	2.0	15	—	DSG‡
TPS950	-30	-1.0	-1.0	-15	-2.5	-6.0	15	100	10	15	15	3.0	—	15	6.0	15	2.0	15	—	DSG‡
TP5951	-30	-1.0	-1.0	-15	-2.0	-5.0	15	100	7.0	13	15	3.0	—	15	6.0	15	2.0	15	—	DSG‡
TP5952	-30	-1.0	-1.0	-15	-1.3	-3.5	-15	100	4.0	8.0	15	1.0	—	15	6.0	15	2.0	15	—	DSG‡
TP5953	-30	-1.0	-1.0	-15	-0.8	-3.0	15	100	2.5	5.0	15	1.0	—	15	6.0	15	2.0	15	—	DSG‡
BF244A	-30	-1.0	-5	-20	-0.5	-8.0	15	10	2.0	6.5	15	3.0	6.5	15	—	—	—	—	—	DGS†
BF244B	-30	-1.0	-5	-20	-0.5	-8.0	15	10	6.0	15	15	3.0	6.5	15	—	—	—	—	—	DGS†
BF244C	-30	-1.0	-5	-20	-0.5	-8.0	15	10	12	25	15	3.0	6.5	15	—	—	—	—	—	DGS†
BF246A	-25	-1.0	-5	-15	-0.6	-14.5	15	10	30	80	15	—	—	—	—	—	—	—	65	DGS†
BF246B	-25	-1.0	-5	-15	-0.6	-14.5	15	10	60	140	15	—	—	—	—	—	—	—	50	DGS†
BF246C	-25	-1.0	-5	-15	-0.6	-14.5	15	10	110	250	15	—	—	—	—	—	—	—	35	DGS†
BF256A	-30	-1.0	-5	-20	-0.5	-7.5	15	10	3.0	7.0	15	4.5	—	15	4.5	15	1.2	15	—	DGS†
BF256B	-30	-1.0	-5	-20	-0.5	-7.5	15	10	6.0	13	15	4.5	—	15	4.5	15	1.2	15	—	DGS†
BF256C	-30	-1.0	-5	-20	-0.5	-7.5	15	10	11	18	15	4.5	—	15	4.5	15	1.2	15	—	DGS†
BFR30	-25	-1.0	-0.2	-10	—	-5.0	10	0.5	4.0	10	10	1.0	4.0	10^6	5.0	10^6	1.5	10^6	—	DSG‡
BFR31	-25	-1.0	-0.2	-10	—	-2.5	10	0.5	1.0	5.0	10	1.5	4.5	10^6	5.0	10^6	1.5	10^6	—	DSG‡
J111	-35	-1.0	-1.0	-15	-3.0	-10	5.0	1.0[2]	20	—	15	—	—	—	16	15	5	-10[3]	30	DSG‡
J112	-35	-1.0	-1.0	-15	-1.0	-5.0	5.0	1.0[2]	5.0	—	15	—	—	—	16	15	5	-10[3]	50	DSG‡
J112A	-40	-1.0	-0.2	-15	-2.0	-7.0	5.0	1.0[2]	15	—	15	—	—	—	16	15	5	-10[3]	50	DSG‡
J113	-35	-1.0	-1.0	-15	—	-3.0	5.0	1.0[2]	2.0	—	15	—	—	—	16	15	5	-10[3]	100	DSG‡
J113A	-40	-1.0	-0.2	-15	-1.0	-5.0	5.0	1.0[2]	8.0	—	15	—	—	—	16	15	5	-10[3]	80	DSG‡
J201	-40	-1.0	-0.1	-20	-0.3	-1.5	20	10	0.2	1.0	20	0.5	—	20	4.0	20	1.0	20	—	DSG
J202	-40	-1.0	-0.1	-20	-0.8	-4.0	20	10	0.9	4.5	20	1.0	—	20	4.0	20	1.0	20	—	DSG
J203	-40	-1.0	-0.1	-20	-2.0	-10	20	10	4.0	20	20	1.5	—	20	6.0	20	1.2	20	—	DSG
J230	-40	-1.0	-0.2	-30	-0.5	-3.0	20	1.0[2]	0.7	3.0	20	1.0	3.5	20	—	—	—	—	—	DSG
J231	-40	-1.0	-0.2	-30	-1.5	-5.0	20	1.0[2]	2.0	6.0	20	1.5	4.0	20	—	—	—	—	—	DSG
J232	-40	-1.0	-0.2	-30	-3.0	-6.0	20	1.0[2]	5.0	10	20	2.5	5.0	20	—	—	—	—	—	DSG
J304	-30	-1.0	-0.1	-20	-2.0	-6.0	15	1.0	5.0	15	15	4.5	7.5	15	—	—	—	—	—	DSG

NOTES: † Reversed pinning (S-G-D) available on special order—add suffix letter 'R' to part number.

Continued next page...

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

§ Reversed pinning (G-S-D) available on special order—add suffix letter 'R' to part number.

1) V_{GS} = 0 V.
2) I_D in μA.
3) V_{DS} = 0 V, V_{GS} in volts.
4) I_D = 10 mA.
5) I_D = 5.0 mA.
6) I_D = 1.0 mA.
7) I_D = 500 μA.
8) I_D = 200 μA.

N-CHANNEL JFETs
TO-92/TO-226AA

ELECTRICAL CHARACTERISTICS continued

Device Type	$V_{(BR)GSS}$		I_{GSS}		$V_{GS(off)}$ Limits		$V_{GS(off)}$ Conditions		I_{DSS}			g_{fs}			C_{iss}[1]		C_{rss}[1]		r_{DS}	Pinning 1, 2, 3
	Min. (V)	@I_G (μA)	Max. (nA)	@ V_{DS} (V)	Min. (V)	Max. (V)	V_{DS} (V)	I_D (nA)	Min. (mA)	Max. (mA)	@V_{DS} (V)	Min. (mS)	Max. (mS)	@ V_{DS} (V)	Max. (pF)	@ V_{DS} (V)	Max. (pF)	@ V_{DS} (V)	Max. (Ω)	
J305	-30	-1.0	-0.1	-20	-0.5	-3.0	15	1.0	1.0	8.0	15	3.0	—	15	—	—	—	—	—	DSG‡
TPJ308	-25	-1.0	-1.0	-15	-1.0	-6.5	10	1.0	12	60	10	8.0	—	10^4	7.5	-10^3	3.5	-10^3	—	DSG‡
TPJ309	-25	-1.0	-1.0	-15	-1.0	-4.0	10	1.0	12	30	10	10	—	10^4	7.5	-10^3	7.5	-10^3	—	DSG‡
TPJ310	-25	-1.0	-1.0	-15	-2.0	-6.5	10	1.0	24	60	10	8.0	—	10^4	7.5	-10^3	7.5	-10^3	—	DSG‡
TPU308	-25	-1.0	-1.0	-15	-1.0	-6.0	10	1.0	12	60	10	—	—	—	7.5	-10^3	3.5	-10^3	—	DSG‡
TPU309	-25	-1.0	-1.0	-15	-1.0	-4.0	10	1.0	12	30	10	—	—	—	7.5	-10^3	3.5	-10^3	—	DSG‡
TPU310	-25	-1.0	-1.0	-15	-2.5	-6.0	10	1.0	24	60	10	—	—	—	7.5	-10^3	3.5	-10^3	—	DSG‡
TPU1897	-40	-1.0	-0.4	-20	-5.0	-10	20	1.0	30	—	20	—	—	—	16	20	3.5	20	30	DSG‡
TPU1898	-40	-1.0	-0.4	-20	-2.0	-7.0	20	1.0	15	—	20	—	—	—	16	20	3.5	20	50	DSG‡
TPU1899	-40	-1.0	-0.4	-20	-1.0	-5.0	20	1.0	8.0	—	20	—	—	—	16	20	3.5	20	80	DSG‡

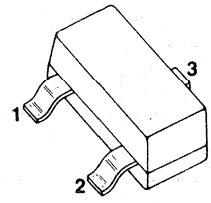
NOTES: † Reversed pinning (S-G-D) available on special order—add suffix letter 'R' to part number.

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

§ Reversed pinning (G-S-D) available on special order—add suffix letter 'R' to part number.

1) V_{GS} = 0 V.
2) I_D in μA.
3) V_{DS} = 0 V, V_{GS} in volts.
4) I_D = 10 mA.
5) I_D = 5.0 mA.
6) I_D = 1.0 mA.
7) I_D = 500 μA.
8) I_D = 200 μA.

N-CHANNEL JFETs



SOT-23/TO-236AB

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	$V_{(BR)GSS}$ Min. (V)	$V_{(BR)GSS}$ @I_G (µA)	I_{GSS} Max. (nA)	I_{GSS} @V_{DS} (V)	$V_{GS(off)}$ Limits Min. (V)	$V_{GS(off)}$ Limits Max. (V)	$V_{GS(off)}$ Conditions V_{DS} (V)	$V_{GS(off)}$ Conditions I_D (nA)	I_{DSS} Min. (mA)	I_{DSS} Max. (mA)	I_{DSS} @V_{DS} (V)	g_{fs} Min. (mS)	g_{fs} Max. (mS)	g_{fs} @V_{DS} (V)	C_{iss}[1] Max. (pF)	C_{iss}[1] @V_{DS} (V)	C_{rss}[1] Max. (pF)	C_{rss}[1] @V_{DS} (V)	r_{DS} Max. (Ω)	Pinning 1, 2, 3
TMPF3819	-25	-1.0	-2.0	-15	—	-8.0	15	2.0	2.0	20	15	2.0	6.5	15	8.0	15	4.0	15	—	DSG
TMPF3821	-50	-1.0	-1.0	-30	—	-4.0	10	1.0	0.5	2.5	15	1.5	4.5	15	6.0	15	2.0	15	—	DSG
TMPF3822	-50	-1.0	-1.0	-30	—	-6.0	10	1.0	2.0	10	15	3.0	6.5	15	6.0	15	2.0	15	—	DSG
TMPF3823	-30	-1.0	-1.0	-20	—	-8.0	10	1.0	4.0	20	15	3.5	6.5	15	6.0	15	2.0	15	—	DSG
TMPF3824	-50	-1.0	-1.0	-30	—	-8.0	15	0.5	4.0	20	15	3.5	6.5	15	6.0	15	2.0	15	250	DSG
TMPF4091	-40	-1.0	-1.0	-20	-5.0	-10	20	1.0	30	—	20	—	—	—	16	20	5.0	-20[3]	30	DSG
TMPF4092	-40	-1.0	-1.0	-20	-2.0	-7.0	20	1.0	15	—	20	—	—	—	16	20	5.0	-20[3]	50	DSG
TMPF4093	-40	-1.0	-1.0	-20	-1.0	-5.0	20	1.0	8.0	—	20	—	—	—	16	20	5.0	-20[3]	80	DSG
TMPF4117	-40	-1.0	-0.01	-20	-0.6	-1.8	10	1.0	0.03	0.09	10	0.07	0.21	10	3.0	10	1.5	10	—	DSG
TMPF4118	-40	-1.0	-0.01	-20	-1.0	-3.0	10	1.0	0.08	0.24	10	0.08	0.25	10	3.0	10	1.5	10	—	DSG
TMPF4119	-40	-1.0	-0.01	-20	-2.0	-6.0	10	1.0	0.2	0.6	10	0.10	0.33	10	3.0	10	1.5	10	—	DSG
TMPF4220	-30	-10	-1.0	-15	—	-4.0	15	1.0	0.5	3.0	15	1.0	4.0	15	6.0	15	2.0	15	—	DSG
TMPF4221	-30	-10	-1.0	-15	—	-6.0	15	1.0	2.0	6.0	15	2.0	5.0	15	6.0	15	2.0	15	—	DSG
TMPF4222	-30	-10	-1.0	-15	—	-8.0	15	1.0	5.0	15	15	2.5	6.0	15	6.0	15	2.0	15	—	DSG
TMPF4223	-30	-10	-1.0	-20	—	-8.0	15	1.0	3.0	18	15	3.0	7.0	15	6.0	15	2.0	15	—	DSG
TMPF4224	-30	-10	-1.0	-20	—	-8.0	15	1.0	2.0	20	15	2.0	7.5	15	6.0	15	2.0	15	—	DSG
TMPF4391	-40	-1.0	-1.0	-20	-4.0	-10	20	1.0	50	150	20	—	—	—	16	20	5.0	-12[3]	30	DSG
TMPF4392	-40	-1.0	-1.0	-20	-2.0	-5.0	20	1.0	25	100	20	—	—	—	16	20	5.0	-7.0[3]	60	DSG
TMPF4393	-40	-1.0	-1.0	-20	-0.5	-3.0	20	1.0	5.0	30	20	—	—	—	16	20	5.0	-5.0[3]	100	DSG
TMPF4416	-30	-1.0	-1.0	-20	—	-6.0	15	1.0	5.0	15	15	4.5	7.5	15	4.5	15	1.2	15	—	DSG
TMPF4416A	-35	-1.0	-1.0	-20	-2.5	-6.0	15	1.0	5.0	15	15	4.5	7.5	15	4.5	15	1.2	15	—	DSG
TMPF4856	-40	-1.0	-1.0	-20	-4.0	-10	15	1.0	50	—	15	—	—	—	18	-10[3]	8.0	-10[3]	25	DSG
TMPF4857	-40	-1.0	-1.0	-20	-2.0	-6.0	15	1.0	20	100	15	—	—	—	18	-10[3]	8.0	-10[3]	40	DSG
TMPF4858	-40	-1.0	-1.0	-20	-0.8	-4.0	15	1.0	8.0	80	15	—	—	—	18	-10[3]	8.0	-10[3]	60	DSG
TMPF4859	-30	-1.0	-1.0	-15	-4.0	-10	15	1.0	50	—	15	—	—	—	18	-10[3]	8.0	-10[3]	25	DSG
TMPF4860	-30	-1.0	-1.0	-15	-2.0	-6.0	15	1.0	20	100	15	—	—	—	18	-10[3]	8.0	-10[3]	40	DSG
TMPF4861	-30	-1.0	-1.0	-15	-0.8	-4.0	15	1.0	8.0	80	15	—	—	—	18	-10[3]	8.0	-10[3]	60	DSG
TMPF5163	-25	-1.0	-10	-15	0.4	8.0	15	1.0[2]	1.0	40	15	2.0	9.0	15	12	15	3.0	15	—	DSG
TMPF5245	-30	-1.0	-1.0	-20	-1.0	-6.0	15	10	5.0	15	15	4.0	—	15	4.5	15	1.5	15	—	DSG
TMPF5246	-30	-1.0	-1.0	-20	-0.5	-4.0	15	10	1.5	7.0	15	2.5	—	15	4.5	15	1.5	15	—	DSG
TMPF5247	-30	-1.0	-1.0	-20	-1.5	-8.0	15	10	8.0	24	15	4.0	—	15	4.5	15	1.5	15	—	DSG
TMPF5248	-30	-1.0	-5.0	-20	-1.0	-8.0	15	10	4.0	20	15	3.0	—	15	6.0	15	2.0	15	—	DSG
TMPF5358	-40	-1.0	-1.0	-20	-0.5	-3.0	15	100	0.5	1.0	15	1.0	3.0	15	6.0	15	2.0	15	—	DSG
TMPF5359	-40	-1.0	-1.0	-20	-0.8	-4.0	15	100	0.6	1.6	15	1.2	3.6	15	6.0	15	2.0	15	—	DSG
TMPF5360	-40	-1.0	-1.0	-20	-0.8	-4.0	15	100	1.5	3.0	15	1.4	4.2	15	6.0	15	2.0	15	—	DSG

NOTES: 1) V_{GS} = 0 V.

Continued next page...

2) I_D in µA.

3) V_{DS} = 0 V, V_{GS} in volts.

4) I_D = 10 µA.

5) I_D = 5.0 µA.

6) I_D = 1.0 mA.

7) I_D = 500 µA.

8) I_D = 200 µA.

ELECTRICAL CHARACTERISTICS continued

Device Type	$V_{(BR)GSS}$ Min. (V)	$@I_G$ (μA)	I_{GSS} Max. (nA)	@ V_{DS} (V)	$V_{GS(off)}$ Limits Min. (V)	Limits Max. (V)	Conditions V_{DS} (V)	Conditions I_D (nA)	I_{DSS} Min. (mA)	I_{DSS} Max. (mA)	@ V_{DS} (V)	g_{fs} Min. (mS)	g_{fs} Max. (mS)	@ V_{DS} (V)	C_{iss}[1] Max. (pF)	@ V_{DS} (V)	C_{rss}[1] Max. (pF)	@ V_{DS} (V)	r_{DS} Max. (Ω)	Pin-ning 1, 2, 3
TMPF5361	-40	-1.0	-1.0	-20	-1.0	-6.0	15	100	2.5	5.0	15	1.5	4.5	15	6.0	15	2.0	15	—	DSG
TMPF5362	-40	-1.0	-1.0	-20	-2.0	-7.0	15	100	4.0	8.0	15	2.0	5.5	15	6.0	15	2.0	15	—	DSG
TMPF5363	-40	-1.0	-1.0	-20	-2.5	-8.0	15	100	7.0	14	15	2.5	6.0	15	6.0	15	2.0	15	—	DSG
TMPF5364	-40	-1.0	-1.0	-20	-2.5	-8.0	15	100	9.0	18	15	2.7	6.5	15	6.0	15	2.0	15	—	DSG
TMPF5457	-25	-10	-1.0	-15	-0.5	-6.0	15	10	1.0	5.0	15	1.0	5.0	15	7.0	15	3.0	15	—	DSG
TMPF5458	-25	-10	-1.0	-15	-1.0	-7.0	15	10	2.0	9.0	15	1.5	5.5	15	7.0	15	3.0	15	—	DSG
TMPF5459	-25	-10	-1.0	-15	-2.0	-8.0	15	10	4.0	16	15	2.0	6.0	15	7.0	15	3.0	15	—	DSG
TMPF5484	-25	-1.0	-1.0	-20	-0.3	-3.0	15	10	1.0	5.0	15	3.0	6.0	15	5.0	15	1.0	15	—	DSG
TMPF5485	-25	-1.0	-1.0	-20	-0.5	-4.0	15	10	4.0	10	15	3.5	7.0	15	5.0	15	1.0	15	—	DSG
TMPF5486	-25	-1.0	-1.0	-20	-2.0	-6.0	15	10	8.0	20	15	4.0	8.0	15	5.0	15	1.2	15	—	DSG
TMPF5638	-30	-10	-1.0	-15	—	-12	15	1.0	50	—	20	—	—	—	10	-12[3]	4.0	-12[3]	30	DSG
TMPF5639	-30	-10	-1.0	-15	—	-8.0	15	1.0	25	—	20	—	—	—	10	-12[3]	4.0	-12[3]	60	DSG
TMPF5640	-30	-10	-1.0	-15	—	-6.0	15	1.0	5.0	—	20	—	—	—	10	-12[3]	4.0	-12[3]	100	DSG
TMPF5653	-30	-10	-1.0	-15	—	-12	15	1.0	40	—	20	—	—	—	10	-12[3]	3.5	-12[3]	50	DSG
TMPF5654	-25	-10	-10	-15	—	-8.0	15	1.0	15	—	20	—	—	—	10	-8.0[3]	3.5	-8.0[3]	100	DSG
TMPF5668	-25	-10	-1.0	-15	-0.2	-4.0	15	10	1.0	5.0	15	1.0	—	15	7.0	15	3.0	15	—	DSG
TMPF5669	-25	-10	-1.0	-15	-1.0	-6.0	15	10	4.0	10	15	1.6	—	15	7.0	15	3.0	15	—	DSG
TMPF5670	-25	-10	-1.0	-15	-2.0	-8.0	15	10	8.0	20	15	2.0	—	15	7.0	15	3.0	15	—	DSG
TMPF5949	-30	-1.0	-1.0	-15	-3.0	-7.0	15	100	12	18	15	3.0	—	15	6.0	15	2.0	15	—	DSG
TMPF5950	-30	-1.0	-1.0	-15	-2.5	-6.0	15	100	10	15	15	3.0	—	15	6.0	15	2.0	15	—	DSG
TMPF5951	-30	-1.0	-1.0	-15	-2.0	-5.0	15	100	7.0	13	15	3.0	—	15	6.0	15	2.0	15	—	DSG
TMPF5952	-30	-1.0	-1.0	-15	-1.3	-3.5	15	100	4.0	8.0	15	1.0	—	15	6.0	15	2.0	15	—	DSG
TMPF5953	-30	-1.0	-1.0	-15	-0.8	-3.0	15	100	2.5	5.0	15	1.0	—	15	6.0	15	2.0	15	—	DSG
TMPFBC264A	-30	-1.0	-10	-20	-0.5	—	15	10	2.0	4.5	15	2.5	—	15	4.0	15	1.2	15	—	DSG
TMPFBC264B	-30	-1.0	-10	-20	-0.5	—	15	10	3.5	6.5	15	3.0	—	15	4.0	15	1.2	15	—	DSG
TMPFBC264C	-30	-1.0	-10	-20	-0.5	—	15	10	5.0	8.0	15	3.5	—	15	4.0	15	1.2	15	—	DSG
TMPFBC264D	-30	-1.0	-10	-20	-0.5	—	15	10	7.0	12	15	4.0	—	15	4.0	15	1.2	15	—	DSG
TMPFBF244A	-30	-1.0	-5.0	-20	-0.5	-8.0	15	10	2.0	6.5	15	3.0	6.5	15	—	—	—	—	—	DSG
TMPFBF244B	-30	-1.0	-5.0	-20	-0.5	-8.0	15	10	6.0	15	15	3.0	6.5	15	—	—	—	—	—	DSG
TMPFBF244C	-30	-1.0	-5.0	-20	-0.5	-8.0	15	10	12	25	15	3.0	6.5	15	—	—	—	—	—	DSG
TMPFBF246A	-25	-1.0	-5.0	-15	-0.6	-14.5	15	10	30	80	15	—	—	—	—	—	—	—	65	DSG
TMPFBF246B	-25	-1.0	-5.0	-15	-0.6	-14.5	15	10	60	140	15	—	—	—	—	—	—	—	50	DSG
TMPFBF246C	-25	-1.0	-5.0	-15	-0.6	-14.5	15	10	110	250	15	—	—	—	—	—	—	—	35	DSG
TMPFBF256A	-30	-1.0	-5.0	-20	-0.5	-7.5	15	10	3.0	7.0	15	4.5	—	15	4.5	15	1.2	15	—	DSG
TMPFBF256B	-30	-1.0	-5.0	-20	-0.5	-7.5	15	10	6.0	13	15	4.5	—	15	4.5	15	1.2	15	—	DSG
TMPFBF256C	-30	-1.0	-5.0	-20	-0.5	-7.5	15	10	11	18	15	4.5	—	15	4.5	15	1.2	15	--	DSG
TMPFJ111	-35	-1.0	-1.0	-15	-3.0	-10	5.0	1.0	20	—	15	—	—	—	16	15	5	-10[3]	30	DSG
TMPFJ112	-35	-1.0	-1.0	-15	-1.0	-5.0	5.0	1.0	5.0	—	15	—	—	—	16	15	5	-10[3]	50	DSG
TMPFJ112A	-40	-1.0	-0.2	-1.0	-2.0	-7.0	5.0	1.0	15	—	15	—	—	—	16	15	5	-10[3]	50	DSG
TMPFJ113	-35	-1.0	-1.0	-15	—	-3.0	5.0	1.0	2.0	—	15	—	—	—	16	15	5	-10[3]	100	DSG

NOTES: 1) V_{GS} = 0 V.

2) I_D in μA.

3) V_{DS} = 0 V, V_{GS} in volts.

4) I_D = 10 μA.

5) I_D = 5.0 μA.

6) I_D = 1.0 mA.

7) I_D = 500 μA.

8) I_D = 200 μA.

Continued next page...

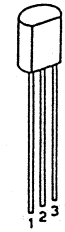
N-CHANNEL JFETs
SOT-23/TO-236AB

ELECTRICAL CHARACTERISTICS continued

Device Type	$V_{(BR)GSS}$ Min. (V)	$V_{(BR)GSS}$ @I_G (μA)	I_{GSS} Max. (nA)	I_{GSS} @ V_{DS} (V)	$V_{GS(off)}$ Limits Min. (V)	$V_{GS(off)}$ Limits Max. (V)	$V_{GS(off)}$ Conditions V_{DS} (V)	$V_{GS(off)}$ Conditions I_D (nA)	I_{DSS} Min. (mA)	I_{DSS} Max. (mA)	I_{DSS} @ V_{DS} (V)	g_{fs} Min. (mS)	g_{fs} Max. (mS)	g_{fs} @ V_{DS} (V)	C_{iss}[1] Max. (pF)	C_{iss}[1] @ V_{DS} (V)	C_{rss}[1] Max. (pF)	C_{rss}[1] @ V_{DS} (V)	r_{DS} Max. (Ω)	Pinning 1, 2, 3
TMPFJ113A	-40	-1.0	-0.2	-1.0	-1.0	-5.0	5.0	1.0	8.0	—	15	—	—	—	16	15	5	-10^3	80	DSG
TMPFJ201	-40	-1.0	-1.0	-20	-0.3	-1.5	20	10	0.2	1.0	20	0.5	—	20	4.0	20	1.0	20	—	DSG
TMPFJ202	-40	-1.0	-1.0	-20	-0.8	-4.0	20	10	0.9	4.5	20	1.0	—	20	4.0	20	1.0	20	—	DSG
TMPFJ203	-40	-1.0	-1.0	-20	-2.0	-10	20	10	4.0	20	20	1.5	—	20	6.0	20	1.2	20	—	DSG
TMPFJ230	-40	-1.0	-1.0	-30	-0.5	-3.0	20	1[2]	0.7	3.0	20	1.0	3.5	20	—	—	—	—	—	DSG
TMPFJ231	-40	-1.0	-1.0	-30	-1.5	-5.0	20	1[2]	2.0	6.0	20	1.5	4.0	20	—	—	—	—	—	DSG
TMPFJ232	-40	-1.0	-1.0	-30	-3.0	-6.0	20	1[2]	5.0	10	20	2.5	5.0	20	—	—	—	—	—	DSG
TMPFJ304	-30	-1.0	-1.0	20	-2.0	-6.0	15	1.0	5.0	15	15	4.5	7.5	15	—	—	—	—	—	DSG
TMPFJ305	-30	-1.0	-1.0	-20	-0.5	-3.0	15	1.0	1.0	8.0	15	3.0	—	15	—	—	—	—	—	DSG
TMPFJ308	-25	-1.0	-1.0	-15	-1.0	-6.5	10	1.0	12	60	10	8.0	—	10^4	7.5	-10^3	3.5	-10^3	—	DSG
TMPFJ309	-25	-1.0	-1.0	-15	-1.0	-4.0	10	1.0	12	30	10	10	—	10^4	7.5	-10^3	3.5	-10^3	—	DSG
TMPFJ310	-25	-1.0	-1.0	-15	-2.0	-6.5	10	1.0	24	60	10	8.0	—	10^4	7.5	-10^3	3.5	-10^3	—	DSG
TMPFU308	-25	-1.0	-1.0	-15	-1.0	-6.0	10	1.0	12	60	10	—	—	—	7.5	-10^3	3.5	-10^3	—	DSG
TMPFU309	-25	-1.0	-1.0	-15	-1.0	-4.0	10	1.0	12	30	10	—	—	—	7.5	-10^3	3.5	-10^3	—	DSG
TMPFU310	-25	-1.0	-1.0	-15	-2.5	-6.0	10	1.0	24	60	10	—	—	—	7.5	-10^3	3.5	-10^3	—	DSG
TMPFU1897	-40	-1.0	-1.0	-20	-5.0	-10	20	1.0	30	—	20	—	—	—	16	20	3.5	20	30	DSG
TMPFU1898	-40	-1.0	-1.0	-20	-2.0	-7.0	20	1.0	15	—	20	—	—	—	16	20	3.5	20	50	DSG
TMPFU1899	-40	-1.0	-1.0	-20	-1.0	-5.0	20	1.0	8.0	—	20	—	—	—	16	20	3.5	20	80	DSG

NOTES: 1) V_{GS} = 0 V.
2) I_D in μA.
3) V_{DS} = 0 V, V_{GS} in volts.
4) I_D = 10 μA
5) I_D = 5.0 μA
6) I_D = 1.0 mA
7) I_D = 500 μA
8) I_D = 200 μA

P-CHANNEL JFETs



TO-92/TO-226AA

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	$V_{(BR)GSS}$		I_{GSS}		$V_{GS(off)}$ Limits		$V_{GS(off)}$ Conditions		I_{DSS}			g_{fs}			C_{iss}[1]		C_{rss}[1]		r_{DS}	Pin-ning
	Min. (V)	@I_G (μA)	Max. (nA)	@ V_{DS} (V)	Min. (V)	Max. (V)	V_{DS} (V)	I_D (nA)	Min. (mA)	Max. (mA)	@ V_{DS} (V)	Min. (mS)	Max. (mS)	@ V_{DS} (V)	Max. (pF)	@ V_{DS} (V)	Max. (pF)	@ V_{DS} (V)	Max. (Ω)	1, 2, 3
2N3820	20	10	20	10	—	8.0	-10	-10^2	-0.3	-15	-10	0.8	5.0	-10	32	-10	16	-10	—	DGS†
TP3993	25	1.0	1.0	15	4.0	9.5	-10	-1^2	-10	—	-10	6.0	12	-10	16	-10	5.5	10^3	150	DSG‡
TP3994	25	1.0	1.0	15	1.0	5.5	-10	-1^2	-2.0	—	-10	4.0	10	-10	16	-10	5.5	10^3	300	DSG‡
TP4381	25	1.0	1.0	15	1.0	5.0	-15	-1.0^2	-3.0	-12	-15	2.0	6.0	-15	20	-15	5.0	-15	—	DSG‡
2N5460	40	10	5.0	20	0.75	6.0	-15	-1.0	-1.0	-5.0	-15	1.0	5.0	-15	7.0	-15	3.0	-15	—	DSG‡
2N5461	40	10	5.0	20	1.0	7.5	-15	-1.0	-2.0	-9.0	-15	1.5	5.5	-15	7.0	-15	3.0	-15	—	DSG‡
2N5462	40	10	5.0	20	1.8	9.0	-15	-1.0	-4.0	-16	-15	2.0	6.0	-15	7.0	-15	3.0	-15	—	DSG‡
J174	30	1.0	1.0	20	5.0	10	-15	-10	-20	-135	-15	—	—	—	—	—	—	—	85	DSG†
J175	30	1.0	1.0	20	3.0	6.0	-15	-10	-7.0	-70	-15	—	—	—	—	—	—	—	125	DSG†
J176	30	1.0	1.0	20	1.0	4.0	-15	-10	-2.0	-35	-15	—	—	—	—	—	—	—	250	DSG†
J177	30	1.0	1.0	20	0.8	2.25	-15	-10	-1.5	-20	-15	—	—	—	—	—	—	—	300	DSG†
TPU304	30	1.0	1.0	20	5.0	10	-15	-1^2	-30	-90	-15	—	—	—	27	-15	7.0	12^3	85	DSG‡
TPU305	30	1.0	1.0	20	3.0	6.0	-15	-1^2	-15	-60	-15	—	—	—	27	-15	7.0	7.0^3	110	DSG‡
TPU306	30	1.0	1.0	20	1.0	4.0	-15	-1^2	-5.0	-25	-15	—	—	—	27	-15	7	5.0^3	175	DSG‡

NOTES: † Reversed pinning (S-G-D) available on special order—add suffix letter 'R' to part number.

‡ Reversed pinning (S-D-G) available on special order—add suffix letter 'R' to part number.

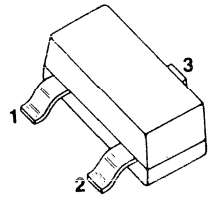
1) V_{GS} = 0 V.

2) I_D in μA.

3) V_{DS} = 0 V, V_{GS} in volts.

4) V_{GS} = 1.0 V.

P-CHANNEL JFETS



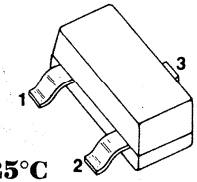
SOT-23/TO-236AB

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	$V_{(BR)GSS}$		I_{GSS}		$V_{GS(off)}$				I_{DSS}			g_{fs}			C_{iss}[1]		C_{rss}[1]		r_{DS}	Pin-ning
					Limits		Conditions													
	Min.	@I_G	Max.	@ V_{DS}	Min.	Max.	V_{DS}	I_D	Min.	Max.	@ V_{DS}	Min.	Max.	@ V_{DS}	Max.	@ V_{DS}	Max.	@ V_{DS}	Max.	1, 2, 3
	(V)	(μA)	(nA)	(V)	(V)	(V)	(V)	(nA)	(mA)	(mA)	(V)	(mS)	(mS)	(V)	(pF)	(V)	(pF)	(V)	(Ω)	
TMPF3820	20	10	20	10	—	8.0	-10	-10[2]	-0.3	-15	-10	0.8	5.0	-10	32	-10	16	-10	—	DSG
TMPF3993	25	1.0	1.0	15	4.0	9.5	-10	-1.0[2]	-10	—	-10	6.0	12	-10	20	-10	4.5	10^3	150	DSG
TMPF3994	25	1.0	1.0	15	1.0	5.5	-10	-1.0[2]	-2.0	—	-10	4.0	10	-10	20	-10	4.5	10^3	300	DSG
TMPF4381	25	1.0	1.0	15	1.0	5.0	-15	-1.0[2]	-3.0	-12	-15	2.0	6.0	-15	20	-15	5.0	-15	—	DSG
TMPF5460	40	10	5.0	20	0.75	6.0	-15	-1.0	-1.0	-5.0	-15	1.0	5.0	-15	7.0	-15	3.0	-15	—	DSG
TMPF5461	40	10	5.0	20	1.0	7.5	-15	-1.0	-2.0	-9.0	-15	1.5	5.5	-15	7.0	-15	3.0	-15	—	DSG
TMPF5462	40	10	5.0	20	1.8	9.0	-15	-1.0	-4.0	-16	-15	2.0	6.0	-15	7.0	-15	3.0	-15	—	DSG
TMPFJ174	30	1.0	1.0	20	5.0	10	-15	-10	-20	-135	-15	—	—	—	—	—	—	—	85	DSG
TMPFJ175	30	1.0	1.0	20	3.0	6.0	-15	-10	-7.0	-70	-15	—	—	—	—	—	—	—	125	DSG
TMPFJ176	30	1.0	1.0	20	1.0	4.0	-15	-10	-2.0	-35	-15	—	—	—	—	—	—	—	250	DSG
TMPFJ177	30	1.0	1.0	20	0.8	2.25	-15	-10	-1.5	-20	-15	—	—	—	—	—	—	—	300	DSG
TMPFU304	30	1.0	1.0	20	5.0	10	-15	-1.0[2]	-30	-90	-15	—	—	—	27	-15	7.0	12^3	85	DSG
TMPFU305	30	1.0	1.0	20	3.0	6.0	-15	-1.0[2]	-15	-60	-15	—	—	—	27	-15	7.0	7.0^3	110	DSG
TMPFU306	30	1.0	1.0	20	1.0	4.0	-15	-1.0[2]	-5.0	-25	-15	—	—	—	27	-15	7.0	5.0^3	175	DSG

NOTES: 1) V_{GS} = 0 V.
2) I_D in μA.
3) V_{DS} = 0 V, V_{GS} in volts.
4) V_{GS} = 1.0 V.

DIODES



SOT-23/TO-236AB

'TMPD' GENERAL-PURPOSE DIODES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Description	Marking	I_F Max. (mA)	V_{BR} Min. (V)	V_F Max. (V)	V_F @I_F (mA)	I_R Max. (nA)	t_{rr} Max. (ns)	C_O Max. (pF)	Pinning 1, 2, 3
TMPD914	General-Purpose	5D	600	100	1.0	10	25	4.0	6.0	A NC K
TMPD4148	General-Purpose	5D	600	100	1.0	10	25	4.0	4.0	A NC K
TMPD4150	General-Purpose	ABA	600	75	0.62	1.0	100	4.0	2.5	A NC K

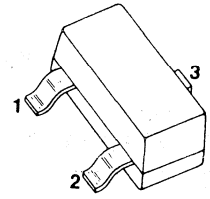
'TMPD' SCHOTTKY DIODES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	V_{BR} Min. (V)	V_F Max. I_F = 1 mA (V)	V_F Max. I_F = 10 mA (mA)	I_R Max. V_R = 1 V (nA)	I_R Max. V_R = 20 V (nA)	I_R Max. V_R = 50 V (nA)	C_O Max. (pF)	Pinning 1, 2, 3
TMPD5711	70	0.41	0.75	—	50	200	2.0	A NC K
TMPD6916	40	0.34	0.47	100	200	—	5.0	A NC K
TMPD6919	50	0.45	0.80	—	200	—	1.2	A NC K
TMPD6924	70	0.41	0.75	—	—	200	2.0	A NC K

PRO-ELECTRON DEVICE TYPES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Description	Marking	I_F Max. (mA)	V_{BR} Min. (V)	V_F Max. (V)	V_F @I_F (mA)	I_R Max. (nA)	t_{rr} Max. (ns)	C_O Max. (pF)	Pinning 1, 2, 3
BAR18	Schottky	D76	—	70	0.41	1.0	200	—	1.7	A NC K
BAS16	General-Purpose	A6	600	75	0.72	1.0	1000	6.0	2.0	A NC K
BAS19	General-Purpose	A8	200	100	1.25	200	100	50	5.0	A NC K
BAS21	General-Purpose	A82	200	200	1.0	100	100	50	5.0	A NC K
BAV70	Common Cathode	A4	100	70	0.86	10	5000	6.0	1.5	A1 A2 K
BAV74	Common Cathode	JA	70	50	1.0	100	100	4.0	2.0	A1 A2 K
BAV99	Dual In-Series	A7	70	70	1.1	50	2500	6.0	2.0	A1 K2 A/K
BAW56	Common Anode	A1	70	70	1.1	50	2500	6.0	2.0	K1 K2 A

ZENER DIODES



SOT-23/TO-236AB

'TMPZ' ZENER DIODES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Marking	Zener Voltage				Leakage Current		Zener Impedance		Pinning
		Min. (V)	Nom. (V)	Max. (V)	@I_{ZT} (mA)	Max (μA)	@V_R (V)	Max. Z_{ZT} (Ω)	@I_{ZT} (mA)	1, 2, 3
TMPZ5229	8D	4.08	4.3	4.52	20	5.0	1.0	22	20	A NC K
TMPZ5230	8E	4.47	4.7	4.94	20	5.0	2.0	19	20	A NC K
TMPZ5231	8F	4.85	5.1	5.36	20	5.0	2.0	17	20	A NC K
TMPZ5232	8G	5.32	5.6	5.88	20	5.0	3.0	11	20	A NC K
TMPZ5233	8H	5.70	6.0	6.30	20	5.0	3.5	7.0	20	A NC K
TMPZ5234	8J	5.98	6.2	6.51	20	3.0	4.0	7.0	20	A NC K
TMPZ5235	8K	6.46	6.8	7.14	20	3.0	5.0	5.0	20	A NC K
TMPZ5236	8L	7.13	7.5	7.88	20	3.0	6.0	6.0	20	A NC K
TMPZ5237	8M	7.79	8.2	8.61	20	3.0	6.5	8.0	20	A NC K
TMPZ5238	8N	8.26	8.7	9.14	20	3.0	6.5	8.0	20	A NC K
TMPZ5239	8P	8.65	9.1	9.56	20	3.0	7.0	10	20	A NC K
TMPZ5240	8Q	9.50	10	10.5	20	3.0	8.0	17	20	A NC K
TMPZ5241	8R	10.5	11	11.6	20	2.0	8.4	22	20	A NC K
TMPZ5242	8S	11.4	12	12.6	20	1.0	9.1	30	20	A NC K
TMPZ5243	8T	12.4	13	13.7	9.5	0.5	9.9	13	9.5	A NC K
TMPZ5244	8U	13.3	14	14.7	9.0	0.1	10.0	15	9.0	A NC K
TMPZ5245	8V	14.3	15	15.8	8.5	0.1	11.0	16	8.5	A NC K
TMPZ5246	8W	15.2	16	16.8	7.8	0.1	12.0	17	7.8	A NC K
TMPZ5247	8X	16.2	17	17.9	7.4	0.1	13.0	19	7.4	A NC K
TMPZ5248	8Y	17.1	18	18.9	7.0	0.1	14.0	21	7.0	A NC K
TMPZ5249	8Z	18.1	19	20.0	6.6	0.1	14.0	23	6.6	A NC K
TMPZ5250	81A	19.0	20	21.0	6.2	0.1	15.0	25	6.2	A NC K
TMPZ5251	81B	20.9	22	23.1	5.5	0.1	17.0	29	5.5	A NC K
TMPZ5252	81C	22.8	24	25.2	5.2	0.1	18.0	33	5.2	A NC K
TMPZ5253	81D	23.8	25	26.3	5.0	0.1	19.0	35	5.0	A NC K
TMPZ5254	81E	25.7	27	28.4	4.6	0.1	21.0	41	4.6	A NC K
TMPZ5455	81F	26.6	28	29.4	4.5	0.1	21.0	44	4.5	A NC K
TMPZ5256	81G	28.5	30	31.5	4.2	0.1	23.0	49	4.2	A NC K
TMPZ5257	81H	31.4	33	34.7	3.8	0.1	25.0	58	3.8	A NC K

ZENER DIODES
SOT-23/TO-236AB

'BZX84' ZENER DIODES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

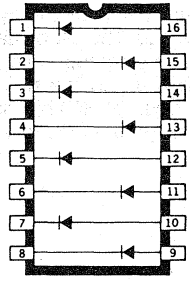
Device Type	Marking	Zener Voltage				Leakage Current		Zener Impedance		Pinning
		Min. (V)	Nom. (V)	Max. (V)	@I_{ZT} (mA)	Max (μA)	@V_R (V)	Max. Z_{ZT} (Ω)	@I_{ZT} (mA)	1, 2, 3
BZX84C4V7	Z1	4.4	4.7	5.0	5.0	3.0	2.0	80	5.0	A NC K
BZX84C5V1	Z2	4.8	5.1	5.4	5.0	2.0	2.0	60	5.0	A NC K
BZX84C5V6	Z3	5.2	5.6	6.0	5.0	1.0	2.0	40	5.0	A NC K
BZX84C6V2	Z4	5.8	6.2	6.6	5.0	3.0	4.0	10	5.0	A NC K
BZX84C6V8	Z5	6.4	6.8	7.2	5.0	2.0	4.0	15	5.0	A NC K
BZX84C7V5	Z6	7.0	7.5	7.9	5.0	1.0	5.0	15	5.0	A NC K
BZX84C8V2	Z7	7.7	8.2	8.7	5.0	0.7	5.0	15	5.0	A NC K
BZX84C9V1	Z8	8.5	9.1	9.6	5.0	0.5	6.0	15	5.0	A NC K
BZX84C10	Z9	9.4	10.0	10.6	5.0	0.2	7.0	20	5.0	A NC K
BZX84C11	Y1	10.4	11.0	11.6	5.0	0.1	8.0	20	5.0	A NC K
BZX84C12	Y2	11.4	12.0	12.7	5.0	0.1	8.0	25	5.0	A NC K
BZX84C13	Y3	12.4	13.0	14.1	5.0	0.1	8.0	30	5.0	A NC K
BZX84C15	Y4	13.8	15.0	15.6	5.0	0.05	10.5	30	5.0	A NC K
BZX84C16	Y5	15.3	16.0	17.1	5.0	0.05	11.2	40	5.0	A NC K
BZX84C18	Y6	16.8	18.0	19.1	5.0	0.05	12.6	45	5.0	A NC K
BZX84C20	Y7	18.8	20.0	21.2	5.0	0.05	14.0	55	5.0	A NC K
BZX84C22	Y8	20.8	22.0	23.3	5.0	0.05	15.4	55	5.0	A NC K
BZX84C24	Y9	22.8	24.0	25.6	5.0	0.05	16.8	70	5.0	A NC K
BZX84C27	Y10	25.1	27.0	28.9	2.0	0.05	21.0	80	2.0	A NC K
BZX84C30	Y11	28.0	30.0	32.0	2.0	0.05	18.9	80	2.0	A NC K
BZX84C33	Y12	31.0	33.0	35.0	2.0	0.05	23.1	80	2.0	A NC K

'TMPZ' TEMPERATURE-COMPENSATED ZENER DIODES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_{ZT} (mA)	V_Z Nom. (V)	Z_{ZT} Max. (Ω)	Temp. Coefficient (±ppm/°C)	ΔV_Z Max. (±mV/°C)	Test Temperature (°C)	Pinning 1, 2, 3
TMPZ4565	0.5	6.4	200	100	0.64	0 / +25 / +75	A K NC
TMPZ4565A	0.5	6.4	200	100	0.64	-55 / +25 / +100	A K NC
TMPZ4566	0.5	6.4	200	50	0.32	0 / +25 / +75	A K NC
TMPZ4566A	0.5	6.4	200	50	0.32	-55 / +25 / +100	A K NC
TMPZ4570	1.0	6.4	100	100	0.64	0 / +25 / +75	A K NC
TMPZ4570A	1.0	6.4	100	100	0.64	-55 / +25 / +100	A K NC
TMPZ4571	1.0	6.4	100	50	0.32	0 / +25 / +75	A K NC
TMPZ4571A	1.0	6.4	100	50	0.32	-55 / +25 / +100	A K NC
TMPZ4575	2.0	6.4	50	100	0.64	0 / +25 / +75	A K NC
TMPZ4575A	2.0	6.4	50	100	0.64	-55 / +25 / +100	A K NC
TMPZ4576	2.0	6.4	50	50	0.32	0 / +25 / +75	A K NC
TMPZ4576A	2.0	6.4	50	50	0.32	-55 / +25 / +100	A K NC

SERIES TND

DIODE ARRAYS

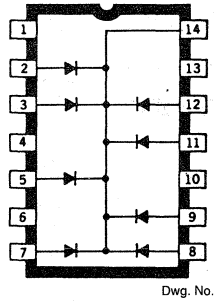


Dwg. No. A-10,903

TND903
TND907
TND908
TND918
TND921

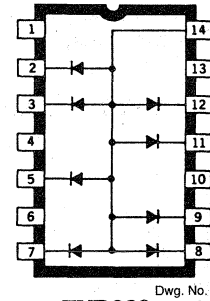
The TND series consists of diode arrays packaged in 14-pin and 16-pin dual in-line plastic packages for easy automatic insertion and better printed circuit board density.

In addition to the diode characteristics for standard products shown here, arrays consisting of diodes with 1N3070, 1N3595, 1N3600, 1N4153, or 1N4447 characteristics can be furnished on request. Other package configurations are available on special order.



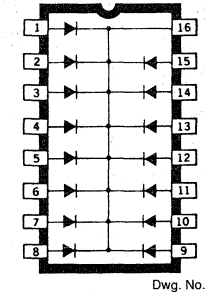
Dwg. No. A-13,359

TND933
TND940



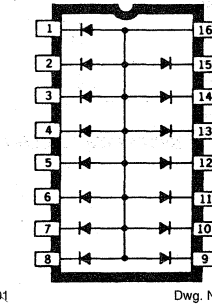
Dwg. No. A-13,360

TND938
TND939



Dwg. No. A-10,901

TND905



Dwg. No. A-13,361

TND942

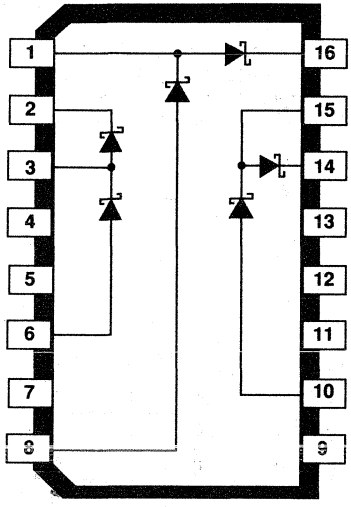
ELECTRICAL CHARACTERISTICS at T_A = +25°C

Device Type	V_{BR} Min. (V)	V_F Max. (V)	V_F @I_F (mA)	I_R Max. (nA)	I_R @ V_R (V)	Device Type	V_{BR} Min. (V)	V_F Max. (V)	V_F @I_F (mA)	I_R Max (nA)	I_R @ V_V (V)
TND903	75	1.0	100	—	—	TND933	60	1.0	100	100	40
TND905	100	1.0	10	—	—	TND938	60	1.0	100	100	40
TND907	120	1.0	100	10	50	TND939	40	1.0	100	100	25
TND908	100	1.0	10	—	—	TND940	40	1.0	100	100	25
TND918	75	1.0	50	—	—	TND942	75	1.0	100	100	25
TND921	75	1.0*	10	—	—						

* All diodes match to with ±15 mV at I_F = 10 mA.

TND8000

SCHOTTKY DIODE ARRAY



Dwg. PD-001

Schottky barrier diodes combine high rectification efficiency with high switching speeds and low series resistance. The six-diode TND8000 array is designed specifically for clamping applications with three-phase brushless dc motor drivers. It is supplied in a surface-mountable 16-lead small-outline integrated circuit (SOIC) plastic package for use over the operating temperature range of -40°C to +125°C.

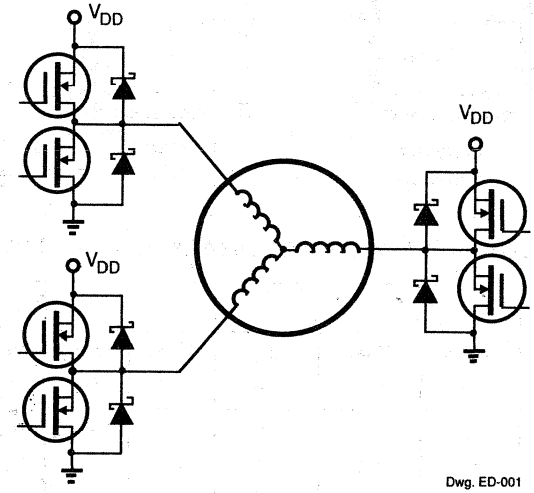
FEATURES

- High Forward Conductance
  400 mV Typical at 100 mA
- 500 mA Forward Current
- 15 V Reverse Voltage

BENEFITS

- Ideal for Disk and Tape Drives Using a 5 V or 12 V Supply
- Low Voltage Drop to Critical Low Supply Voltage Applications
- Reduced Part Count Results In Lower Insertion Cost and Increased Reliability

TYPICAL APPLICATION



Dwg. ED-001

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Forward Current, I_F . . . . . 1.0 A
Reverse Voltage, V_R . . . . . 15 V
Package Power Dissipation,
P_D . . . . . 1.5 W*
Operating Temperature Range,
T_A . . . . . -40°C to +125°C
Storage Temperature Range,
T_S . . . . . -65°C to +150°C

*Derate linearly to 0 W at T_A = +150°C.

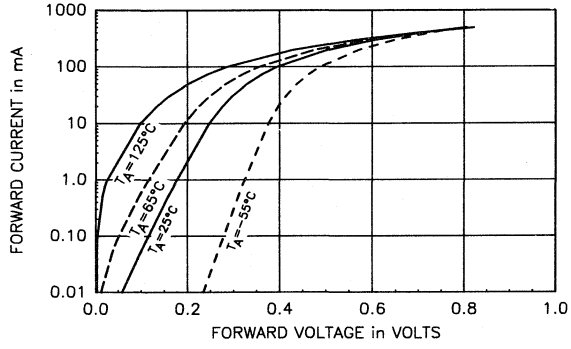
TND8000
SCHOTTKY DIODE ARRAY

ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise specified).

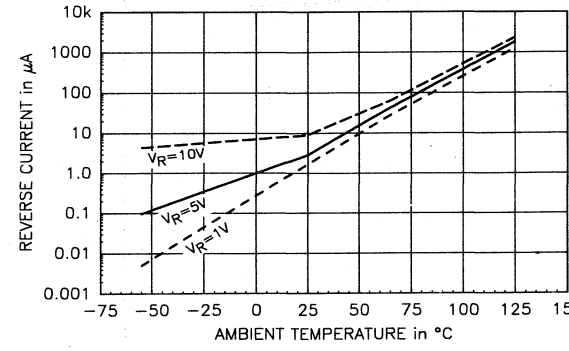
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 200 µA	15	20	—	V
Reverse Leakage Current	I_R	V_R = 10 V	—	10	100	µA
Forward Voltage	V_F	I_F = 100 mA	—	400	500	mV
Junction Capacitance	C_T	V_R = 0 V, f = 1 MHz	—	370	—	pF
Reverse Recovery Time	t_{rr}	$I_F = I_R$ = 100 mA	—	32	—	ns

TYPICAL CHARACTERISTICS

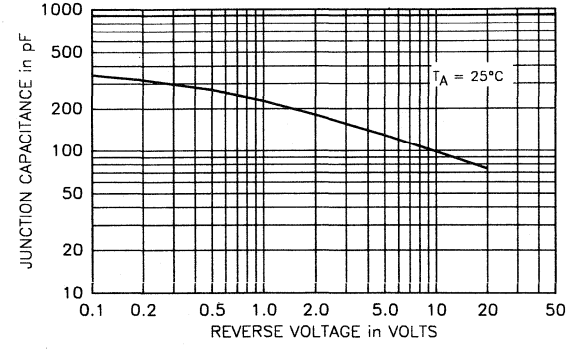
FORWARD VOLTAGE vs FORWARD CURRENT



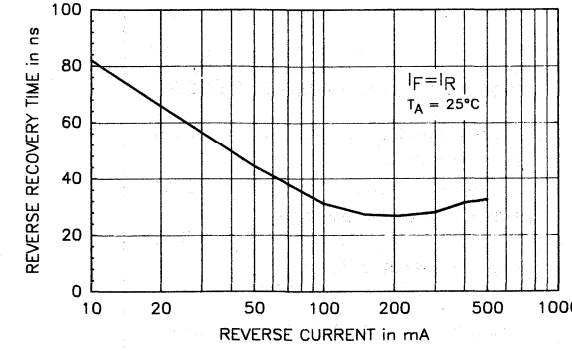
REVERSE CURRENT vs TEMPERATURE



JUNCTION CAPACITANCE vs REVERSE VOLTAGE

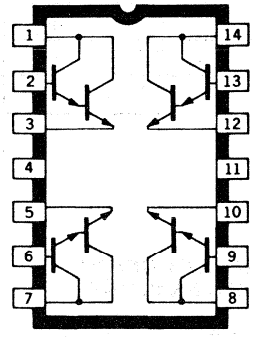


REVERSE RECOVERY TIME vs REVERSE CURRENT



TPP4000

MEDIUM-POWER DARLINGTON ARRAY



Dwg. No. A-10,782A

This medium-power array consists of four Darlington pairs in a single 14-pin dual in-line plastic package. Features include a collector-current rating of 4 A, a minimum h_{FE} of 2000, and a package power dissipation rating of 2 W.

The standard molded dual in-line package is identical to the type used for many integrated circuits. It offers superior mechanical protection for circuit elements during automatic insertion into printed wiring boards.

ABSOLUTE MAXIMUM RATINGS

Collector Current, I_C . . . . . **4.0 A**
Power Dissipation,
P_D (total package) . . . . . **2 W***
Operating Temperature Range,
T_A . . . . . **-55°C to +150°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

* Derate at the rate of 16 mW/°C above T_A = +25°C

TPP4000
DARLINGTON ARRAY

ELECTRICAL CHARACTERISTICS at T_A = +25°C

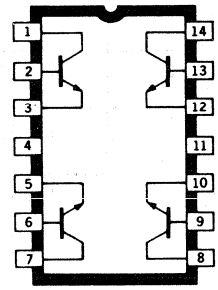
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 100 µA	40	50	—	V
Collector-Base Breakdown Voltage	BV_{CBO}	I_C = 100 µA	50	60	—	V
Emitter-Base Breakdown Voltage	BV_{EBO}	I_E = 100 µA	12	14	—	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 30 V	—	10	100	nA
Emitter-Cutoff Current	I_{EBO}	V_{EB} = 10 V	—	10	100	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_B = 1.0 mA, I_C = 1.0 A	—	1.0	1.5	V
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	I_B = 1.0 mA, I_C = 1.0 A	—	1.6	2.0	V
Static Forward Current-Transfer Ratio	h_{FE}	V_{CE} = 5.0 V, I_C = 500 mA	2000	—	—	—
		V_{CE} = 5.0 V, I_C = 1.0 A	2000	—	—	—
		V_{CE} = 5.0 V, I_C = 2.0 A	2000	—	—	—

SERIES TPQ

QUAD TRANSISTOR ARRAYS

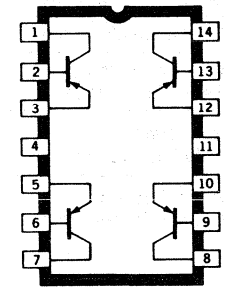
Series TPQ quad transistor arrays are general-purpose silicon transistor arrays consisting of four independent devices.

All of these devices are furnished in a 14-pin dual in-line plastic package. The molded package is identical to that used with most consumer integrated circuits and offers superior mechanical protection during insertion into printed wiring boards.



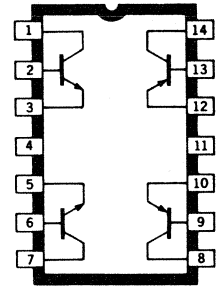
Dwg. No. A-10,050A

TPQ2222 TPQ2222A TPQ2369 TPQ6427 TPQ3904 TPQA06 TPQA05



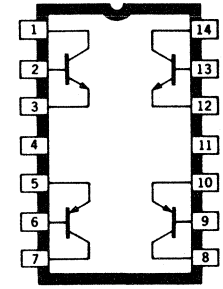
Dwg. No. A-10,051A

TPQ2907 TPQ2907A TPQ5401 TPQ3906 TPQA56 TPQA55



Dwg. No. A-10,052A

TPQ6002



Dwg. No. A-10,053A

TPQ6502 TPQ6700

ABSOLUTE MAXIMUM RATINGS

Power Dissipation, P_D
(Each Transistor) . . . . . **500 mW**
(Total Package) . . . . . **2.0 W***
Operating Temperature Range,
T_A . . . . . **-55°C to +150°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

* Derate at the rate of 16 mW/°C above T_A = +25°C

SERIES TPQ
QUAD TRANSISTOR ARRAYS

ELECTRICAL CHARACTERISTICS at T_A = +25°C

Part Number	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max @ V_{CB} (nA)	(V)	DC Current Gain h_{FE} Min.	Conditions I_C (mA)	V_{CE} (V)	Saturation Voltage V_{CE} Max. (V)	V_{BE} Max. (V)	@ I_C (mA)	f_T Min. (MHz)	@ I_C (mA)	Max. (pF)	Similar Discrete Devices
Four NPN Devices															
TPQ2222	60	40	5.0	50	50	75	10	10	0.40	1.30	150	200	20	8.0	2N2222
						100	150	10	1.60	2.60	300				
						30	300	10							
TPQ2222A	75	40	6.0	50	50	75	10	10	0.40	1.30	150	200	20	8.0	2N2222A
						100	150	10	1.60	2.60	300				
						30	300	10							
TPQ2369	40	15	4.5	400	20	40	10	1.0	0.25	0.90	10	450	10	4.0	2N2369
						20	100	2.0							
TPQ3904	60	40	6.0	50	40	30	0.1	1.0	0.20	0.85	10	250	10	4.0	2N3904
						50	1.0	1.0							
						75	10	1.0							
TPQ6427	50	40	12	100	30	5k	10	5.0	1.5	2.0	100	125	10	8.0	2N6427
						10k	100	5.0							
TPQA05	60	60	4.0	100	(Note 2)	50	10	1.0	0.25	—	100	—	—	10	MPSA05
						50	100	2.0							
TPQA06	80	80	4.0	100	(Note 3)	50	10	1.0	0.25	—	100	—	—	10	MPSA06
						50	100	2.0							

NOTE: 1. Base-emitter voltage shown is $V_{BE(ON)}$ at indicated I_C, V_{CE} = 5.0 V.

2. I_{CES} at V_{CE} = 50 V, V_{BE} = 0

3. I_{CES} at V_{CE} = 60 V, V_{BE} = 0

SERIES TPQ
QUAD TRANSISTOR ARRAYS

ELECTRICAL CHARACTERISTICS at T_A = +25°C

Part Number	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max (nA)	@V_{CB} (V)	DC Current Gain h_{FE} Min.	Conditions I_C (mA)	V_{CE} (V)	Saturation Voltage V_{CE} Max. (V)	V_{BE} Max. (V)	@I_C (mA)	f_T Min. (MHz)	@I_C (mA)	Max. (pF)	Similar Discrete Devices
Four PNP Devices															
TPQ2907	-60	-40	-5.0	50	-30	75 100 50	10 150 300	-10 -10 -10	-0.40 -1.60	-1.30 -2.60	150 300	200	50	8.0	2N2907
TPQ2907A	-60	-60	-5.0	50	-30	75 100 50	10 150 300	-10 -10 -10	-0.40 -1.60	-1.30 -2.60	150 300	200	50	8.0	2N2907A
TPQ3906	-40	-40	-5.0	50	-30	40 60 75	0.1 1.0 10	-1.0 -1.0 -1.0	-0.25	-0.85	10	200	10	4.5	2N3906
TPQ5401	-160	-150	-5.0	100	(Note 4)	50 60 50	1.0 10 50	-5.0 -5.0 -5.0	-0.20 -0.50	1.00 1.00	10 50	100	10	6.0	2N5401
TPQA55	-60	-60	-4.0	100	(Note 5)	50 50	10 100	-1.0 -2.0	-0.25	—	100	—	—	15	MPSA55
TPQA56	-80	-80	-4.0	100	(Note 6)	50 50	10 100	-1.0 -2.0	-0.25	—	100	—	—	15	MPSA56
Two NPN/Two PNP Devices (Note 7)															
TPQ6002	60	30	5.0	30	50	50 75 100 30	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2222 and 2N2907
TPQ6502	60	30	5.0	30	50	50 75 100 30	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2222 and 2N2907
TPQ6700	40	40	5.0	50	30	30 50 70	0.1 1.0 10	1.0 1.0 1.0	0.25	0.90	10	200	10	4.5	2N3904 and 2N3906

NOTE: 4. I_{CES} at V_{CE} = 120 V, V_{BE} = 0.

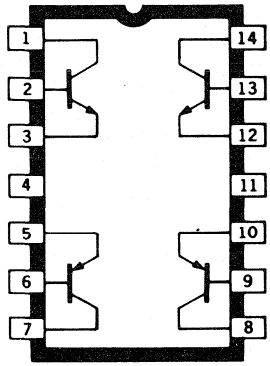
5. I_{CES} at V_{CE} = 50 V, V_{BE} = 0.

6. I_{CES} at V_{CE} = 60 V, V_{BE} = 0.

7. Complimentary pairs. Polarity shown is for NPN devices.

CHIPS-IN-DIPS

CUSTOM-ARRAY PROGRAM



Dwg. No. A-10,053A

MAXIMUM RATINGS

Package Power Dissipation, P_D . . . . . **2 W***

Operating Temperature Range,

T_A . . . . . **-55°C to +150°C**

Storage Temperature Range,

T_S . . . . . **-65°C to +150°C**

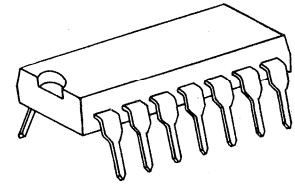
* Derate at the rate of 16 mW/°C above T_A = +25°C

The Chips-In-DIPs program uses discrete semiconductor chips from a comprehensive line of standard devices to create transistor, diode, and Darlington arrays assembled to users' specifications.

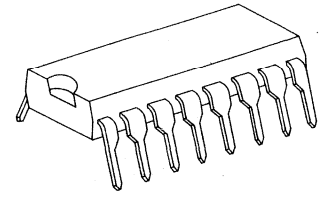
The program provides extensive special-design capabilities for applications with design restrictions such as short lead time, small quantities, and unique circuit requirements. Chips-In-DIPs is an attractive alternative to development of monolithic integrated circuits and commitment to high-volume purchases.

Assembly of discrete devices in dual in-line packages allows relatively higher power dissipation while reducing handling and boosting component density. The standard molded DIP, the package most commonly used for automated circuit assembly, offers superior mechanical protection of components during automatic insertion into printed wiring boards.

Series TPQ transistor arrays, Series TND diode arrays, and Series TPP Darlington arrays are among standard products offered by the Chips-In-DIPs program. Semiconductor chips available for custom-array products include those described in the most recent issue of Brochure CN-193.



Dwg. No. A-11,562A



Dwg. No. A-11,420A

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HALL-EFFECT & OPTOELECTRONIC SENSOR ICs 4

INTEGRATED CIRCUITS to MIL-STD-883 5

AUTOMOTIVE, SIGNAL-PROCESSING, & CONSUMER ICs 6

DISCRETE TRANSISTORS, DIODES, & ARRAYS 7

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SECTION 8. QUALITY & RELIABILITY INFORMATION

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RELIABILITY

BACKGROUND INFORMATION

CMOS, bipolar, and BiMOS integrated circuits exhibit the same reliability characteristics as other electronic devices in that the failure rate has three distinct phases:

1) Within a relatively short time after manufacture, certain failure mechanisms appear under moderate levels of stress. The failure during this period is termed "infant mortality."

2) After the period of infant mortality, failure rate falls dramatically and, for a long period, only infrequent random failures occur.

3) Finally, device packages can actually wear out and the failure rate will increase again.

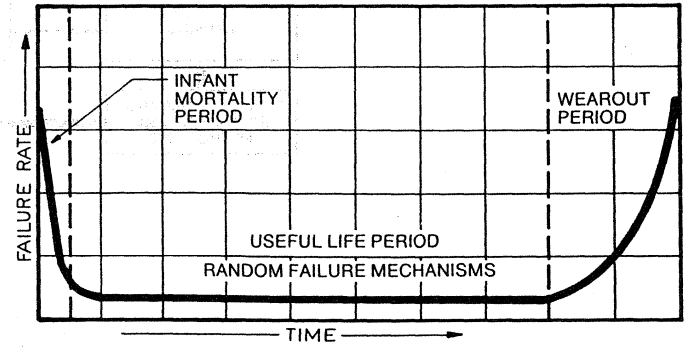
When the failure rate for electronic components is plotted as a function of time, the result is a characteristic bathtub curve. While the bathtub shape is universal throughout the industry, actual values for a single component type can vary greatly from one manufacturer to another. Through many years of experience in the manufacture of integrated circuits, design rules and processing techniques have been developed to:

1) Minimize the infant mortality failure mechanisms.

2) Detect potential failures before they reach the customer.

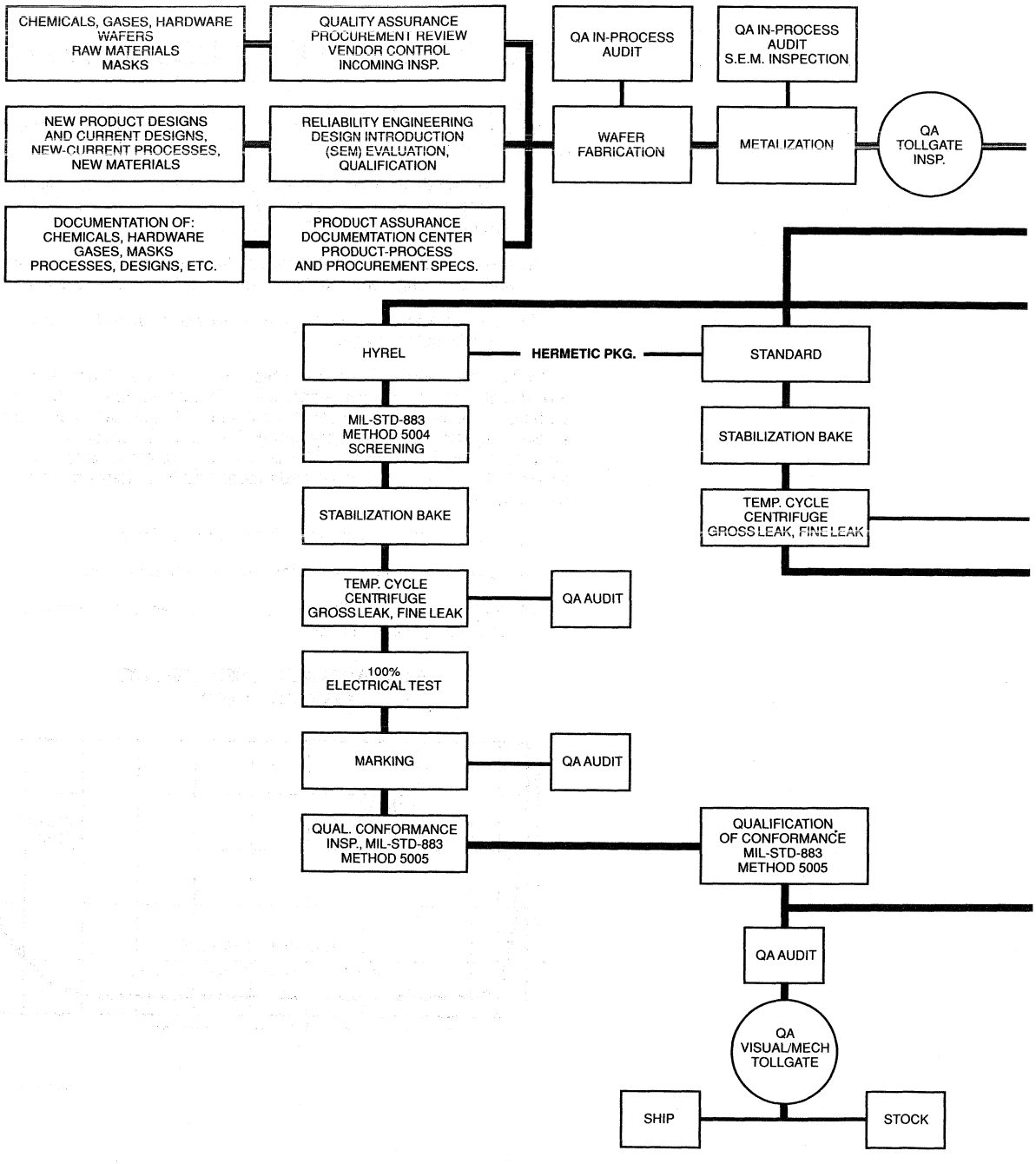
3) Control wear-out so that operating life far exceeds the lifetime required by the customer.

RELIABILITY LIFE CYCLE
TYPICAL CURVE

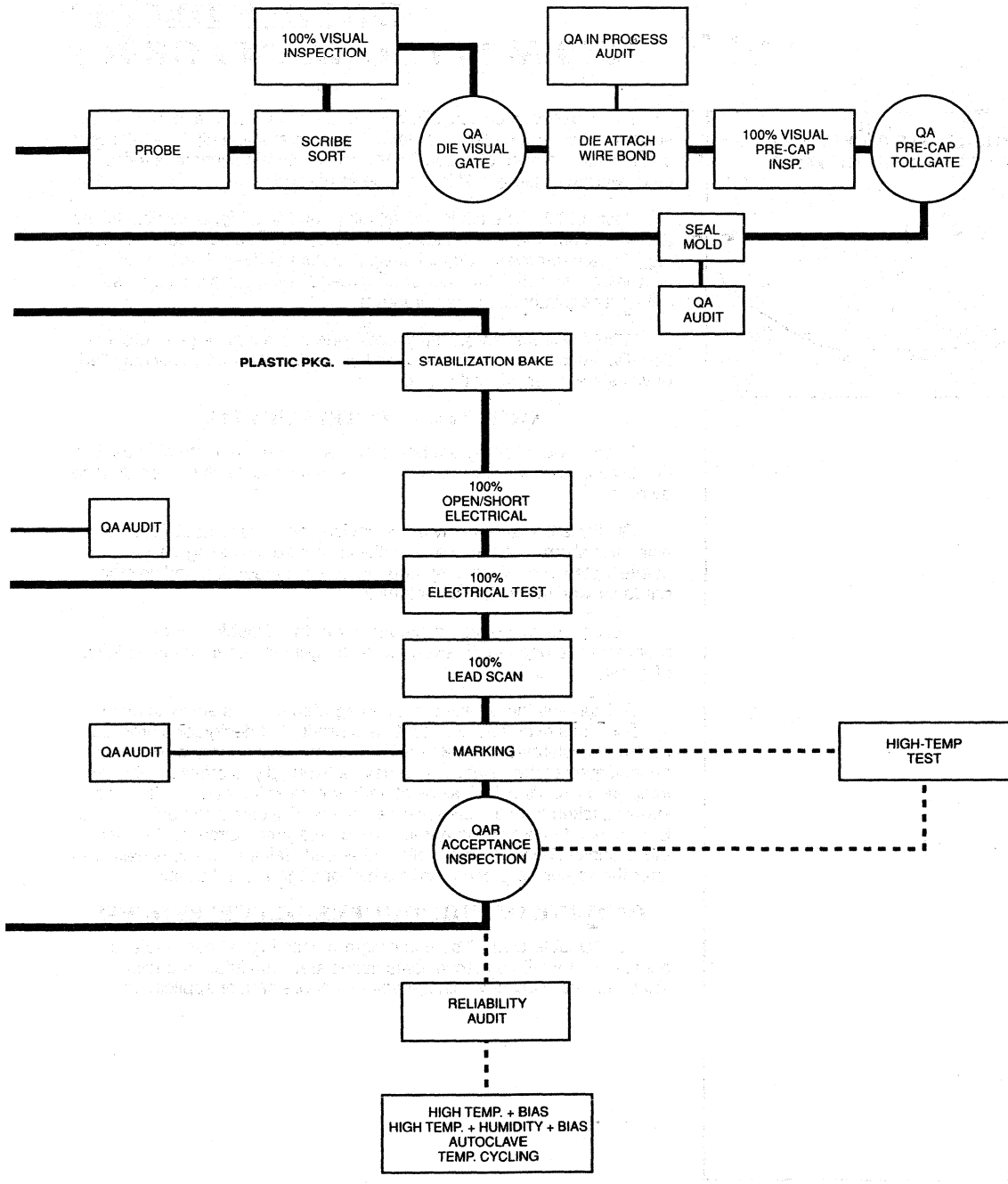


Dwg. No. A-14,410

QUALITY ASSURANCE FLOW CHART



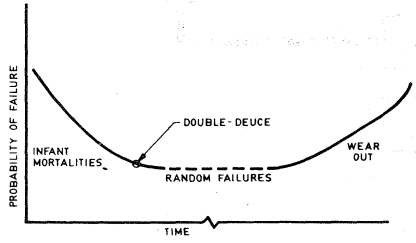
QUALITY ASSURANCE FLOW CHART



Dwg. No. B-1474

'DOUBLE DEUCE' BURN-IN PROGRAM FOR ICs

PROBABILITY OF FAILURE AS A FUNCTION OF TIME



Dwg. No. A-11,417

The expense of device failure is more than the time and money spent locating and replacing a defective integrated circuit. The total cost can include the price ot assembly rework, system downtime, service calls, warranty claims and lost customer goodwill.

Costs of $25 for each in-house failure and $250 for each field failure are not uncommon. At a relatively low cost, the "Double-Deuce" screening program removes marginal devices before shipment. Improved customer satisfaction with performance and reliability is an immeasurable but certain bonus of the program.

"Double-Deuce" screening is done during the last stage of production. Because the screening is done by the manufacturer, only qualified devices are received by the user.

QUALITY AND RELIABILITY

Quality and reliability are terms that are often used interchangeably. Quality implies reliability, but a product's merit should always be defined by both.

Quality is the extent to which a device conforms to specifications when it is shipped to the user. Quality is verified by testing. Inspections at every step of production ensure the devices meet demanding standards for workmanship and materials.

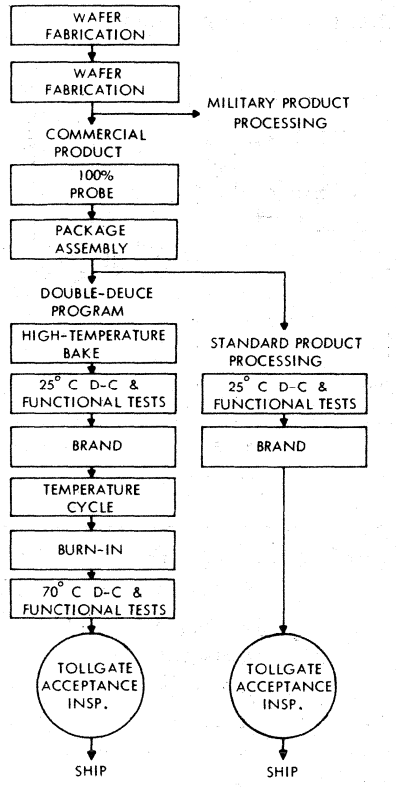
Inspections of integrated circuits under the "Double-Deuce" program have been made even more stringent to secure a higher level of quality.

Reliability is the measure of an integrated circuit's ability to meet specifications over time. Reliability is a product of design and process control. Accelerated-life tests provide the manufacturer and user with an indication of the reliability of a device. Normally, a small number of integrated circuits exhibit signs of early failure or infant mortality. This statistic, taken from the steepest part of the IC lifetime probability curve, is often used to project time-to-failure for integrated circuits. Because the "Double-Deuce" program eliminates early failures, devices delivered after the screening process have a higher degree of reliability.

OUTLINE OF THE 'DOUBLE-DEUCE' PROCESS

The "Double-Deuce" burn-in program uses high stress levels to accelerate the failure mechanisms associated with infant mortality. These normally occur within the first few hours of user application.

'DOUBLE DEUCE' BURN-IN PROGRAM FOR ICs



Dwg. No. A-11,418A

Although typically less than 1 percent of a lot will be rejected, user confidence in lot integrity is greatly improved. The screening program is designed to eliminate the following failure modes:

Stress	Failure Mode
High Temp. Bake	Contamination
Temp. Cycling	Package-Related
Burn-in	Process-Related
High Temp. Testing	Electrical Degradation

The majority of early integrated circuit failures (infant mortality or ionic contamination) can be attributed to manufacturing defects, package or assembly defects, or final test escapes. The "Double-Deuce" program is designed to eliminate weaker parts, reduce or eliminate user shipment inspection, assembly rework, system checkout, and warranty returns.

TEST PROCEDURES

The "Double-Deuce" burn-in program includes five test procedures:

1. HIGH-TEMPERATURE BAKE

This is a process designed to stabilize electrical drift and to accelerate chemical degradation such as surface contamination. It is a four-hour bake at +175°C without electrical stress (similar to MIL-STD-883, Method 1008).

2. TEMPERATURE CYCLING

This is a screening process designed to mechanically stress the integrated circuit by alternately heating and cooling it. Potential failures are seal or bond failure, cracked packages or chips.

The process has 10 cycles with 10 minutes of dwell at -65°C and 10 minutes of dwell at +150°C (air to air), with a maximum transfer time of five minutes (MIL-STD-883, Method 1010, Condition C). At manufacturer's option, this process may be changed to thermal shock (liquid to liquid) for 10 cycles, five minutes at 0°C and five minutes at +100°C with a transfer lime of 10 seconds (MIL-STD-883, Method 1011, Condition A).

3. BURN-IN

The burn-in, or accelerated-life test, is performed to screen out marginal devices, those with inherent defects, or defects resulting from manufacturing deviations that can cause time-dependent or stress-dependent failures. Without this conditioning, marginal circuits that initially meet all specifications could exhibit early lifetime failures under normal operating conditions. The test is conducted for 96 hours at a junction temperature of +150°C under electrical stress conditions (similar to MILSTD-883, Method 1015) such as:

Type of Device	Electrical Stress
Bipolar Interface	Steady-State Reverse Bias
Linear Devices	Steady-State Forward Bias
I^2L and MOS Logic	Clocked

'DOUBLE DEUCE' BURN-IN PROGRAM FOR ICs

The burn-in conditions (96 hours at T_J = +150°C) are equivalent to 525 hours at T_J = +125°C for ionic contamination (E_A = 1.0 eV) or for 192 hours at T_J = +125°C for infant mortality defects (E_A = 0.4 eV).

4. HIGH TEMPERATURE TEST

Every device is subjected to complete electrical tests at +70°C for function and dc parameters (similar to MIL-STD-883, Methods 3001 through 3014 and 4001 through 4007, as applicable). Relaxed +25°C limits or published high-temperature limits, are used to remove devices with circuit anomalies such as beta mismatch, high leakage current, and intermittent bonds, which may only affect the circuit at higher temperatures.

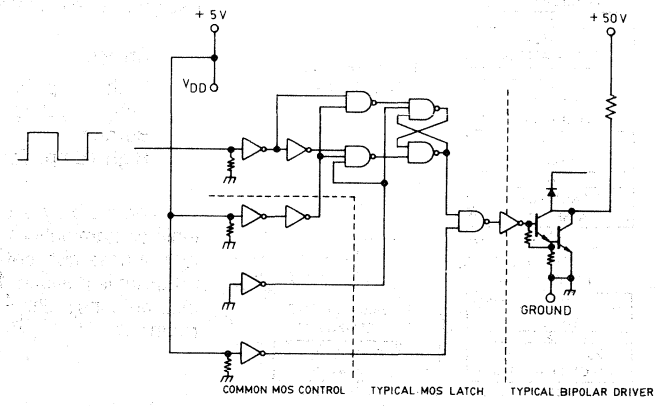
5. OUTGOING QUALITY CONTROL INSPECTION

A "Double-Deuce" product is inspected to an outgoing sampling plan that guarantees the product will meet an acceptable quality level of 0.10%.

HOW TO ORDER DEVICES IN 'DOUBLE-DEUCE' PROGRAM

Devices processed in the "Double-Deuce" burn-in program are specified by adding the suffix "BU" to the end of the part number. For example, to order UDN2981A with this processing, specify UDN2981ABU: to order UDN6118A-1, specify UDN6118A-1BU.

TYPICAL BiMOS DRIVER BURN-IN



Dwg. No. A-11,419

DEVICES CURRENTLY AVAILABLE

ULN2064B	UCN5800A
ULN2069B	UCN5801A
UDN2595A	UDN5810A
UDN2981A	UCN5821A
UDN2983A	UDN6118A

Unlisted devices may be processed In the "Double-Deuce" burn-in program if order size is sufficient.

MILITARY SCREENING FLOWS

MIL-M 38510 (1)	DESC/SMDP DRAWING (2, 3)	883 COMPLIANT (2, 3)
Wafer Fabrication, DESC Certified		
Wafer Probe		
Die Inspection, MIL-STD-883, Method 2010		
Die Bond		
Wire Bond		
Internal Visual, MIL-STD-883, Method 2010		
Package Seal		
Stabilization Bake, MIL-STD-883, Method 1008		
Temperature Cycle, MIL-STD-883, Method 1010		
Constant Acceleration, MIL-STD-883, Method 2001		
Fine Seal, MIL-STD-883, Method 1014		
Gross Seal, MIL-STD-883, Method 1014		
QC External Visual, MIL-STD-883, Method 2009		
Interim Electrical Test, MIL-STD-883, Method 5005, +25°C		
Burn-in Screen, MIL-STD-883, Method 1015		
Static Electrical, MIL-STD-883, Method 5005, +25°C, PDA = 5%		
Static Electrical, MIL-STD-883, Method 5005, +125°C		
Static Electrical, MIL-STD-883, Method 5005, -55°C		
Dynamic and Functional Electrical, MIL-STD-883, Method 5005		
Additional Tests as Specified in the Applicable Drawing		
Quality Conformance Inspection, MIL-STD-883, Method 5005, Class B		
External Visual Inspection, MIL-STD-883, Method 2009		
Shipment		

1. All MIL-M-38510 processing is performed in domestic (USA) facilities certified by the Defense Electronics Supply Center (DESC).
2. All high-reliability manufacturing processes are monitored by the Quality Control Department through gating operations at regular and periodic audits.
3. DESC/SMDP Drawing and 883 Compliant devices may include some offshore processing.

QUALITY CONFORMANCE

The Quality and Reliability Department performs all quality conformance inspection tests required by MIL-STD-883, Methods 5005 and 5010. The data from these tests is on file.

GROUP B TESTING

Package-related testing is performed in accordance with the alternate Group B inspection procedure for Class 8 product per MIL-STD-883, Method 5005, once per date code, package type, and lead finish.

Subgroup	Test	MIL-STD-883 Method
1	Physical Dimensions	2016
2	Resistance to Solvents	2015
3	Solderability	2003
4	Internal Visual/Mechanical	2014
5	Bond Strength	2011
7	Fine and Gross Leak	1014

GROUP C TESTING

Die-related tests are performed once every 13 weeks per generic group.

Subgroup	Test	MIL-STD-883 Method
1	Steady-State Life	1005
2	Temperature Cycle	1010
	Constant Acceleration	2001
	Fine and Gross Leak	1014
	External Visual	1010
	End-Point Electrical Parameters	—

GROUP D TESTING

Package-related tests performed once every 26 weeks per package type, pin count, and lead finish.

Subgroup	Test	MIL-STD-883 Method
1	Physical Dimensions	2016
2	Lead Integrity	2004
	Fine and Gross Leak	1014
3	Thermal Shock	1011
	Temperature Cycle	1010
	Moisture Resistance	1004
	Fine and Gross Leak	1014
	Visual	1004/1010
	End-Point Electrical Parameters	—
4	Mechanical Shock	2002
	Vibration, Variable Frequency	2007
	Constant Acceleration	2001
	Fine and Gross Leak	1014
	Visual	1004
	End-Point Electrical Parameters	—
5	Salt Atmosphere	1009
	Fine and Gross Leak	1014
	Visual	1009
6	Internal Water Vapor Content	1018
7	Adhesion of Lead Finish	2025
8	Lid Torque	2024

RELIABILITY REPORT

RELIABILITY OF SERIES UCN5800A BiMOS DRIVERS

This report summarizes accelerated-life tests that have been performed on Series UCN5800A BiMOS integrated circuits and provides information that can be used to calculate the failure rate at any junction operating temperature.

Product-reliability improvement is a continuous and evolving process. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, burn-in and accelerated-life tests:

1) Qualification testing is performed at an ambient temperature of +125°C, reduced so as to limit junction temperature to +150°C, for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure-rate data in a reasonable period of time.

2) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from the Double-Deuce™ burn-in program found that most failures are due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, are typically less than 0.1%.

3) Accelerated-life testing is performed at junction temperatures above +125°C and is used to generate failure-rate data.

ACCELERATED-LIFE TESTS

Accelerated-life tests are performed on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution can be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C).

b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.

c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminate level.

Table I contains data produced by life tests that were conducted at +150°C. The data includes the number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing allocation of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5 x for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 200 hours at +150°C to 1000 hours at +125°C.

The data at the bottom of Table I are compiled by calculating the probability of success (P_s), the cumulative probability of success, the probability of failure (P_f) and the percentage of failed units in each time period.

CUMULATIVE PERCENT FAILURES

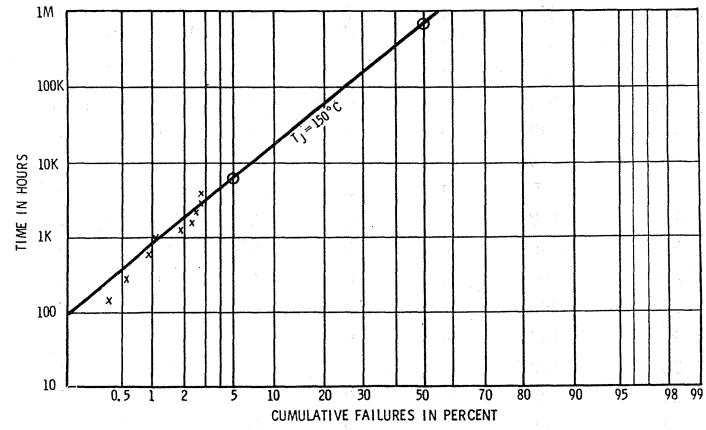


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FIGURE 1

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots as a straight line. A line of best fit is drawn through the plotted points and extended to determine the median life-time at the 50% fail-point. The median life at a junction temperature of +150°C is, in this case, 682,000 hours.

The log-normal distribution is commonly used because most semiconductor device data fit such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1]

TABLE I

TEST RESULTS at T_j = +150°C

TEST NUMBER	QTY.	HOURS ON TEST: 48	150	300	600	1000	1200	1800	2400	3000	4000
		NUMBER OF FAILURES									
1	40	0	0	0	0	0	0	—	—	—	—
2	224	0	2	0	2	0	2	0	0	—	—
3	95	0	0	0	—	—	—	—	—	—	—
4	99	0	0	0	1	1	0	3	—	—	—
5	700	—	3	—	—	5	—	—	—	—	—
6	50	0	1	0	0	0	3	0	—	—	—
7	50	0	0	0	1	0	0	0	0	—	—
8	50	0	1	0	0	0	0	0	0	0	—
9	40	0	0	0	0	0	0	1	—	—	—
10	240	0	0	0	—	—	—	—	—	—	—
11	1000	—	3	—	—	1	—	—	—	—	—
12	27	0	0	0	0	0	0	—	—	—	—
13	27	0	0	1	0	0	0	0	0	0	—
14	42	0	0	0	0	0	0	—	—	—	—
15	30	0	0	0	—	—	—	—	—	—	—
16	100	0	0	0	0	0	0	0	0	0	—
17	980	—	1	—	—	0	—	—	—	—	—
18	100	—	0	0	0	—	0	1	0	1	—
19	77	0	0	2	2	—	—	—	—	—	—
20	120	0	0	0	1	0	0	1	—	—	—
21	68	0	2	0	0	0	1	0	0	—	—
22	32	0	0	0	0	0	0	0	0	0	—
23	400	—	0	—	—	0	—	—	—	—	—
24	100	—	0	—	—	—	—	—	—	—	—
25	190	—	0	—	—	1	—	—	—	—	—
26	55	0	0	0	0	0	0	0	0	—	—
27	30	0	0	0	0	0	2	0	1	0	—
28	50	0	0	0	0	0	0	0	—	—	—
29	100	0	0	0	0	0	—	—	—	—	—
30	25	0	0	0	0	0	0	0	0	—	—
31	36	0	0	1	0	0	0	0	—	—	—
32	34	0	0	0	0	0	0	0	0	—	—
33	100	—	3	3	0	—	0	0	—	—	—
34	20	0	0	0	—	—	—	—	—	—	—
35	18	0	0	0	0	0	0	0	—	—	—
36	18	0	0	0	0	0	0	—	—	—	—
37	36	0	0	0	0	0	0	0	1	0	—
38	48	0	1	0	1	0	0	—	—	—	—

Continued next page...

TEST RESULTS at T_J = +150°C continued

TEST NUMBER	QTY.	HOURS ON TEST 48	150	300	600	1000	1200	1800	2400	3000	4000
		NUMBER OF FAILURES									
39	48	0	0	0	0	0	0	—	—	—	—
40	48	0	0	0	0	0	7	—	—	—	—
41	45	0	0	0	0	—	—	—	—	—	—
42	100	0	0	0	0	0	0	1	0	0	0
43	100	0	0	0	0	—	—	—	—	—	—
44	50	0	0	0	0	0	0	—	—	—	—
45	580	1	4	0	—	—	—	—	—	—	—
46	90	0	1	0	0	0	0	—	—	—	—
47	37	0	0	0	0	0	0	—	—	—	—
48	26	0	0	0	0	0	0	0	0	0	—
49	25	0	1	—	—	—	—	—	—	—	—
TOTAL ON TEST		3030	6629	3189	2222	5065	1895	1442	943	493	99
TOTAL FAILURES		1	23	7	8	8	15	7	2	1	0
TOTAL GOOD		3029	6606	3182	2214	5057	1880	1435	941	492	99
P_s		1.00	.997	.998	.996	.998	.992	.995	.998	.998	1.00
Cumulative P_s		1.00	.996	.994	.990	.989	.981	.976	.974	.972	.972
$P_f = 1-P_s$		.000	.004	.006	.010	.011	.019	.024	.026	.028	.028
Failures		0.03	0.38	0.60	0.96	1.11	1.90	2.37	2.58	2.78	2.78

The Arrhenius equation is:

$$V_r = V_r^o e^{-\epsilon/kT}$$

where V_r^o = a constant

ϵ = activation energy

k = Boltzmann's constant

T = absolute temperature in degrees Kelvin.

An activation energy of 1.0 electron-volt was established by testing Series ULN2000A, Series UDN5710M, and Series UDN2980A devices at multiple temperatures. Failure analysis of devices rejected during that test-ing also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

The median life-point is drawn on Arrhenius graph paper in Figure 2. The Arrhenius plot gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line is drawn through this point (or points when multiple temperatures are used) with a slope of ϵ = 1.0 eV.

Although not as statistically accurate as the median lifetime, the 5% fail-point can be read from Figure 1 and plotted parallel to the median-life line in Figure 2.

The median life at reduced junction temperatures can now be determined using Figure 2. It must be emphasized that this is junction temperature and *not* ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D R_{\theta JA} + T_A \text{ or } T_J = P_D R_{\theta JC} + T_C$$

The median lifetime, or 50% fail-point, as graphically determined in Figure 2, is approximately 22 years at +125°C or 190 years at +100°C junction temperature.

The approximate failure rate (FR) may be determined from FR = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life line. The actual instantaneous failure rate can be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$FR = 1/(2.7 \times 10^7 \text{ hours})$$

$$= 0.0037\%/1000 \text{ hours} = 37 \text{ FIT}$$

where FIT = failures per 10^9 unit-hours

Other failure-rate values have been calculated and appear in Table II.

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides a failure rate within design objectives.

Figure 2 shows that a design with a continuous operating junction temperature of +125°C (internal power dissipation plus external ambient temperature) would reach the 5% failure point in 4.5 years. Lowering the junction temperature to +100°C increases the time to the 5% failure point to 38 years.

A complete sequence of environmental tests, including temperature cycle, pressure cooker, and biased humidity tests, are continuously monitored to ensure that assembly and package technology remain within established units.

The environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

MEDIAN LIFE

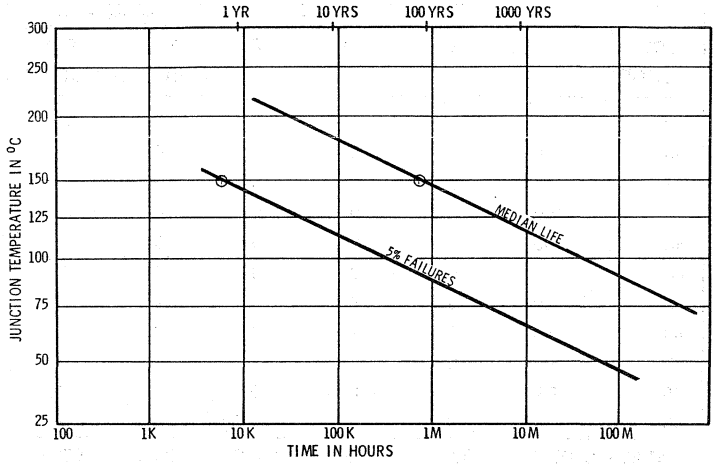

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FIGURE 2

TABLE II
SERIES UCN5800A FAILURE RATE

T_J (°C)	Median Life (h)	Failure Rate (%/1000 h)	Failures In Time (No./10^9unit-hours)
150	6.8×10^5	0.15	1466
125	3.8×10^6	0.026	263
100	2.7×10^7	0.0037	37
75	2.5×10^8	0.0004	4.0
50	3.3×10^9	0.000033	0.33

REFERENCES

1) Manchester, K. E., and Bird, D. W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions*, Vol. CHMT-3, No. 4, 1980, pp. 580-587.

2) Peck, D. S., and Trapp, O. D., *Accelerated Testing Handbook*, Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.*, p. 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control*, 1961, pp. 208-213.

RELIABILITY REPORT

RELIABILITY OF SERIES UDN6100A HIGH-VOLTAGE DISPLAY DRIVERS

This report summarizes accelerated-life tests that have been performed on Series UDN6100A integrated circuits and provides information that can be used to calculate the failure rate at any junction operating temperature.

Product-reliability improvement is a continuous and evolving process. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, accelerated tests, and burn-in:

1) Qualification testing is performed at an ambient temperature of +125°C for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure rates in a reasonable period of time.

2) Accelerated testing is performed at junction temperatures above +125°C and is used to generate failure-rate data.

3) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from the DoubleDeuce™ burn-in program found 1.27% failures in more than 325,000 pieces tested in a recent time period. Most failures were due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, were less than 0.1%.

ACCELERATED-LIFE TESTS

Accelerated-life tests are performed on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution may be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.

TABLE I

TEST RESULTS at T_J = +150°C

TEST NUMBER	BIAS VOLTS	QTY.	HOURS ON TEST 90	150	300	600	1200	1800	2000	5000	6000
			NUMBER OF FAILURES								
1	80	24	0	0	2	—	—	—	—	—	—
2	80	24	0	0	0	0	0	0	1	0	—
3	80	12	0	0	0	0	0	—	—	—	—
4	80	12	0	0	0	0	2	1	1	0	0
5	110	24	0	0	0	0	0	0	1	—	—
6	80	12	0	0	0	—	—	—	—	—	—
TOTAL ON TEST			108	108	108	72	72	58	57	31	8
TOTAL FAILURES			0	0	2	0	2	1	3	0	0
TOTAL GOOD			108	108	106	72	70	57	54	31	8
P_s			1.00	1.00	0.981	1.00	0.972	0.983	0.947	1.00	1.00
Cumulative P_s			1.00	1.00	0.981	0.981	0.954	0.938	0.888	0.888	0.888
$P_f = 1 - P_s$			0	0	0.019	0.019	0.046	0.062	0.112	0.112	0.112
Cumulative % Failures			0	0	1.9	1.9	4.6	6.2	11.2	11.2	11.2

b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.

c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminant level.

Table I contains Series UDN6100A data produced by life tests that were conducted at +150°C. The data include the number of test samples, number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing allocation of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5x for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 200 hours at +150°C to 1000 hours at +125°C. If these tests had been qualification tests, they would have ended at 200 hours at +150°C or 40 hours at +175°C.

The data at the bottom of Table I is compiled by calculating the probability of success (P_s), the cumulative probability of success, the probability of failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% fail-point. The median life at a junction temperature of +150°C is 100,000 hours, in this case.

The log-normal distribution is commonly and widely used because most semiconductor device data fit such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1] The Arrhenius equation is:

$$V_r = V_r^o e^{-\epsilon/kT}$$

where V_r^o = a constant

ϵ = activation energy

k = Boltzmann's constant

T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN2000A, Series UDN5710M, and Series UDN2980A devices at multiple temperatures. Failure analysis of devices rejected during this testing also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

The median life-point is drawn on Arrhenius graph paper in Figure 2. Arrhenius plotting paper gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line is drawn through this point (or points when multiple temperatures are used) with a slope of E = 1.0 eV.

Although not as statistically accurate as the median lifetime, the 5% fail-point can be read from Figure 1 and plotted parallel to the median-life line in Figure 2.

The median life with lower junction temperatures may now be determined by using Figure 2. It must be emphasized that this is junction temperature and not ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D R_{\theta JA} + T_A \text{ or } T_J = P_D R_{\theta JC} + T_C$$

The median lifetime, or 50% fail-point, as determined in Figure 2, is approximately 100 years at +125°C or 1,000 years at +90°C junction temperature.

The approximate failure rate (FR) can be determined from FR = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life plot. The

CUMULATIVE PERCENT OF FAILURES

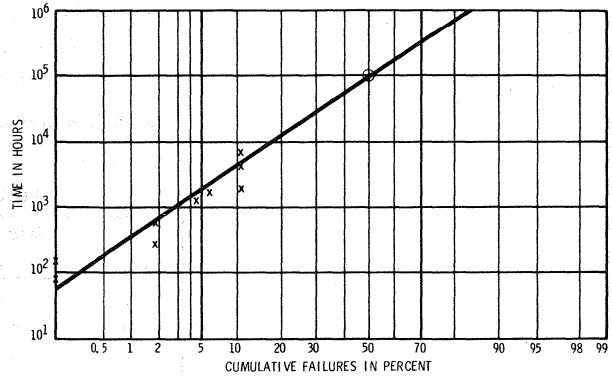

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FIGURE 1

MEDIAN LIFE

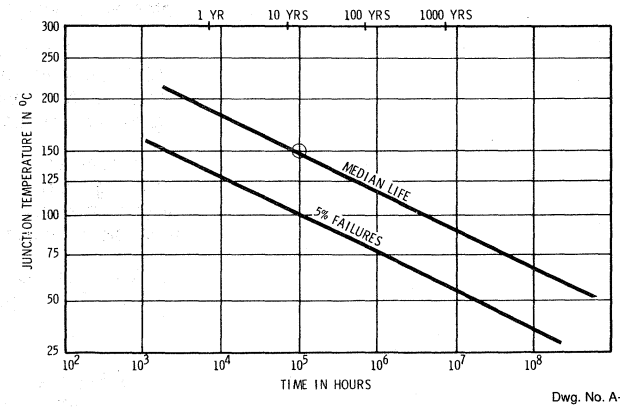

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FIGURE 2

actual instantaneous failure rate may be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$FR = 1/(4 \times 10^6 \text{ hours})$$

$$= 0.025\%/1000 \text{ hours}$$

Other failure rate values have been calculated in Table II.

TABLE II
SERIES ULN6100A FAILURE RATES

T_J (°C)	Median Life (h)	Failure Rate (%/1000 h)	Failures In Time (No./10^9 unit-hours)
125	6×10^5	0.167	1670
100	4×10^6	0.025	250
75	4×10^7	0.0025	25
50	5×10^8	0.0002	2

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides failure rates within design objectives.

Figure 2 shows that a design with a junction temperature of +100°C, calculated from internal power dissipation and external ambient temperature, would not reach the 5% fail-point in 10 years. Lowering the junction temperature to +70°C increases the time to 100 years.

A complete sequence of environmental tests on Series UDN6100A, including temperature cycle, pressure cooker, and biased humidity tests are continuously monitored to ensure that assembly and package technology remain within established limits.

These environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

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1) Manchester, K. E., and Bird, D. W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions,* Vol. CHMT-3, No. 4, 1980, pp. 580-587.

2) Peck, D. S., and Trapp, O. D., *Accelerated Testing Handbook,* Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid., p.* 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control,* 1961, pp. 208-213.

RELIABILITY DATA

SOT-23 TRANSISTORS

All transistor and diode device types are constantly monitored through ongoing mechanical and moisture tests. The reliability chart below shows typical data from moisture tests (pressure cooker and humidity life tests) and mechanical tests, including those for intermittent operating life and thermal shock. Solderability testing is performed on a regular sample basis. Individual process data is available on request.

Test	MIL-S-750 Method	Test Conditions	Unit Hours	Number of Failures	Failure Rate in FITs[1, 2]	MTBF[1, 2] (hours)
High-Temperature Storage	1031.4	T_A = +150°C 1000 hours	4.42×10^6	4	1187	8.42×10^5
Steady-State Operating Life	1026.3	T_A = +25°C 1000 hours P_D = 350 mW $V_{CB} = 0.8\ V_{(BR)CEO}$	5.23×10^6	5	1205	8.30×10^5
High-Temperature Reverse Bias		T_A = +125°C 1000 hours $V_{CB} = 0.8\ V_{(BR)CEO}$	8.10×10^6	12	1680	5.95×10^5
Thermal Shock		MIL-STD-202 Method 107 Condition F	1.98×10^6	3	2117	4.72×10^5
Pressure Cooker		15 psig T_A = +115°C 96 hours	5.57×10^5	3	7511	1.33×10^5
Humidity Life Test		T_A = +85°C Rel. Hmd. = 85%	5.03×10^6	3	831	1.20×10^6
Intermittent Operating Life	1036	T_A = +25°C 1000 hours P_D = 350 mW $V_{CB} = 0.8\ V_{(BR)CEO}$ t_{on} = 120 s t_{off} = 120 s	3.81×10^6	2	817	1.22×10^6

NOTES: 1. For confidence level of 60%.
2. Cumulative rate (includes infant mortals).

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PACKAGE INFORMATION

PACKAGE THERMAL CHARACTERISTICS

Allegro Package Code	Package Type (Common Package Designators)	Qty-Type of Terminals	$R_{\theta JA}$ (°C/W)	$R_{\theta JC}$ (°C/W)
A	Plastic Dual In-Line (DIP or PDIP)	14-Pin	60	38
		16-Pin	60	38
		18-Pin	55	25
		20-Pin	55	25
		22-Pin	50	21
		28-Pin	45	16
		40-Pin	36	—
B	Semi-Tab Plastic Dual In-Line (DIP or PDIP)	8-Pin	60	6.0*
		14-Pin	45	6.0*
		16-Pin	43	6.0*
		22-Pin	40	6.0*
		24-Pin	40	6.0*
EA	Semi-Tab Plastic Leaded Chip Carrier (PLCC or PQCC)	28-J Lead	50	6.0*
		44-J Lead	—	6.0*
EB	Semi-Tab Plastic Leaded Chip Carrier (PLCC or PQCC)	28-J Lead	42	6.0*
		44-J Lead	30	6.0*
EK	Square Hermetic Leadless Chip Carrier (LCC, CCC, or CQCC)	20-Contact	110	14-19
		28-Contact	100	10-19
		44-Contact	—	8.0-19
EP	Square Plastic Leaded Chip Carrier (PLCC or PQCC)	20-J Lead	70	35
		28-J Lead	55	30
		44-J Lead	46	25
H	Hermetic Side-Brazed DIP (H-DIP or CDIP)	8-Pin	120	40
		14-Pin	46	20
		16-Pin	46	20
		18-Pin	44	20
		22-Pin	40	20
K	Plastic Single In-Line (SIP or PSIP)	4-Lead	177	—
L	Plastic Small-Outline Transistor (SO or SOT)	3-Gull Wing	575	—
L	Plastic Small-Outline IC (SO, SOIC, or SOL)	8-Gull Wing	108	45
		14-Gull Wing	95	33
		16-Gull Wing	90	32

The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods. Where differences exist, the detail specification takes precedence.

Continued next page...

* $R_{\theta JT}$

PACKAGE THERMAL CHARACTERISTICS

Allegro Package Code	Package Type (Common Package Designators)	Qty-Type of Terminals	$R_{\theta JA}$ (°C/W)	$R_{\theta JC}$ (°C/W)
LB	Semi-Tab Plastic Small-Outline IC (SO, SOIC, or SOL)	20-Gull Wing 24-Gull Wing	60 50	6.0* 6.0*
LW	Wide-Body Plastic Small-Outline IC (SO, SOIC, or SOL)	16-Gull Wing 18-Gull Wing 20-Gull Wing 28-Gull Wing	80 80 70 66	— — 17 —
M	Mini Plastic Dual In-Line (DIP or PDIP)	8-Pin	87	55
R	Hermetic Ceramic Dual In-Line (CerDIP or GDIP)	14-Pin 16-Pin 18-Pin 28-Pin	57 57 55 50	30 30 30 —
V	Hermetic Metal Flange-Mount (FM or MBFM)	15-Pin	45	2.0*
W	Power-Tab Plastic Single In-Line (SIP)	12-Lead	36	2.0*
Y	Plastic Transistor	3-Lead	200	—
Z	Power-Tab Plastic Single In-Line (SIP)	3-Lead 5-Lead	67 65	3.0* 3.0*

The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods. Where differences exist, the detail specification takes precedence.

* $R_{\theta JT}$

PACKAGE INFORMATION

THERMAL DESIGN FOR PLASTIC INTEGRATED CIRCUITS

Proper thermal design is essential for reliable operation of many electronic circuits. Under severe thermal stress, leakage currents increase, materials decompose, and components drift in value or fail. Present-day linear integrated circuits are capable of delivering 5 to 10 watts of continuous power. Previously, such power levels came only with discrete metal can power transistors. It was relatively easy to determine the thermal resistance of these devices and attach a massive heat sink. However, in many markets, economic factors now dictate the use of molded dual in-line plastic packaged monolithic circuits. The guidelines to be discussed will provide the circuit design engineer with information on maintaining junction temperature below a safe limit under worst case conditions.

DESIGN CONSIDERATIONS

Four factors must be considered before the required heat-sinking can be determined. These are:

1. Maximum ambient temperature
2. Maximum allowable chip temperature
3. Junction-to-ambient thermal resistance
4. Continuous chip power dissipation

Maximum ambient temperature for the integrated circuit is normally between +70°C and +85°C and is usually dependent on the case material. In most applications, however, the limiting factor is the associated discrete components and a limit of about +50°C is specified. The maximum allowable chip temperature is usually +150°C for silicon.

Thermal resistance is the all-important design factor. It is composed of several individual elements, some of which are determined by the integrated circuits manufacturer, and some by the user.

CHIP POWER DISSIPATION

The chip power dissipation should be obtainable from the manufacturer's specifications. In most applications it is a variable and determined by the user when he specifies the circuit variables.

HEAT DISSIPATION

In any circuit involving power, a major design objective is to reduce the temperature of the components in order to improve reliability, reduce cost, or improve operation. The logical place to start is with the heat-producing component itself. First, keep the amount of heat generated to a minimum. Second, get rid of the heat that must be generated.

Heat generation can be minimized through proper circuit design. Heat dissipation is a function of thermal resistance.

With the typical discrete component, heat dissipation can be accomplished by fastening it directly to the chassis. Dual in-line plastic packaged integrated circuits, however, are quite a bit different. Their shape is not conducive to fastening directly to the chassis, they are

THERMAL DESIGN FOR PLASTIC ICs

normally installed in a plastic socket or on a printed wiring board, and the heat producing chip is not readily accessible.

Some users specify unusual packages so as to get the heat sink as close as possible to the chip and/or provide an attachment point for an external heat sink. A common factor in many of these special designs is that the lead frame is an integral part of the heat sink.

Since the plastic package may have a thermal resistance of between 50 and 100°C/W and the lead frame a thermal resistance of only 10 to 20°C/W, this would seem like the best route to go.

STANDARD PACKAGES

The most common lead frame material has been Kovar (an iron-nickel-cobalt alloy). Its coefficient of expansion is close to that of silicon thereby minimizing mechanical stresses. However, Kovar has a relatively high thermal resistance and consequently is not suitable for standard lead frames in high power dissipation circuits. For these applications, copper or copper-alloy lead frames should be used. Additionally, some type of added heat sinking may be necessary. Thus lead frame configurations are being altered from the standard 14-pin or 16-pin designs.

Rapidly becoming an industry standard is the "bat-wing" package. This package is the same size as a dual in-line package, but the center portion of the frame is left as tabs. These tabs can be soldered to a heat sink or inserted directly into a socket. The worst case thermal resistance of various lead frames ($R_{\theta JC}$) is given below.

Lead Frame	Thermal Resistance
14-pin Kovar	47°C/W
14-pin copper	38°C/W
"Bat-wing"	13°C/W

WHICH HEAT SINK?

If the integrated circuit manufacturer has done his job well, the chip-to-ambient thermal resistance wil be minimized for maximum chip power dissipation. It would appear that even the Kovar lead frame would be adequate for most applications. However, the total thermal resistance ($R_{\theta JA}$) is also dependent on a stagnant layer of air at the lead frame-ambient interface which will suport a temperature gradient. The total thermal resistance of a non-heat sinked dual in-line plastic package is therefore much higher. Since air is a natural thermal insulator, maximum heat transfer is through convection and the total thermal resistance will decrease some at high power levels.

Lead Frame	Total Thermal Resistance	Max. Power Diss. (W) at 50°C T_A, 150°C T_J
14-Pin Kovar	120°C/W	0.83
14-Pin Copper	60°C/W	1.67
"Bat-Wing"	45°C/W	2.22

Ignoring any safety margin and device performance, even the "bat-wing" is now only barely adequate for many power driver applications. The obvious solution is the use of an external heat sink.

Actual performance in a specific situation depends on factors such as the proximity of objects interfering with air flow, heat radiated or convected from other components, atmospheric pressure, and humidity. A good safety factor is therefore in order.

Heat sinks for plastic dual in-line packages can be of almost unlimited variety in design, material, and finish. Economics will normally play a very important role in the selection of any heat sink.

The least expensive and easiest to fabricate heat sink is the plain copper sheet. It is also very effective in reducing the total thermal resistance. The necessary dimensions can be obtained from Figure 1. These heat sinks are square in geometry, 0.015 inches thick, mounted vertically on each side of the lead frame, and with a dull or painted surface (Figure 2). The heat sinks should be soldered directly to the lead frame (approximately 0.3°C/W interface thermal resistance)

The plain copper sheet heat sink is also available commercially and may be less expensive than in-house manufacture. Two standard types are the Staver V7 and V8.

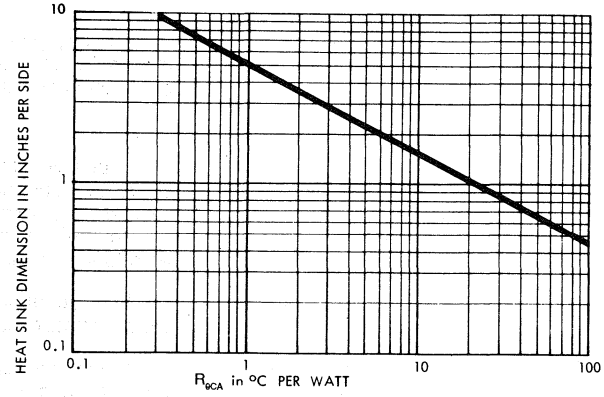

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FIGURE 1

THERMAL DESIGN FOR PLASTIC ICs

HEAT SINK FINISHES

The most common finish is probably black anodizing. It is economical and offers a good appearance. The black finish will also increase the performance of the heat sink, due to radiation, by as much as 25%. However, since anodizing is an electrical and thermal insulator, the heat sink should have an area free of anodize where the heat-generating device is attached.

Other popular finishes for heat sinks are irridite and chromic acid dips. They are economical and have negligible thermal and electrical resistances. These finishes, however, do not enjoy the 25% increase in performance that a dull black finish has.

FORCED AIR COOLING

The performance of many heat sinks can be increased by as much as 100% by forcing air over the fins. Where space is a problem, the cost of a small fan can often be justified. If a fan is required for other purposes, it is advantageous to place the semiconductor heat source in the air flow. A rule-of-thumb is that semiconductor failure rate is halved for each 10°C reduction in junction operating temperature.

CHIP DESIGN

Proper thermal design by the integrated circuit user can reduce the operating temperature of the semiconductor junction. However, the minimum chip temperature at any power level is determined solely by the device manufacturer. For this reason, care must be taken in choosing the manufacturer. "Exact equivalent" integrated circuits are not necessarily identical. Electrically and mechanically they may be the same, but thermal differences can mean that "identical" audio power amplifiers will not put out the same power without exceeding the rated junction temperature.

The circuit manufacturer must optimize his chip design so that component drift is minimized and/or equalized so that rated performance can actually be obtained under maximum thermal stress.

Note in Figures 3 and 4 that the Darlington input differential pairs are cross-connected so as to minimize differences in gain as a function of output transistor power dissipation. Transistor Q_4, being closest to

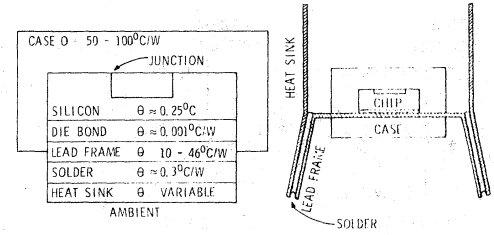

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FIGURE 2

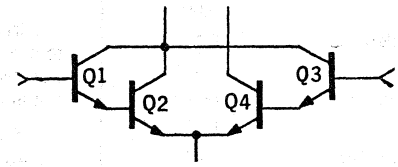

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FIGURE 3

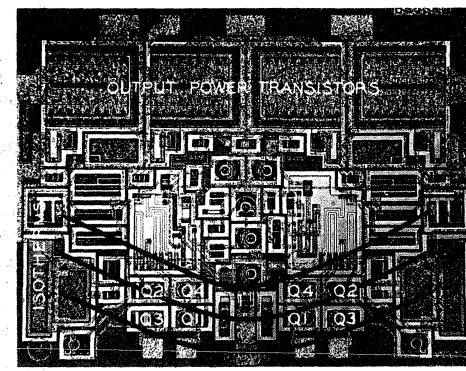

FIGURE 4

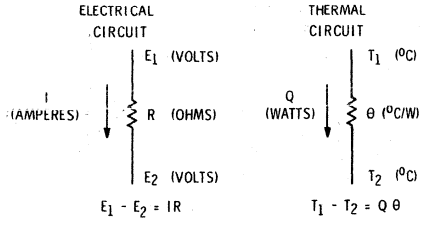

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FIGURE 5

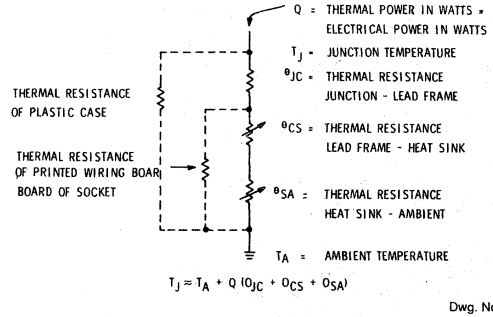

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FIGURE 6

Material	Thermal Resistance in °C/W for Unit Area/Unit Length
Silver	0.09
Copper, Annealed	0.10
Gold	0.12
Beryllia Ceramic	0.20
Aluminum	0.20
Brass (66 Cu, 34 Zn)	0.40
Silicon	0.50
Germanium	0.70
Steel, SAE 1045	0.80
Solder (60 Sn, 40 Pb)	1.5
Alumina Ceramic	2.0
Kovar (54 Fe, 29 Ni, 17 Co)	3.0
Glass	40
Epoxy	40
Mica	50
Teflon PTFE	200
Air	2000

the output power transistors, is naturally the hottest; Q_3 is a degree or two cooler; Q_1 and Q_2 are about equal and midway between Q_3 and Q_4. The gain of the Q_1-Q_2 Darlington pair is about equal to the gain of Q_3-Q_4 at all output power levels because of careful thermal design.

In certain specialized applications, thermal coupling can be used to a distinct advantage. Experimentally, thermal coupling has been used to provide a low-pass feedback network which otherwise could be obtained only with very large values of capacitance.

The foregoing discussion has covered the average thermal characteristics of dual in-line plastic integrated circuits. The specific devices will vary with the different packages and bonding techniques employed, but the concepts will remain the same.

APPENDIX

The following is intended to review terminology and compare thermal circuits with the more familiar electrical quantities.

The first law of thermodynamics states that energy cannot be created or destroyed but can be converted from one form to another. The second law of thermodynamics states that energy transfer will occur only in the direction of lower energy. In the semiconductor junction, the electrical energy is converted to thermal energy. Since no heat will be stored at the junction, the heat will flow to a lower temperature medium, air. The rate of heat flow is dependent on the resistance to that flow and the temperature difference between the source and the sink.

This thermal electrical analogy is convenient only for conduction problems where heat flow and temperature obey linear equations. The analogy becomes much more complex for situations involving heat flow by convection and radiation. Where these two modes are not negligible, they can be approximated by an equivalent thermal resistance. If ignored, the error introduced will only improve the device reliability.

A simplified thermal flow diagram of a molded dual in-line package and heat sink is shown. The thermal resistance of the lead frame-heat sink-ambient is shown as a variable resistor, because this is under the control of the user and may be varied over a considerable range.

APPLICATIONS INFORMATION

HIGH-PERFORMANCE POWER PACKAGE FOR POWER-INTEGRATED CIRCUIT DEVICES

ABSTRACT

A new, high-performance version of a Plastic Dual-In-Line package with improved reliability levels has been developed for high-power integrated circuit industrial and automotive applications. Superior thermal capability and reliability performances have been achieved with no increase in manufacturing cost or change in package outline.

The development of this package is based on a package optimization approach. Development methodology and package characterization results will be outlined. Data for production lots of the package show a thermal performance improvement of up to 35 percent compared with currently available packages, without the aid of an external heat sink. Furthermore, qualification test results indicate that this new package has an excellent reliability performance and its long-term survival exceeds the industry standard requirements. An improvement by a factor of 4 in the resistance to device metal deformation and a factor of 7 in wire-bond thermal fatigue has been achieved as a result of reducing the shear and normal stresses inside the package by proper selection of a state-of-the-art low modulus molding compound and optimizing the leadframe design. In addition, new design fundamentals will be briefly discussed.

This paper was presented at the 39th Electronic Components Conference, Houston, TX, May 22-24, 1989.

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INTRODUCTION

As the maturation of power integrated circuit technologies continues to promise more miniaturization of power electronic systems, the role of package thermal management is becoming critical. Since the present power packaging technology lags sharply behind the chip technology, the device performance and its reliable operation can be described to a great extent as limited by the package thermal capability. This paper presents the results of a package design study, which employs a "package optimization approach." The package chosen for this study is the 16-lead web-DIP, class of Plastic Dual-In-Line-Package (PDIP), which was specifically developed for medium- to high-power applications. An important practical feature of the web-DIP is that it costs no more to produce than a conventional DIP.

The initial phase of this program is a comparative analysis, based on package thermal and physical evaluations. Five variations of power DIP packages from major power integrated circuit manufacturers were evaluated. The evaluation results indicate that packages presently available are still far from optimum, thus making further improvements a feasible goal. In parallel to the comparative analysis, three-dimensional finite-element models are constructed to simulate and analyze the expected thermal performance of the design under study. The projected configuration is also analyzed thermostructurally to examine the mechanical behavior of the new packaging system, prior to implementation. The reliability improvement of the new package is based on optimization of the leadframe design, and the proper selection of materials. The package reliability design is aimed at improving wire fatigue life and device metal deformation resistance during temperature cycling. In addition, the study provides a new insight into this type of package and new design principles which can be extended to packages of similar internal configuration, such as power surface-mount packages.

OPTIMIZATION STRATEGY

PDIP's are still the most common package option for high-volume IC production, due to their established manufacturing and handling, and their low cost. However, there are two different types of PDIP's. The first is the standard type in which the chip pad is not attached to any of the internal leads (Fig. 1(a)), and which is mainly used for low-power applications. The second is a modified form of the standard type in which the central leads are tied in pairs and connected with the paddle, forming one piece (Fig. 1(b)). This unconventional configuration has been employed to improve the package thermal performance, mainly by enhancing the conduction heat transfer mechanisms by allowing the chip to be cooled directly by means of these four leads which are soldered to a board. This design format has made such a package suitable for medium-power applications up to 2.5 W in natural convection. Also, if the chip pad is extended to the outside of the package forming a web shape (Figure 1(c)), a miniature heat sink can be soldered to the web for even higher power dissipation.

HIGH-PERFORMANCE POWER PACKAGE FOR POWER-INTEGRATED CIRCUIT DEVICES

WEB-DIP DESIGN

Although there are several extensive studies concerning thermal performance and reliability of standard PDIP's [1]-[4], there have been no similar efforts directed towards its web version. However, we felt that a new insight should be gained and established for the web-type package for the following reasons:

(1) The power dissipation capability of the package is greatly influenced by the web concept, which dramatically changes the temperature fields inside the package. Consequently, all of the previously identified thermal paths for standard packages are affected, and their relative thermal contributions are altered.

(2) It has been demonstrated that converting from the standard package to the web-type package has led to an improvement of the package power handling capability by 70 percent. For example, a 1-W standard package can dissipate 1.7 W instead by tying its four central leads to the chip pad. However, our observations, as will be described later, indicate that some package designers have conflicting views about the thermal merits of the concept compared with other paths. This limited understanding as to the precise relationship between the web and other leadframe parameters has cost some manufacturers a great thermal penalty, as will be explained in the next section.

(3) The mechanical configuration of the leadframe and its physical behavior within the package during assembly, testing, and operation has introduced a considerable amount of uncertainty involving the package component structural responses and long-term reliability.

(4) Since this concept is being extended to new package families, notably PLCC's and SOIC's, to improve their thermal performance, new safe design limits are required, particularly when these packages have not been completely perfected.

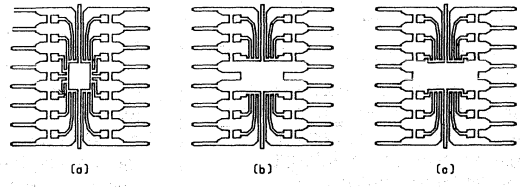

FIGURE 1

16-Lead PDIP leadframes (a) standard (b) unconventional (c) unconventional-web

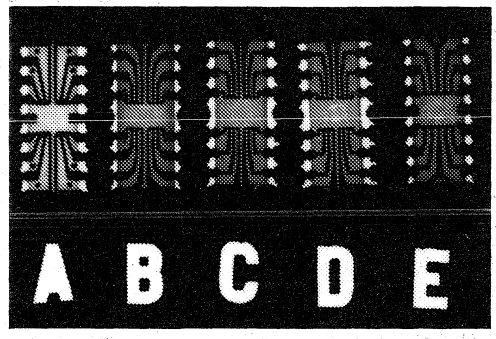

FIGURE 2

Leadframe designs for five different PDIP manufacturers

COMPARATIVE ANALYSIS

The primary purpose of this analysis was to assess the thermal performance of the industry state-of-the-art power DIP packages made by leading IC manufacturers. This performance evaluation enabled us to gain knowledge about the range of the thermal capabilities of existing packages and to establish an optimization target. Figure 2 shows the leadframe design of the examined packages.

Representative packages from five major companies including our targeted package were chosen for this study based on device performance equivalents and similarity of package outlines.

Steady-state thermal resistance of the packages was measured in still air under the same conditions at different power levels, using the Temperature Sensitive Parameters (TSP) method. During the measurements, packages were mounted individually by soldering to a printed circuit board which was oriented vertically and housed in a 1-ft.^{3} plexiglas sealed enclosure. Measurements were taken with the aid of a

TABLE I

16-LEAD DIP THERMAL RESISTANCE $R_{\theta JA}$ (°C/W)

Manufacturer	$R_{\theta JA}$ (°C/W) at 150°C T_J
A	47
B	51.5
C	52
D	55
E	59

Sage model Theta 400A thermal resistance tester. Results of the measurements of the thermal resistance from junction to ambient, $R_{\theta JA}$ are presented in Table I. The manufacturers are listed in ascending rank, based on their package performances.

The next step of the analysis was to correlate these thermal resistances to their packaging systems. For this purpose, a construction analysis was performed. The results of the construction examination are summarized in Table II. The material analysis has been performed with the aid of a SEM equipped with an EDAX analyzer. Although it is not the intent of this study to critique these packages, the following discussion is in order.

WORST PERFORMANCE

Manufacturer E, whose package shows the highest thermal resistance, uses a very high thermal conductivity leadframe material which is identified as "silver-bearing copper." Its conductivity is 35 percent higher than that of Copper Alloy C194, used by other manufacturers. One might therefore expect that the package thermal resistance, $R_{\theta JA}$, would be lower than that of other packages employing C194 leadframes. However, as is indicated in Table I, this is not the case. The main reason is that the leadframe design has left out the tie bar. As a result, a dramatic increase in $R_{\theta JA}$ occurs, which is not compensated for by the higher conductivity leadframe. To verify this, an experiment was run with packages assembled using copper alloy C151 leadframes, whose conductivity is 25 percent higher than that of C194 leadframes. The tie bar was removed from some of these packages. Thermal resistance measurements showed that in natural convection cooling the leadframe material and the tie bar make separate contributions to $R_{\theta JA}$. First, despite the substitution of C194 material by C151, only about a 2.5°C/W improvement in $R_{\theta JA}$ is gained. The reason for this is that the package external resistance, $R_{\theta CA}$ (where C refers to both the package and lead surfaces) is the pre-dominant resistance, and is more than 75 percent of the package total resistance in still air. This $R_{\theta CA}$ has less dependency on the leadframe material [4], and is mainly a function of the motion and temperature of the boundary layers that exist on the package and the external lead surfaces. Second, packages with tie bar show a 6°C/W improvement in $R_{\theta JA}$ over packages assembled without a tie bar. Therefore, we conclude that the leadframe thermal conductivity has a minor effect on $R_{\theta JA}$, while the tie bar has a greater influence. This is due to its multiplying effect on heat distribution within the package to the adjacent leads as well as heat spreading to both the top and bottom surfaces of the packages, resulting in an additive thermal enhancement by conduction and convection. The same effect was also verified analytically, as will be discussed later.

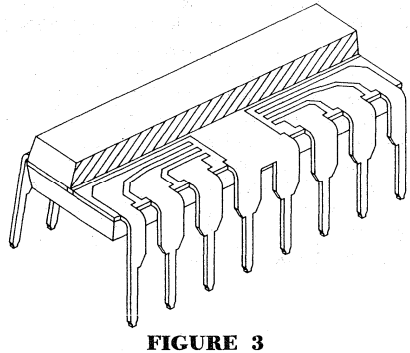

FIGURE 3

Web 16-lead PDIP

BEST PERFORMANCE

Manufacturer A, whose package exhibits the lowest thermal resistance shown in Table I, employed the same high-conductivity leadframe material used by manufacturer E, but did not remove the tie bar. In addition, manufacturer A increased the leadframe thickness to 15 mils from the standard 10 mils. To evaluate the impact of the leadframe thickness on the package power handling capability, packages assembled with C194 and C151 leadframes with 10-, 12-, and 15-mil thickness were evaluated. Results of thermal resistance measurements in still air are summarized as follows:

(1) $R_{\theta JA}$ for packages assembled with 10-mil C151 leadframes was 2.5°C/W lower than those assembled with 10-mil C194 leadframes.

(2) Packages assembled with 12- and 15-mil C151 leadframes showed an improvement in their $R_{\theta JA}$ by 3.5 and 7°C/W respectively over packages with 10-mil C151 leadframes.

Thus it is concluded that a thicker leadframe reduces the package heat spreading resistance and enhances the package surface thermal properties that result in improved thermal exchange between the package surfaces and their immediate surrounding air layers. As a result, $R_{\theta CA}$ is also reduced.

TABLE II

16-Lead DIP CONSTRUCTION ANALYSIS

Manufacturer	Leadframe Material	Leadframe Thickness (mm)	Chip Thickness (mm)	Die-Attach Material	Gold Wire Diameter (mm)	Leadframe Design (Refer to Fig. 1)
A	Silver-Bearing Copper	0.375	0.250	Solder	0.0375	(b)
B	Copper Alloy C-194	0.250	0.350	Silver Epoxy	0.0375	(c)
C	Copper Alloy C-194	0.250	0.450	Silver Epoxy	0.0375	(c)
D	Copper Alloy C-194	0.250	0.250	Silver Epoxy	0.375	(c)
E	Silver-Bearing Copper	0.250	0.350	Silver Epoxy	0.325	(b)

THERMAL MODELING

FINITE ELEMENT PROGRAM

In parallel to the comparative analysis, numerical solutions for a steady-state thermal model were obtained by using the finite element program, ANSYS. A three-dimensional (3-D) model for a typical web-16-lead package was first constructed as a reference model to simulate the thermal performance of a standard web-16-lead DIP for a typical package system. Parametric changes were then applied to the model to determine the best variable combinations which can be implemented to optimize the package power dissipation, while maintaining a constant junction temperature of 150°C. Major variables investigated in this study were:

1 - leadframe material
2 - leadframe thickness
3 - tie bar size and layout
4 - lead lock hole size
5 - leadframe design, (web design versus internal termination), see Figures 1(b) and (c)
6 - die attach material
7 - die pad area

MODELING PROCEDURES

A typical web-DIP is shown schematically in Figure 3. Due to symmetry, only half of the package was modeled, with an adiabatic boundary condition at the symmetry plane. The model consists of 3032 nodes and 2270 elements. A 3-D view of the model is shown in Figure 4. A steady-state thermal analysis with free convection cooling is assumed. For half of the package, a 1.2-W dissipated power was used to simulate a 150°C junction temperature. The power was assumed to be uniformly generated in a 0.025-mm-thick active layer at the top of the silicon chip. For half of the chip (1.5 mm x 3.38 mm), the power was specified as heat generation per unit volume (9.49 W/mm^3). The surfaces of the package and the external leads were assumed to have a convective heat transfer coefficient of 0.00001 W/mm^2°C. Table III shows the materials properties that were used in the analysis.

MODELING RESULTS AND DISCUSSION

Reference Model: The temperature distribution across the chip active layer is shown in Figure 5. The individual roles of the web and the tie bar in the package thermal performance are illustrated in Figure 6. It can be seen from Figure 6 that the web represents the primary thermal path in the transverse direction to the chip, where heat is directly conducted down through the chip pad out of the package to the connected protruding leads and dissipated into the board by conduction and to the air by convection and radiation. Also, it can be seen that the major remaining thermal barrier inside the package is the plastic layer between the chip edge and the lead tips, while the tie bar has a multiplying effect in dissipating and spreading heat to the adjacent leads and top and bottom surfaces of the package, as illustrated in Figures 6 and 7. Therefore, to achieve an effective thermal design, the plastic layer should be minimized and a massive tie bar utilized.

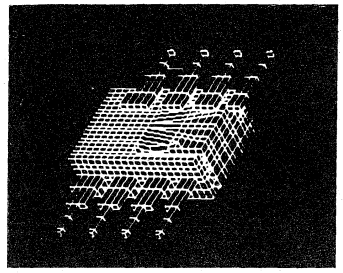

FIGURE 4

16-Lead DIP finite element model (3-D view)

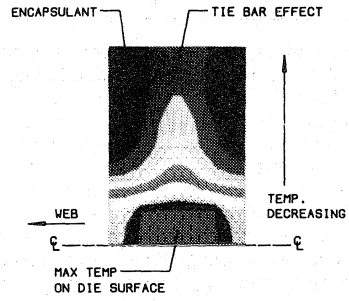

FIGURE 5

Temperature distribution on the die surface

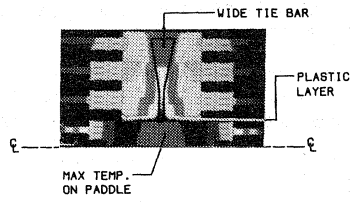

FIGURE 6

Temperature distribution across the leadframe surface

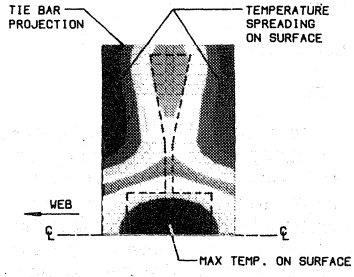

FIGURE 7

Temperature distribution on the package top surface

Parametric Study: For this analysis, the power generated in the active layer is held fixed and the junction temperature allowed to vary, while variables are applied. The results and conclusions of this parametric study are summarized as follows: (i) In natural convection cooling, for high-conductivity leadframe material, $R_{\theta JA}$ has a minor dependency on the material thermal conductivity. An increase in thermal conductivity of 25 percent yields an 8 percent decrease in $R_{\theta JA}$. The leadframe thickness is of somewhat greater influence, yielding a 10 percent decrease in $R_{\theta JA}$ for only a 20 percent increase in thickness. Both $R_{\theta JC}$ and $R_{\theta CA}$ are decreased, due to the massive size of the thicker frame and its effect of reducing the package internal resistance and improving the convection mechanism. (ii) The tie bar is critical to the package thermal performance even in the presence of the web feature because of its contribution in directing the heat flow throughout the package and disseminating heat to the package surfaces. Therefore, the package designer should not be tempted to remove it from the leadframe. (iii) Extending the chip pad outside the package has a thermal contribution. A 1.6°C/W increase in $R_{\theta JA}$ was found when the web had been removed and the paddle was terminated inside the package as in the case of package type in Figure 1 (b). (iv) Lead lock holes of 0.2 mm^2 each have no effect on the package thermal performance if they are placed on all the leads except the four central leads. (v) An improvement in $R_{\theta JA}$ of only 1.2°C/W was achieved by changing the die-attach material from epoxy to solder, despite the large difference in their conductivities. This is attributed to the very small thickness of this layer. (vi) For a given chip, $R_{\theta JA}$ is insensitive to the increase in the die pad area beyond a critical dimension, since any increase in the paddle area in the longitudinal direction is accompanied by moving the lead tips away from the chip edge which results in increasing the plastic thickness between the chip and the leads, thus, increasing lead resistance. Complete numerical data are summarized in Figure 8. The accuracy of these data is within 10 percent of the experimental results.

Based on these data, we have predicted that a potential improvement in the package thermal performance of 25 percent could be achieved over our targeted package. It is also estimated that the proposed package could achieve a 40 percent increase in power dissipation capability over the worst case. Consequently, we decided to develop a new leadframe to meet the absolute targeted thermal improvement with the following characteristics: (i) optimum configuration, (ii) higher thermal conductivity copper C151, and (iii) increased thickness, 0.375 mm compared to the standard 0.25 mm thickness. The reliability aspects of the new package are detailed in the reliability improvement and in the thermostructural modeling sections.

RELIABILITY IMPROVEMENT

Although the package thermal enhancement seems to be the principal driving force for this program, package reliability improvement has been an intrinsic part of the package optimization strategy. For example, two separate studies recommended the use of (i) a new epoxy die-attach adhesive for its effectiveness in reducing the amount of voids and improving the die shear resistance, and (ii) a new state-of-the-art low modulus molding compound which has proven its contribution in reducing the shear force on the die surface. Experimental results with the low-modulus molding compound showed a reduction in device

TABLE III

MATERIAL PROPERTIES OF 16 LEAD-PDIP PACKAGE COMPONENTS

Material	Thermal Conductivity (W/mm • °C)	Thermal Expansion Coefficient (10^{-6}/°C)	Poisson's Ratio	Young's Modulus (kg/mm²)
Molding compound	0.75×10^{-3}	19	0.30	15 000
Leadframe, C194	0.236	17	0.30	12 300
Silicon	0.140	2.4	0.28	17 000
Epoxy adhesive	0.004	20	0.30	6000
Leadframe, C151	0.331	17	0.30	12 300
Solder die attach	0.025	29	0.35	1800

metal deformation by a factor of 4, after temperature cycling from -65°C to 150°C. The low stress characteristics of this new molding compound result from lowering its Young's modulus, without sacrificing the glass transition temperature for the finished product. [5], [6].

MECHANISM OF GROUND WIRE BOND FATIGUE AND RELIEF

A novel leadframe design change has extended the fatigue life of grounding wires during temperature cycling by a factor of 7. Earlier temperature cycling tests had indicated the occurrence of a wedge bond (heel), failure of the grounding wire that is used for a large number of devices. The failure mode was identified as a rupture or fracture occurring at the heel of the bond located on the leadframe, particularly on the die pad periphery, as seen in Figure 9. Experimental observations indicated that the mechanism of the bond fatigue failure is plastic flow and rupture in the heel area induced by cumulative cyclic strain during thermal fluctuations. The identified failure mechanism can briefly be described as follows: (i) An excessive reduction in the heel cross-sectional area, accompanied by plastic deformation, is caused by the edge of the bonding tool. (ii) The bond knee, which represents the junction between the heel and the wire span, sustains high localized stress by virtue of stress concentration effects. (iii) This stress will be intensified by the superimposed molding stress. (iv) As the package undergoes temperature changes under temperature cycling conditions the heel is displaced. The displacement has both a horizontal and a vertical component. The horizontal component results from the shear force which is due to thermal coefficient mismatch between the molding compound and the leadframe, while the vertical component results from the molding compound normal stress. (v) Due to very low yield strength and high ductility of the gold wire, the displacement will produce a large amount of plastic strain, i.e., permanent deformation, at the knee for each temperature cycle. This plastic strain will accumulate during the course of the temperature cycling. (vi) In addition, during the high-temperature part of the cycle, a significant reduction in the gold yield strength could occur and the wire can behave as a perfectly plastic material [7] which will yield a very large cyclic strain at the knee and the molding compound interface. (vii) As the plastic straining continues and the cumulative magnitude of cyclic plastic strain reaches critical value (gold fracture strength), the heel will rupture at the knee and a fatigue crack can initiate, marking the beginning of the bond failure.

Analysis of experimental data suggested that the bond failure during temperature cycling is a function of heel strain. As a result, it was inferred that the bond fatigue life or number of cycles to failure can be expressed by the Coffin Law [8]

$$\Delta\epsilon_p = C/\sqrt{N}$$

where

$\Delta\epsilon_p$ = cumulative plastic strain

N = number of cycles to failure

C = constant.

Consequently, to improve the bond fatigue life, the heel cumulative plastic strain should be minimized during temperature cycling. Based on the discussion outlined above, the leadframe was designed to satisfy the plastic strain-number of cycles to failure criterion. The new leadframe design concept for reducing the cyclic strain, and in turn improving the bond fatigue life, is based on the following mechanical approaches which have been substantiated by reliability data and experimental verifications.

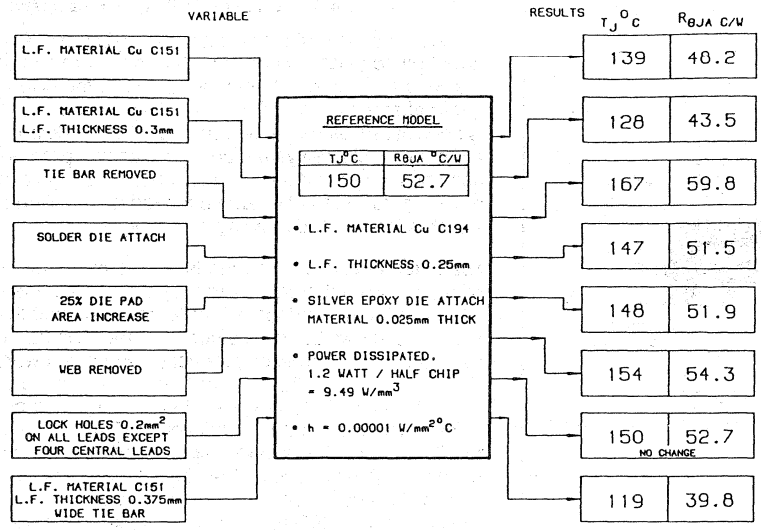

FIGURE 8

Numerical results of 3-D finite element analysis.

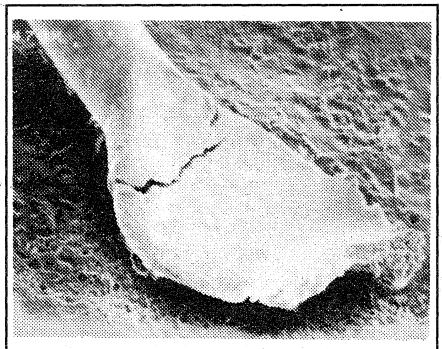

FIGURE 9

Wire heel damage after 1000 temperature cycles.

(1) Decreasing the area of the heel supportive, underlying pad of the leadframe would reduce the plastic strain amplitude. This is due to the reduced effect of the thermal coefficient mismatch between the leadframe and the molding compound.

(2) Reduction in the heel displacement can be achieved by minimizing the heel pad movement. Therefore, an improvement of the interfacial adhesion between the heel and the surrounding will reduce the pad displacement. Consequently, stresses transmitted to the heel-molding compound interface will be reduced.

(3) The fatigue damage accumulation of the heel is not only dependent on pre-mold stress [9], but mostly on the plastic straining effects resulting from mechanical interaction between the molding compound and the configuration of the underlying pad.

THERMOSTRUCTURAL ANALYSIS

Although the proposed leadframe posed an attractive option to augment the package power dissipation capability, its mechanical compatibility with other package components was considered to be the key factor for its final utilization for long-term reliable performance. Therefore, a thermostructural analysis study was performed to compare the structural behavior of the new package system, with the thicker C151 leadframe, versus the standard package, whose leadframe thickness is only 0.25 mm. Since the new leadframe material, C151, and the standard leadframe, C194, have the same elastic moduli and coefficients of thermal expansion, the only variable considered in the analysis is the thickness (see Table III).

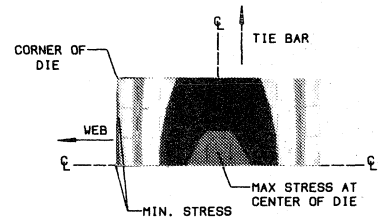

FIGURE 10

Die surface tensile stress distribution after die attach.

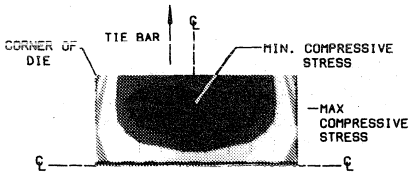

FIGURE 11

Die surface compressive stress distribution after die molding.

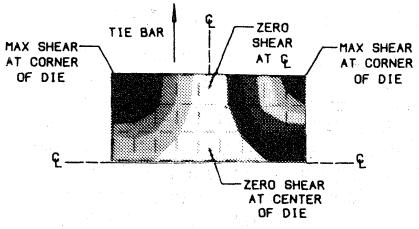

FIGURE 12

Die surface shear stress distribution after molding.

3-D FINITE ELEMENT MODELING

As the state of the shear and normal stresses on the die surface are of prime reliability concern, due to their role in device passivation cracking and metal deformation [10)-(12], they were analytically investigated after the die attach and molding processes. Only the web feature is considered, since the tie bar and other leads do not significantly affect the package system during these two processes. The following assumptions are made: (1) linear elastic analysis, (2) isotropic materials, (3) zero stress at or above the glass transition temperature of die attach adhesive and molding compound.

Die Attach Process: The modeling results show that for both assemblies, with two different leadframe thicknesses, the maximum normal stress on the die surface is tensile and occurs at the center of the chip. Figure 10 shows the tensile stress distribution on the die surface. It can be seen that the stresses gradually decrease towards the chip edges. Though the stress distributions on the die surface are identical in shape for both assemblies, they are different in magnitude. Assembly with the 0.25 mm thick leadframe produced 11.5 Kg/mm^2 while assembly with the 0.375 mm thick leadframe produced 10.0 Kg/mm^2. The model shows no shear stress on the die surface, which is expected since the surface is in pure bending. However, the chip maximum deflection at the center was 0.92/10^{-2} mm and 0.80 x 10^{-2}mm for thinner and thicker leadframes, respectively. This particular finding suggests that using a thicker leadframe in the assembly will produce lower die deflection which, in turn, can lead to a higher resistance to thermal cyclic fatigue during temperature changes that will be elaborated on later in reference to the thermal cyclic model.

Molding Process: Figure 11 shows the stress contours on the die surface at the end of the molding and cure process. Zero stress conditions were assumed at T_g = 155°C. The whole surface is seen to be under compressive stress, with maximum stress concentrated on the die edges parallel to the longitudinal axis and on the corners. The compressive stress distributions are similar for both assemblies but different in magnitude. Assembly with the 0.25 mm thick leadframe yielded 19.5 kg/mm^2 stress on the chip corners, while assembly with the 0.375 mm thick leadframe yielded only 16.5 kg/mm^2. A 15 percent reduction in stress on the chip corners is achieved by using a thicker leadframe in the package. In addition, the die surface shear stress is 12 percent lower for 0.375 mm thick leadframe. The shear stress distribution on the chip surface is the same for both assemblies. As shown in Figure 12, the maximum shear is concentrated on the chip corners and exponentially decreases to zero at the center of the die. [13]

In summary, these comparative results show that the 0.375 mm thick leadframe could be better than the 0.25 mm thick leadframe because (i) the permanent *in-situ* normal and shear stresses produced on the chip surface as a result of either the die attach or the molding processes are lower, (ii) the temperature dependence of the die surface stress is lower, and (iii) the maximum die deflection is also lower. These theoretical findings highlight the potential contribution that the leadframe thickness would have in reducing thermal-fatigue damage and vulnerability of the die to stress caused by temperature changes. To explain this, the following model is postulated.

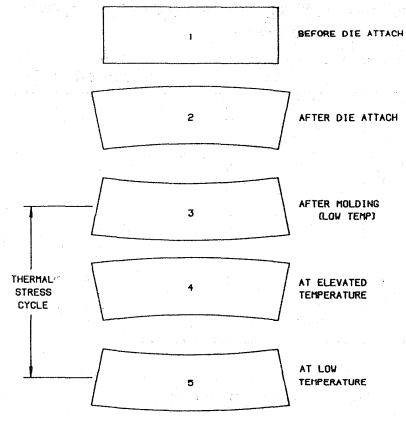

FIGURE 13

Die thermal stress fatigue model.

DIE THERMAL FATIGUE MODEL

At the beginning of the molding process, the die surface is completely under tensile stress, as depicted in Figure 13. At the end of the molding process, at room temperature, the stress reverses to a compressive stress If the package system is heated again to a higher temperature the compressive stress will reverse to a tensile stress. This reversible process is repeated whenever the package is exposed to temperature excursions, causing the die to deflect in a butterfly-like movement. [14] The reversible deflection is further aggravated by the effects of the superimposed shear force which eventually will lead to a combined vertical and horizontal thermal cyclic strain, particularly on the edges and corners of the die. Ultimately, microcracks will start to grow in the passivation layer. Subsequently, the device metal deformation will initiate.

Based on the analysis of the experimental and analytical results and the model proposed above, we inferred that a lower failure rate should be expected for package systems with thicker leadframes, since the cyclic die deflection and level of stresses will be lower during thermal stress transition. Therefore, less thermal fatigue effects will be induced on the surface of a die that is mounted on this thicker leadframe.

NEW PACKAGE EVOLUTION AND PERFORMANCE EVALUATION

Based upon the modeling predictions and the experimental evidence of thermal and reliability enhancement, the new package system was designed and placed into production. The features of the optimized package are described in Figure 14. Production lot samples of the newly developed package system were thermally characterized and exposed to an extensive reliability qualification study.

THERMAL CHARACTERIZATION

Production samples were thermally characterized under different ambient and cooling conditions. Results are summarized in Table IV. As shown in the table, two modes of cooling at room temperature were used during thermal characterization of the new package: natural convection, and moving air, both with and without a miniature heat sink. In still air at room temperature, the basic power dissipation capability of the new package without a heat sink is 3 W at T_J = 150°C. This represents a 25 and 35 percent improvement over the average and worst performances, respectively (see Table I). The comparison can be seen in Figure 15, which demonstrates the relationship between the thermal resistance and package power dissipation for the new package compared to packages discussed earlier. The boundary line in Figure 15 relates maximum power dissipation of the packages at T_J = 150°C, which is normally specified as the junction temperature safe limit for BiMOS silicon technology. The best absolute thermal improvement with the new package can be achieved in moving air with a heat sink mounted on its web. The maximum steady-state power capability then is 9.1 W.

TABLE IV

NEW PACKAGE SYSTEM THERMAL PERFORMANCE AT T_J = 150°C

No.	Test Conditions	$R_{\theta JA}$(°C/W)	Power Dissipated (W)
1	• Still air (room temp.) • No heat sink	41.6	3.05
2	• Still air (room temp.) • Heat sink (staver type)	24.8	5.1
3	• Moving air (200 LFM) • Room temperature • No heat sink	25.8	4.9
4	• Moving air (200 LFM) • Room temperature • Heat sink	13.9	9.10

QUALIFICATION TEST PROGRAM

The following were the qualification tests conducted:

1 - High-temperature reverse bias life test—150°C ambient at 50 V applied.
2 - Biased 85°C/85 percent RH test at 50 V applied.
3 - Pressure cooker—121°C, 100 percent RH.
4 - Extended temperature cycle, (-65°C + 150°C).
5 - Thermal resistance, $R_{\theta JA}$ after each interval of 500 temperature cycles.

No failures have been reported to date in any of the tests. Results are summarized in Table V.

SUMMARY AND CONCLUSIONS

A high-performance, unconventional 16-lead Plastic Dual-In-Line Package has been developed. The new package power dissipation capability is 25 percent higher than the average measured for available packages and 35 percent higher than the worst package. The long-term reliability performance of the new package exceeds present industry standard reliability requirements. Reliability data also show that the chip surface metal deformation resistance to temperature cycling is improved by a factor of 4, and the ground wire propensity for thermal cyclic fatigue damage has been reduced by a factor of 7.

The superiority of the package is due to a combination of an optimum leadframe design and proper choice of materials, such as a low-modulus molding compound. The development strategy was based on a package optimization approach, in which a comparative analysis indicated that existing packages are not fully optimized. Extensive thermal and thermostructural studies have been performed. The finite element results have provided an insight into both the thermal and structural performance of the package.

TABLE V

RELIABILITY QUALIFICATION RESULTS FOR NEW 16-LEAD DIP

No.	Test	No. of Hours or Cycles Completed	Sample Size	Number of Failures
1	150°C HTRB	6000 h	100	0
2	85°C/85 percent RH/Bias	6000 h	50	0
3	Temp. cycle - 65°C + 150°C "Electrical"	10 000 C	50	0
4	Temperature cycling, "Thermal resistance"	9000 C	12	0
5	Temperature cycling (ground wire fatigue life)	9000 C	50	0

ACKNOWLEDGEMENTS

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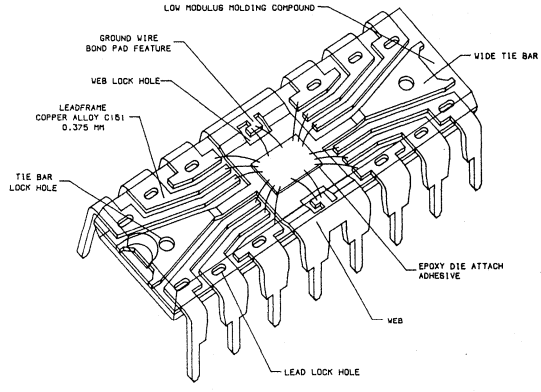

FIGURE 14

New web 16-lead PDIP.

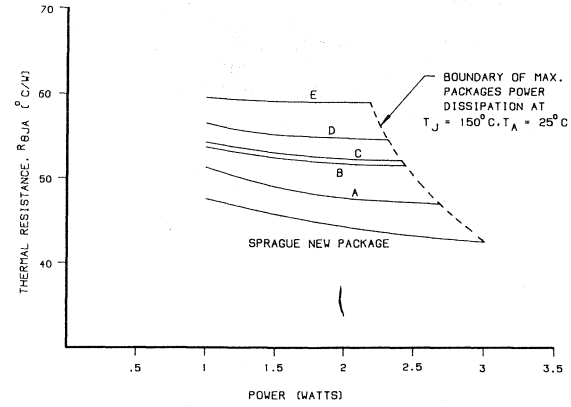

FIGURE 15

Thermal resistance versus power dissipation capability for various packages.

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APPLICATIONS INFORMATION

OPERATING AND HANDLING PRACTICES FOR MOS INTEGRATED CIRCUITS

MOUNTING POWER TAB DEVICES

Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. "Brute Force" mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

HANDLING PRACTICES— PACKAGED DEVICES

Input protection diodes are incorporated in all MOS/CMOS devices. However, because of the very high input resistance in MOS devices, the following practices should be observed for protection against high static electrical charges:

1. Device leads should be in contact with a conductive material except when being tested or in actual operation.
2. Conductive parts of tools, fixtures, soldering irons and handling equipment should be grounded.
3. Devices should not be inserted into or removed from test stations unless the power is off.
4. Neither should signals be applied to the inputs while the device power supply is in an off condition.
5. Unused input leads should be committed to either V_{SS}, V_{DD}, or ground

HANDLING PRACTICES—DIE

A conductive carrier should be used in order to avoid differences in voltage potential.

AUTOMATIC HANDLING EQUIPMENT

Grounding alone may not be sufficient and feed mechanisms should be insulated from the devices under test at the point where the devices are connected to the test equipment. Ionized air blowers can be of aid here and are available commercially. This method is very effective in eliminating static electricity problems.

AMBIENT CONDITIONS

Dry weather with accompanying low humidity tends to intensify the accumulation of static charges on any surface. In this atmosphere, proper handling procedures take on added importance. If necessary, steam injectors can be procured commercially.

ALERT FAILURE MODES

The common failure modes that appear when static energy exists and when proper handling practices are not used are:

1. Shorted input protection diodes.
2. Shorted or 'blown' open gates.
3. Open metal runs.

Simple diagnostic checks with curve tracers or similar equipment readily identifies the above failure modes.

APPLICATIONS INFORMATION

SURFACE-MOUNT IC PACKAGES

Significant benefits can be achieved through the use of surface-mounted devices (SMDs) and general surface-mount technology as it applies to all components, both active and passive. The major benefits are reduced size and weight, and improved system reliability through the reduction of printed wiring board holes. Improved quality and lower assembly cost are obtained through the adaptability of SMD to high-speed, pick-and-place assembly automation.

Prior dense circuit packing methods for active components used chip-and-wire hybrids or flatpacks. Hybrids have the disadvantages of yield limitations, specialized assembly requirements, and the difficulty of rework, burn-in, and testing at temperature or under operating conditions. The demand for flatpacks is decreasing with attendant increases in price. They are also prone to user damage in assembly.

Surface-mountable small-outline ICs and leaded or leadless chip carriers (SOIC, PLCC, and LCC, respectively) answer many of the limitations of flatpacks and chip-and-wire hybrids. In addition to the obvious benefits already described, due to the low mass of SMD, their ability to withstand shock and vibration is superior to conventional dual in-line packages (DIPs) and flatpack assemblies. SMD can also provide an improvement in electrical parameters (reduced wiring resistance, capacitance, and inductance) due to shorter signal paths and very dramatic improvements in the application of industry-standard DIPs.

Three types of surface-mount technology have been defined by the industry.

Type I: single- or double-sided board using only surface-mounted components. Space savings of 40% to 75% are achievable; lowest possible cost.

Type II or Mixed Technology: single- or double-sided board using a mixture of surface-mount and through-hole on the top side and possibly surface-mount on the bottom side. Space savings of 20% to 60% are typical; difficult to build with a single soldering process and typically requires two technologies; testing can be difficult and fixturing costly.

Type III: through-hole components on top side, surface-mount on bottom side. Space savings of 10% to 40% are typical; allows the use of existing equipment and technology for phasing in SMDs.

Another approach that facilitates phasing SMD into existing products is to design small Type I assemblies similar to ceramic hybrids. With small boards and few components, testing is easily accomplished using the interconnect pins. This construction is especially effective in utilizing the usually wasted vertical space of most printed wiring board assemblies.

Most SOICs feature gull-wing leads on two sides of the package, similar to the DIP configuration. Lead row spacing is 0.150" (part number suffix "L") for 8, 14, and 16-lead packages; 0.300" row spacing (suffix "LW") for 16, 18, and 20-lead packages. Wide body SOICs with

heat sink contact tabs (sufflx "LB") are used for increased package power dissipation requirements.

PLCCs (part number suffix "EP") are currently supplied in 20, 24, 28, and 44-lead square packages with J-formed leads. Extended temperature, hermetically sealed leadless chip carriers for military applications (suffix "EK" for square packages and "EL" for rectangular packages) are available in 18, 20, 24, 28, and 44-terminal configurations.

THERMAL CHARACTERISTICS

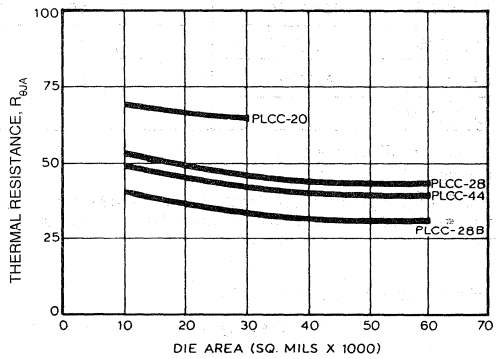
The thermal characteristics of power integrated circuit packages are often the limiting factor in circuit performance. IC packages for surface-mount application may be smaller, lighter, and more economical because of improved reliability and lower assembly cost, but they must still address the thermal problems in order to meet the circuit design requirements.

Regardless of package style (through-hole or surface-mount), the device junction temperature should be limited to +150°C.

The thermal resistance of surface-mounted ICs is increased due to the concentration of heat that results from the reduced package size. For packages with higher lead counts, this increase is minimized.

The printed wiring board on which SMDs are mounted is also very important in thermal management. Thermal resistance is affected less by convection or radiation and more by conduction into the mounting surface. Especially for LCCs, the application of a thermally conductive compound between the package bottom and the mounting surface will further reduce the thermal resistance.

For each surface-mount package type, worst-case thermal resistance is shown in the table on the next page. However, as shown in the curves here, thermal resistance is determined by both package style and chip dimensions. Differences in the data shown here and other industry data are due to the fact that the thermal resistance of these power packages is measured at worst-case junction temperatures at maximum power, making maximum use of convection, radiation, and conduction thermal paths.



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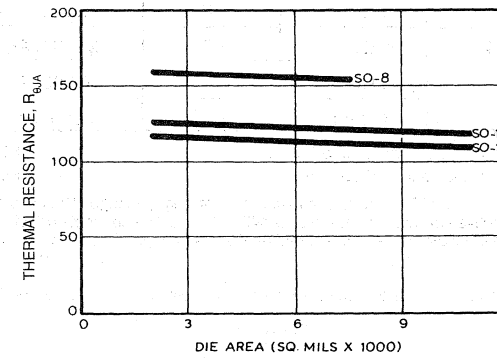

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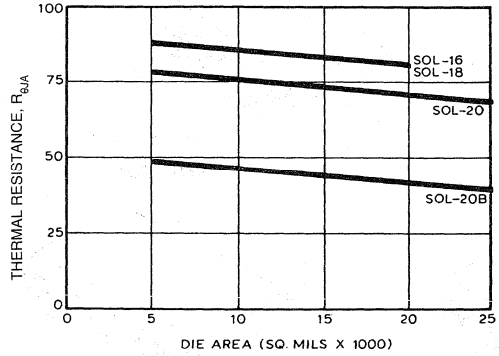

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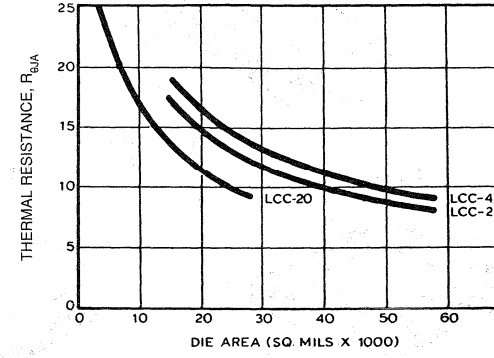

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Note: $R_{\theta JA}$ Measurements made with 2.24" x 2.24" solder-coated copper-clad board in still air.

SURFACE-MOUNT IC PACKAGES

Leads	Package Style	Package Suffix	Industry Package Outline	Thermal Resistance $R_{\theta JC}$[1]	Thermal Resistance $R_{\theta JA}$[2]	Tape and Reel Width x Pitch (mm)
8	SO-8	L	MS-012AA	45°C/W	155°C/W	12 x 8
14	SO-14	L	MS-012AB	29°C/W	118°C/W	16 x 8
16	SO-16	L	MS-012AC	27°C/W	110°C/W	16 x 8
	SOL-16	LW	MS-013AA	—	85°C/W	16 x 12
18	SOL-18	LW	MS-013AB	—	85°C/W	24 x 16
	LCC-18	EL	M38510/C-9	—	—	24 x 12
20	SOL-20	LW	MS-013AC	17°C/W	75°C/W	24 x 12
	SOL-20B	LB	MS-013AC	6°C/W*	45°C/W	24 x 12
	PLCC-20	EP	MO-047AA	35°C/W	70°C/W	16 x 12
	LCC-20	EK	M38510/C-2	14-19°C/W	110°C/W	16 x 12
28	PLCC-28	EP	MS-007AA	30°C/W	55°C/W	24 x 16
	PLCC-28B	EB	MS-007AA	6°C/W*	40°C/W	24 x 16
	LCC-28	EK	M38510/C-4	10-19°C/W	100°C/W	24 x 16
44	PLCC-44	EP	MS-007AB	25°C/W	50°C/W	32 x 44
	PLCC-44B	EB	MS-007AB	6°C/W*	30°C/W	32 x 44
	LCC-44	EK	M38510/C-5	8-19°C/W	—	32 x 44

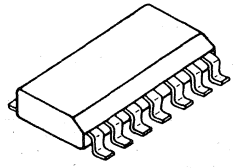
LCC = Hermetic Leadless Chip Carrier.
PLCC = Plastic Leaded Chip Carrier.
SO = Small Outline IC, 0.15" Gull Wing.
SOL = Small Outline IC, 0.30" Gull Wing.

*$R_{\theta JT}$. The SOL-20B package is a miniature "batwing" package (12 active connections plus eight tab/ground connections). The PLCC-28B is a batwing with 14 active connections; the PLCC-44B has 22 active connections. These unique power packages are compatible with other SMD packages and allow the easy attachment of external heat sinks for highest package power dissipation.

[1]Freon bath

[2]Mounted on 2.24" x 2.24" solder-coated copper-clad board in still-air for PLCCs & SOICs; unmounted in still air for LCCs.

SO-14



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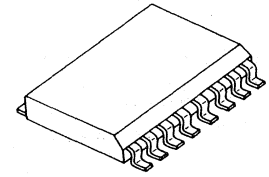
SOL-16



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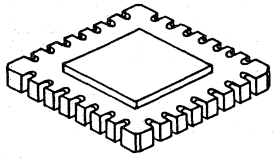
LCC-28



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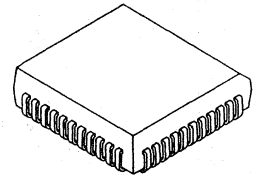
PLCC-44



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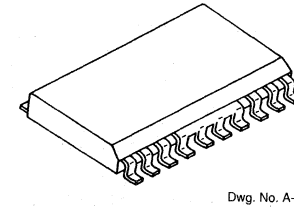
SOL-20B



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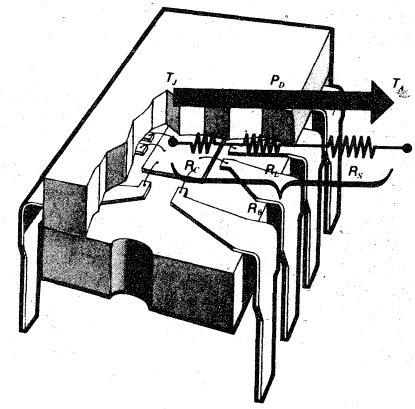
APPLICATIONS INFORMATION

COMPUTING IC TEMPERATURE RISE



IC temperature T_J is determined by ambient temperature T_A, heat dissipated P_D, and total thermal resistance R_θ. This total thermal resistance is comprised of three individual component resistances: chip R_C, lead frame R_L, and heat sink R_S.

WHY IC TEMPERATURES RISE

Heat is the enemy of integrated circuits—particularly power devices. Here's how to use thermal ratings to determine safe IC operation.

Excessive heat shortens the life of an IC and reduces its operating capability. Until recently, ICs were capable of operating only in low-power applications requiring perhaps a few milliwatts of power. But now, new ICs handle several amperes and drive devices such as relays, solenoids, stepping motors, and incandescent lamps. These high power levels may increase IC temperatures substantially and are capable of destroying devices unless appropriate precautions are taken.

THERMAL CHARACTERISTICS

The thermal characteristics of any IC are determined by four parameters. Maximum allowable IC chip junction temperature T_J and thermal resistance R_θ are specified by the IC manufacturer. Ambient temperature T_A and the power dissipation P_D are determined by the user. Equation 1 expresses the relation of these parameters.

$$T_J = T_A + P_D R_\theta \quad (1)$$

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COMPUTING IC TEMPERATURE RISE

Junction temperature T_J usually is limited to 150°C for silicon ICs. Devices may operate momentarily at slightly higher temperatures, but device life expectancy decreases exponentially for extended high temperature operation. Usually, the lower the junction operating temperature, the greater the anticipated life of the IC.

Ambient temperature T_A is traditionally limited either to 70°C or 85°C for plastic dual in-line packages (DIPs) or 125°C for hermetic devices. Again, the objective is to operate at as low a junction temperature as practical.

Thermal resistance R_θ is the basic thermal characteristic for ICs. It is usually expressed in terms of °C/W and represents the rise in junction temperature with a unit of power applied in still air. (The reciprocal of thermal resistance is thermal conductance, or derating factor, G_θ expressed as W/°C.) Thermal resistance of an IC consists of several distinct components, the sum of which is the specified thermal resistance. For a typical IC, these components of thermal resistance are 0.5°C/W per unit thickness of the silicon chip, 0.1 to 3°C/W per unit length of the lead frame, and up to 2,000°C/W per unit thickness of still air surrounding the IC. DIPs are used more than any other type of packaging for ICs and newer copper-alloy lead frames provide a superior thermal rating over the standard iron-nickel-cobalt alloy (Kovar) lead frames. However, power ICs are also available in other packages such as flatpacks and TO-type cans.

The power P_D that an IC can safely dissipate usually depends on the size of the IC chip and the type of packaging. Most common copper-frame DIPs can dissipate about 1.5 W, although some special-purpose types have ratings as high as 5 W.

Total IC power to be dissipated depends on input current, output current, voltage drop, and duty cycle. Thus, for many industrial digital-control ICs, logic-gate power P_I (typically less than 0.1 W) and output power P_0 must be determined to find the total power to be dissipated. Total power dissipation for these logic devices is the sum of P_I and P_0.

$$P_I = n(V_{CC}I_{CC}) \quad (2)$$

$$P_0 = n(V_{CE\,(SAT)}I_C) \quad (3)$$

where V_{CC} = logic-gate supply voltage, I_{CC} = logic-gate supply ON current, $V_{CE(SAT)}$ = output saturation voltage, I_C = output load current, and n = number of logic gates. Manufacturers usually list typical and maximum values for these voltages and currents. For thermal considerations it is best to use the maximum values so that worst-case power dissipation is determined.

If the duty cycle of the device is longer than 0.5 s, the peak power dissipation is the sum of the logic-gate power P_I and output power P_0 for the logic ON state alone. If the ON time is less than 0.5 s, however, average power dissipation must be calculated from instantaneous ON and OFF power P_{ON} and P_{OFF} from

$$P_D = DP_{ON} + (1\text{-}D)\,P_{OFF} \quad (4)$$

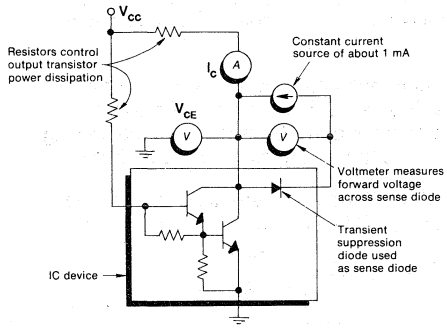
CORRECTIVE ACTIONS

If the junction temperature or the required power dissipation of the IC is calculated to be greater than the maximum values specified by the manufacturer, device reliability and operating characteristics possibly will be reduced. Possible solutions are:

1. Modify or partition the circuit design so the IC is not required to dissipate as much power.
2. Reduce the thermal resistance of the IC by using a heat sink or forced-air cooling.
3. Reduce the ambient temperature by moving heat-producing components such as transformers and resistors away from the IC.
4. Specify a different IC with improved thermal or electrical characteristics (if available).

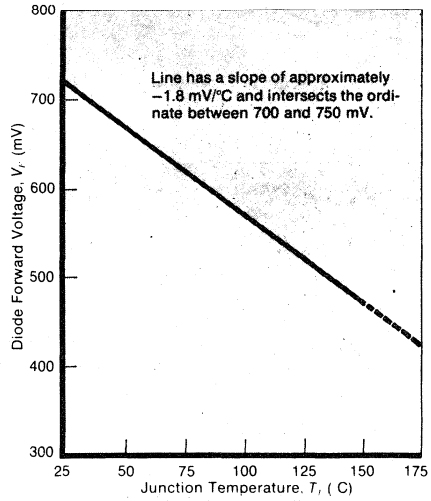
COMPUTING IC TEMPERATURE RISE

SETTING UP THE CIRCUIT



Input power is negligible compared to output power and is therefore not measured.

CALIBRATING THE SENSE DIODE



MEASURING IC TEMPERATURE

Sometimes IC junction temperature cannot be calculated readily and instead must be measured. Measurement should be made when there is insufficient data with which to calculate, when the effects of external variables such as forced-air cooling or enclosure size must be determined, or as a check on the manufacturer's specifications regarding package thermal resistance.

The most popular technique of measuring IC temperature uses the characteristic of a diode to reduce its forward voltage with temperature. Many IC chips have some sort of accessible diode—parasitic, input protection, base-emitter junction, or output clamp. With this technique, a "sense" diode is calibrated so that forward voltage is a direct indicator of diode junction temperature. Then, current is applied to some other component on the chip to simulate operating conditions and to produce a temperature rise. Since the thermal resistance of the silicon chip is low, the temperature of the sense diode is assumed to be the same as the rest of the monolithic chip.

The sense diode should be calibrated over at least the expected junction operating temperature. Apply an accurately measured, low current of about 1 mA through the sense diode and measure the forward voltage in 25°C increments after stabilization at each temperature. This calibration provides enough data for at least six points to construct a diode-forward-voltage versus junction-temperature graph at the specified forward current. A typical 25°C forward voltage is between 600 and 750 mV and decreases 1.6 to 2.0 mV/°C.

For power levels above 2 W, it may be necessary to use more than a single transistor if only the device saturation voltage and sink current are used. When higher power is desired keep the output out of saturation.

Measuring the sense-diode forward voltage may require a considerable waiting period (10 to 15 minutes) for thermal equilibrium. In any event, at the instant of measurement, the heating power may have to be disconnected since erroneous readings may result from IR drop in circuit common leads. Various circuit connections (such as four-point Kelvin) may be arranged to reduce or eliminate this source of error.

The IC junction temperature can be determined by comparing the voltage measurement with the internal power source against the voltage measurement with the temperature chamber.

COMPUTING IC TEMPERATURE RISE

FINDING SAFE OPERATING LIMITS

Here's how to calculate the safe operating limits for an IC. The first two examples are simple calculations involving maximum allowable power and are straightforward. The third and fourth examples are more complex and involve logic power, output power, and duty cycle.

Problem: Determine the maximum allowable power dissipation that can be handled safely by a 16-lead Kovar DIP with an R_θ of 125°C/W in an ambient temperature of 70°C.

Solution: From Equation 1, the maximum allowable power dissipation P_D for this IC is

$$P_D = \frac{150°C - 70°C}{125°C/W}$$
$$= 0.64\ W$$

Problem: Determine the maximum allowable power dissipation that can be handled by a 14-lead copper DIP with a derating factor G_θ of 16.67 mW/°C in an ambient of 70°C.

Solution: Since the derating factor G_θ is the reciprocal of thermal resistance R_θ the maximum allowable power dissipation P_D, from Equation 1 is

$$P_D = (150°C - 70°C) \times (16.67\ mW/°C)$$
$$= 1.33\ W$$

Problem: Calculate the maximum junction temperature for a quad power driver with a thermal resistance of 60°C/W in an ambient of 70°C and which is controlling a 250 mA load on each of the four outputs.

Solution: To determine the maximum (worst case) junction temperature for this IC, the maximum total power dissipation must be determined from the data listed on the IC data sheet. The specifications are usually listed as typical and minimum or maximum values. It is important to use maximum voltage and current limits to insure an adequate design. Common maximum values for an industrial power driver are $V_{CC} = 5.25$ V, $I_{CC} = 25$ mA, and $V_{CE(SAT)} = 0.7$ V, and $I_C = 250$ mA. From Equations 2 and 3, worst case logic and output power dissipation are

$$P_I = 4\ (5.25\ V \times 25\ mA)$$
$$= 525\ mW$$

$$P_0 = 4\ (0.7\ V \times 250\ mA)$$
$$= 700\ mW$$

Thus, the total worst case power dissipation P_D is 525 mW plus 700 mW, or 1.225 W. From Equation 1, maximum junction temperature T_J is

$$T_J = 70°C + (1.225\ W) \times (16.67\ mW/°C)$$
$$= 143.5°C$$

Problem: Determine the acceptable duty cycle for a hermetic power driver with a thermal resistance of 100°C/W in an ambient of 85°C and which is controlling load currents of 250 mA on each of four outputs.

Solution: From Equation 1, the allowable average power dissipation P_D for this IC is

$$P_D = \frac{150°C - 85°C}{100°C/W}$$
$$= 0.65\ W$$

This means that there is 0.65 W limit on average power, but, not instantaneous power. If the duty cycle is low enough, and the ON time is not more than about 0.5 s, the average power dissipation can be considerably lower than the peak power. The ON, or peak power, is determined from the data sheet maximum values of V_{CC}, I_{CC}, and $V_{CE(SAT)}$ at the specified load current of 250 mA. From Equations 2 and 3, logic-gate power P_I and output power P_0 for the ON state are

$$P_I = 4\ (5.5\ V \times 26.5\ mA)$$
$$= 583\ mW$$

$$P_0 = 4\ (0.7\ V \times 250\ mA)$$
$$= 700\ mW$$

Instantaneous ON power P_{ON} is the sum of P_I and P_0 for the ON state, or 1.283 W. The OFF power is primarily the power dissipated by the logic in the OFF state, and is found by using the I_{CC} maximum rated current listed on the specification sheet. The power dissipated in the output stage can be calculated from the leakage current I_C and supply voltage V_{CE}. From Equations 2 and 3, logic-gate power P_I and output power P_0 for the OFF state are

$$P_I = 4\ (5.5\ V \times 7.5\ mA)$$
$$= 165\ mW$$

$$P_0 = 4\ (100\ V \times 0.1\ mA)$$
$$= 40\ mW$$

Instantaneous OFF power P_{OFF} is the sum of P_I and P_0 for the off state, or 205 mW. From equation 4, acceptable duty cycle D is

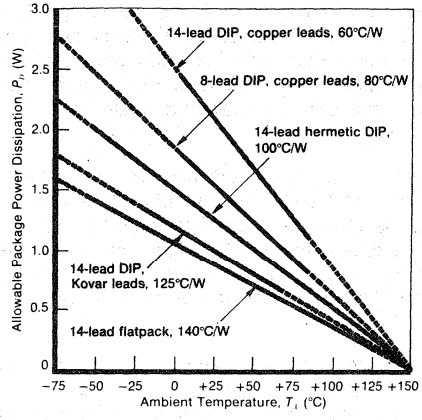
$$D = \frac{P_D - P_{OFF}}{P_{ON} - P_{OFF}}$$
$$= \frac{0.65\ W - 0.205\ W}{1.283\ W - 0.205\ W}$$
$$= 41\%$$

COMPUTING IC TEMPERATURE RISE

WHAT THE CURVES SHOW

The junction temperature of an IC depends on several factors, including the thermal resistance of the IC and the operating duty cycle. Graphs showing the relationship of these factors are often useful in specifying an IC.

Thermal Ratings

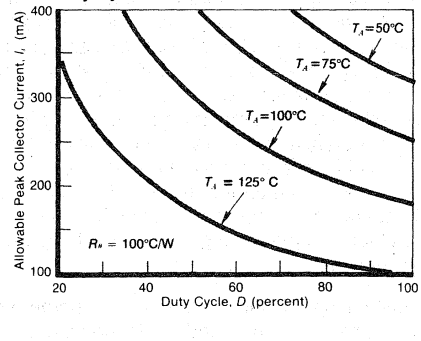


Typical thermal-resistance ratings for ICs in still air range from 60°C/W to 140°C/W. The slope of each curve on this graph is equal to the derating factor G_θ, which is the reciprocal of thermal resistance R_θ. For an ambient temperature of 50°C, a typical 14-lead flatpack with an R_θ of 140°C/W can dissipate about 0.7 W. A typical DIP, however, with 14 copper-alloy leads can dissipate almost 1.7 W at 50°C.

The highest allowable package power dissipation shown here is 2.5 W. Other special-purpose DIP packages are available with power dissipation ratings as high as 3.3 W at 0°C (R_θ = 45°C/W). If not for package limitations, IC chip dissipation might be greater than 9 W at an ambient temperature of up to 70°C.

Although the curve for plastic DIPs goes all the way to 150°C, they ordinarily are not used in ambients above 85°C because of traditional package limitations. Hermetic DIPs are specified to temperatures of 125°C, and at 150°C the device should be derated to 0 W. The higher specification limits for hermetic devices is the result of their design for use in rigorous, high-reliability military applications.

Duty Cycle



Duty cycle is important in calculating IC junction temperature because average power—not instantaneous power—is responsible for heating the IC. To convert from peak power to average power, multiply the peak power dissipation by the duty cycle. The average-power rating is then used with the thermal-resistance rating to calculate the IC junction temperature. Thus, short duty cycles allow peak power to be high without exceeding the 150°C junction-temperature limit. However, this consideration applies only to ON times of less than 0.5 s.

APPLICATIONS INFORMATION

THERMAL RESISTANCE— A RELIABILITY CONSIDERATION

More and more the semiconductor component supplier and the ultimate system user are becoming aware of the need for reliable components. Most failure mechanisms responsible for reliability failures are temperature dependent and the kinetics of the failure reaction are normally described by an Arrhenius function. This dependence, therefore, demands the capability of measuring the mean temperature which an integrated circuit die will attain during operation to realistically assess the reliability of the part.

The problem addressed by this paper is the inconsistency of the measurement techniques and the results used by manufacturers and users to determine the thermal characteristics of packaged semiconductor components. Our objective is to provide insight into the considerations which must be applied when evaluating these thermal properties of the packaged component. These considerations are materials, geometry and environment.

Furthermore, we wish to instill uniformity in the method of determining thermal properties of packaged semiconductors through understanding of the variables involved which can lead to a useable industry standard.

RELIABILITY—THE TEMPERATURE FUNCTION

The recognition of the problems one encounters in measuring the mean temperature of a die has been directly related to our experiences in our reliability assurance programs. The large number of device types manufactured require an equally large number of burn-in boards having different functions and geometry for the individual reliability studies. The variations in board density and thermal environment for a device under test have provided considerable junction temperature data from which we conclude that a "thermal resistance" measured in one oven with its set of conditions is not transferable to another oven with different boards, loading, etc. when the reference temperature for the measurement is the oven control temperature. Furthermore, it has become obvious that these same problems in measuring a mean die temperature exist in a system environment.

Most reactions which can cause a failure in an electrical parameter of an integrated circuit are chemical in nature and are influenced by temperature. The temperature dependence of these reactions has been described very well by S. Arrhenius in his treatment of reaction kinetics.[1] In his treatment, the reaction velocity or rate is given by the equation

$$d\ln V_r/dT = E/RT^2$$

where V_r is the specific reaction rate, T is the absolute temperature, R is the Molar Gas Constant, and E is the energy difference between a mole of active molecules and a mole of normal molecules.

THERMAL RESISTANCE— *A RELIABILITY CONSIDERATION*

This equation integrates to

$$\ln V_r = E/RT + A$$

where A is a constant which is the value of $\ln V_r$ at $1/T = 0$, $(\ln V_r)$. A more familiar expression is

$$\ln V_r = \ln V_r^\circ - \epsilon/kT$$

or

$$V_r = V_r^\circ e^{-\epsilon/kT}$$

where ϵ is the activation energy per molecule (= E/N), N = Avagado's number and k is the gas constant per molecule (= R/N), which is generally known as the Boltzmann constant. it has the value

$$8.6 \times 10^{-5}\ \text{eV/°K}.$$

V_E, the time rate of change of electrical parameters is proportional to V_r, i.e., $V_E = BV_r$. The amount of change in the electrical parameter necessary to cause a normal device to fail, ΔP_f, is $V_E t_f$ where t_f is the time of failure.

Recalling that $V_E = BV_r$, then

$$\Delta P_f = BV_r t_f$$

For a given device ΔP_f is a constant, therefore,

$$t_f = \Delta P_f B^{-1}/V_r$$

but

$$V_r = V_r^\circ e^{\epsilon/kT}$$

therefore

$$t_f = (B^{-1}\,\Delta P_f/V_r^\circ e^{\epsilon/kT}) = \beta e^{\epsilon/kT})$$

where

$$\beta = B^{-1}\Delta P_f/V_r^\circ$$

The acceleration factor ($\overline{AF}$) between any two temperatures is derived from this equation, when the activation energy for the failure reaction is known:

$$\overline{AF} = t_{f_1}/t_{f_2} = e^{\epsilon/k(1T_1 - 1/T_2)}$$

Activation energies of most reactions responsible for random failures in a normal operating period (beyond infant mortality) are nominally

(0.4 - 1.0) eV.

The importance of accurately determining the die temperature is now clear if one considers a not unrealistic situation where a device is thought to be operating with a die temperature of 120° and the actual temperature is 150°C. If the failure reaction has an activation energy of 0.7 eV, then the acceleration factor is 4.3 which means the device would fail in less than one quarter of the time it would have taken if the device actually operated at 120°C .

THERMAL RESISTANCE — $R_{\theta JA}$

Quite frequently, applications engineers have made attempts to identify the temperature attained by a die when a steady state rate of heat is being generated by the die by applying the term called "Thermal Resistance." This "constant," designated $R_{\theta JA}$, or simply θ_{JA}, relates the temperature rise of a packaged integrated circuit die above an ambient temperature when a known constant power is generated in the die. This term is normally defined as

$$\theta_{JA} = (T_J - T_A)/P_D$$

where T_J is the mean junction or die temperature, T_A is an ambient temperature, and P_D is the power generated within the die which must be conducted from the die to the ambient. This is occasionally designated Q_T, the time rate of heat generation in the die. Thermal resistance data supplied by manufacturers may be referenced to a cubic foot of free or still air, flowing air at some velocity, or simply no reference. These are some of the definitions of "ambient" from which one must determine where to measure T_A.

Thermal resistance as defined by θ_{JA} is not constant. It is made up of a constant term (or terms) in series with a number of variable terms. The constant terms relate to the package materials and geometry, which we will designate θ_{JC}, and the variable terms relate to the heat paths from the package boundary to some isothermal envelope in the system which has the temperature T_A. Even if the system for measuring θ_{JA} is defined, it is virtually impossible to reproduce that system in an application since the external thermal paths are determined by the method of mounting, the printed wiring board if used, other heat generating components on the board or in the vicinity, air flow patterns, etc. These are all variables for each application. We have measured values of θ_{JA} for the same device which vary by a factor of two when the mounting and environmental conditions are changed. The values in the θ_{JA} column in Tables 2 and 3 are indicative of the variation.

One is tempted to partition θ_{JA} into two thermal terms,

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where θ_{JC} is defined as the thermal resistance from the source of power at T_J to the boundary of the package not including the external legs, and θ_{CA} is the thermal resistance from the package boundary to that isothermal envelope at T_A. However, when one examines the thermal profile along the surface of a plastic dual-in-line package such as shown in Figure 1, it is immediately obvious that a definition of θ_{JC}

$$\theta_{JC} = (T_J - T_C)/P_D$$

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A RELIABILITY CONSIDERATION

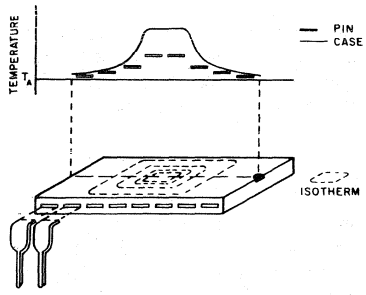


FIGURE 1

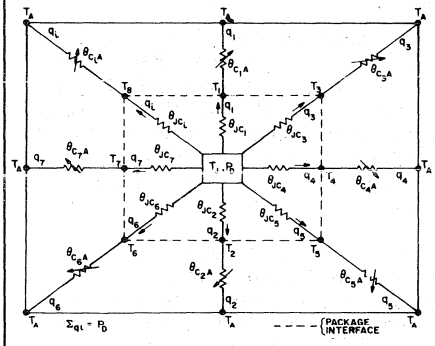


FIGURE 2

cannot be applied because T_C varies with position. Similarly, the term θ_{CA} defined by

$$\theta_{CA} = (T_C - T_A)/P_D$$

suffers from the same variablility in T_C. This being the case, it is invalid to partition θ_{JA} when operating on the *total* power to be dissipated, P_D.

THE THERMAL MODEL

When one examines a plastic package supplied by an individual manufacturer it is found that the geometry of the lead frame, its position within the package boundary, its composition, the composition of the plastic and its filler, the internal wire bonding are very carefully controlled and constant in time. This being the case one can readily build a model of the package which can be as invariant as the package material properties. If one considers all possible heat flows, a very complex model emerges. However, if the thermal conductivities of the package materials and the orders of magnitude difference in the values of these conductivities are considered, a simplified workable model can be generated by neglecting heat paths where heat flows are minimal. The simplified model shown in Figure 2 has ignored the heat flow between leads and assumes that the large difference between the thermal conductivity of the loaded plastic and the metals in the package define the specified heat paths. For example, the heat flow between leads would be a shunting resistor between heat paths in the model. The thermal conductivity of most plastics range between 1.5 and 3×10^{-3} calories/cm - °C while copper based materials range between 0.5 and 0.82 calories/cm - °C and nickel based alloys are about 0.03 calories/cm - °C.

The heat paths defined by θ_{JC_i}, where i refers to a particular path, radiate from the chip to an area on the package periphery defined by the projected chip or pad area as well as the mean cross-sectional area of each of the leads within the plastic package boundary (see Figure 1). Because of package symmetry, a 16-lead isolated-pad package may have seven different heat paths which can be characterized. The thermal resistance, θ_{JC_i}, can be calculated for each path from the geometry and material properties. For example θ_{JC_1} is the resistance from the top of the chip to the projected area on the package surface. The value of θ_{JC_1}, is given by

$$\theta_{JC_1} = (T_J - T_{C_i})/q_1 = L/K_pA$$

where L is the length of the heat path (thickness of the plastic above the die), A is the cross-sectional area of the heat path (area of the die or the pad), K_P is the thermal conductivity of the loaded plastic and q_1 is the heat/second flowing in the path defined by A and L.

θ_{JC_2} is the thermal resistance from the top of the die through the silicon, through the pad and through the plastic to the bottom surface. The value of θ_{JC_2} is given by

$$\theta_{JC_2} = (T_J - T_{C_2})/q_2 =$$
$$[1/A] \Sigma L_n/K_n$$

n = Si, Metal, Plastic

THERMAL RESISTANCE— *A RELIABILITY CONSIDERATION*

Similar expressions can be derived for each of the leads and they have the form

$$\theta_{JC_i} = (T_J - T_{C_i})/q_i =$$
$$[1/t]\,[(L/K_P W_P) + (1/K_M)\,\Sigma\, L_n/W_n]$$
$$n = 1, 2.....$$

where t is the thickness of the lead frame, K_p is the thermal conductivity of the loaded plastic, K_M is the thermal conductivity of the frame metal, L_n is the mean length of each connected portion of a leg segment having a mean width, W_n. In accord with the model, each internal path characterized by a thermal resistance, θ_{JC_i}, is in series with an external thermal resistance, θ_{C_iA}, which completes the path to T_A. The value of θ_{C_iA} can be calculated from the amount of heat, q_i, flowing through the internal package path and the temperature difference, $(T_{C_i} - T_A)$, with the equation

$$\theta_{C_iA} = (T_{C_i} - T_A)/q_i.$$

Values of θ_{C_iA} are variable and depend upon the specific environment.

We identify the heat paths in our calculations and data as follows: a) when i = 1, the path is from die to case surface directly above, b) when i = 2, the path is from die to the case surface directly below and c) when i = 3, 4, 5 . . . the path is from die through an identified metal lead to the intersection with the plastic surface.

VERIFICATION OF MODEL

From the model one can derive the minimum thermal resistance which is characteristic of the package. This can be calculated for the condition when all case temperatures are equal and at T_A. This is equivalent to shorting all external thermal resistances so that $T_{C_i} = T_A$. When all T_{C_i} are equal, the reciprocal of the sum of the reciprocals of all θ_{JC_i} is the minimum thermal resistance for the package. This is realized experimentally by placing the unit in an infinite heat sink such as a rapidly stirred, low-viscosity controlled temperature bath. The case temperature is now forced to be the same over all surfaces and by definition it is T_A. θ_{JC} is the minimum limit of θ_{JA}. Table 1 shows the agreement between the values of θ_{JC} calculated from the model when the case temperatures are shorted together and the values experimentally measured in a controlled temperature liquid bath. The agreement between calculated and experimental values for packages constructed from different materials enhance the validity of the model.

TABLE 1
COMPARISON OF CALCULATED AND EXPERIMENTAL VALUES OF $[\theta_{JC}]\ T_{C_i} = T_A$ (All measurements in °C/W)

Package Type	Frame Material	$[\theta_{JC}]\ T_C = T_A$	
		Experimental	Calculated
16-Pin, Isolated Pad, Epoxy I	Copper	41 ± 3	43
16-Pin, Isolated Pad, Epoxy I	Kovar	100 ± 4	93
16-Pin Tab	Copper	8.6 ± .7	8.5

APPLYING THE MODEL TO MEASURE T_J

Having verified the model, any one of the identified heat paths, which has a constant thermal resistance, θ_{JC_i}, can now be used to determine quite accurately the die temperature, T_J. If one chooses to measure the case temperature directly above the die, the difference between die temperature and case temperature is related to the heat flow, q_i, through that path by the thermal conductivity equation:

$$q_i = K_p A\,(T_J - T_{C_1})/L_1.$$

Rearranging this equation to

$$(T_J - T_{C_1})/q_1 = L_1/k_p A_1 = \theta_{JC_1}$$

Then

$$T_J = T_{C_1} + q_1\theta_{JC_1}$$

If the fraction of total heat, P_D, generated by the die which passes through path 1 is defined as k, then

$$q_1 = k_1 P_D$$

Substituting into the previous equation T_J is now referenced to T_{C_1} by

$$T_J = T_{C_1} + k_i\theta_{JC_1}P_D$$

where T_J, T_{C_1}, and P_D are experimentally measurable quantities. Values of $k_i\theta_{JC_1}$ can be determined. This term can be used to determine T_J in any environment by measuring T_{C_1} and the total heat generated by the die. This equation applies for any path, i, i.e.

$$T_J = T_{C_1} + k_i\theta_{JC_i}P_D$$

Experimental results are presented in Table 2 which establish that $k_i\theta_{JC_i}$ is a constant, the magnitude of which is determined by the heat path chosen.

THERMAL RESISTANCE—
A RELIABILITY CONSIDERATION

TABLE 2

THERMAL RESISTANCE VALUES—ISOLATED PAD—EPOXY PACKAGE (All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_4\theta_{C_4A}$	$k_1\theta_{C_1A}$	$k_1\theta_{JC_1}$	$k_4\theta_{JC_4}$
ULN2003A 16-Pin Copper Frame	1 ft.^{3} Still Air, Socket Mount	84.7	39.1	48.1	36.6	45.6
ULN2003A 16-Pin Copper Frame	Oven #1, 60 CFM, Pin Connectors	60.0	17.0	25.2	34.8	42.3
ULN2003A 16-Pin Copper Frame	AAVID E type 5010 Heat Sink Oven #1, 60 CFM	50.4	11.4	15.2	35.2	39
ULN2003A 16-Pin Copper Frame	Fluorocarbon Bath, Pin Connectors	41.3	3.3	2.9	38.4	38

TABLE 3

THERMAL RESISTANCE VALUES—TAB PAD—EPOXY (All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$K_5\theta_{C_5}A$	$K_5J_{C_5}$
Test Chip "B" Package	Oven #1, T_A = 50°, 60 CFM	32.8	25.0	7.8
ULN2068B	Oven #1, T_A = 50°, 60 CFM	34.9	26.4	8.5
ULN2068B	Socket Mount, FC-40 Bath	23.2	13.5	9.7
ULN2068B	Socket Mounted on Board, FC-40 Bath	26.8	17.4	9.4
Test Die "B" Package	Oven #1, Soldered on Test Board, 60 CFM	31.2	22.8	8.4
Test Die "B" Package	Oven #1, Soldered in Test Board w/Staver Heat Sink	22.3	14.2	8.1

In our notation, $k_4\theta_{JC_4}$ is the thermal resistance of the path determined by measuring the temperature of pin 4 at the point of intersection with the case body. Further data are presented in Table 3 for a copper tab package where the pad on which the die is mounted extends to the outside of the package. The values of $k_5\theta_{JC_5}$ remain constant over a large change in environment. When i = 5, the heat path is from the die through the heat tab to the intersection with the case surface.

Figure 3 shows the outline of the frame in the 16-pin isolated-pad package which is designated the "A" package. The "B" package or tab package frame outline is also shown.

MEASUREMENT OF $k_i\theta_{JC_i}$

Although the derived equations indicate that $k_i\theta_{JC_i}$ are determined by two temperature measurements at one power level, the values are more accurately determined from temperature versus power plots.

THERMAL RESISTANCE— *A RELIABILITY CONSIDERATION*

If one considers any one path, i, in the model, that path is described by:

$$T_J - T_A = q_i (\theta_{JC_i} + \theta_{C_iA})$$

Here again, if k_i is the fraction of the total heat (P_D) which traverses path i, then the previous equation can be written

$$T_J - T_A = k_i P_D (\theta_{JC_i} + \theta_{C_iA})$$

or rearranging terms

$$(T_J - T_A)/P_D = k_i\theta_{JC_i} + k_i\theta_{C_iA}$$

By definition $(T_J - T_A)/P_D = \theta_{JA}$, therefore by subtitution and rearrangement

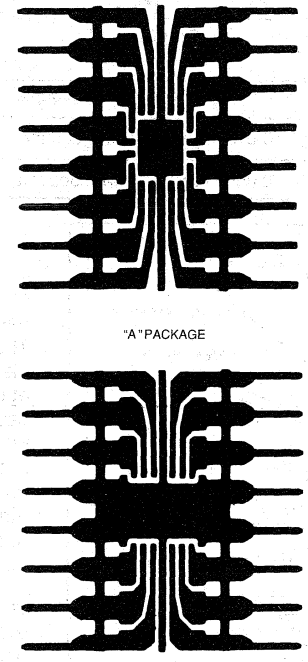
$$k_i\theta_{JC_i} = \theta_{JA} - k_i\theta_{C_iA}$$

where experimentally θ_{JA} is the slope of a plot of T_J versus P_D and $K_i\theta_{CA_i}$ is the slope of the plot of T_{C_i} versus P_D. Figures 4, 5, and 6 are representative of the experimental plots for evaluation of $k_i\theta_{JC_i}$.

T_{Ci} MEASUREMENT

The numerical values of $k_i\theta_{JC_i}$, which we have shown experimentally to be constant over a large variation in environmental conditions, are functions of the measuring system for determining the case or leg temperature, T_{C_i}. This can be shown by considering heat path 1 in the Model shown in Figure 2. In this case, $q_1 = (T_J - T_A)/(\theta_{JC_1} + \theta_{C_1A})$. θ_{JC_1} is defined as L_1/k_pA_1, where A_1 is determined by the die area. When a thermocouple is attached to the surface directly over the die, it also functions as a heat sink. This changes the effective area A of the internal heat path and also changes the external thermal resistance, θ_{C_1A}. The changes are functions of the thermocouple composition and size. The value of θ_{JC_1} is now determined by the effective area of contact of the thermocouple and its value remains constant when the attached thermocouple's size is held constant. k_1, $(= q_1/Q_t)$, also changes because q_1 is determined by the sum of θ_{JC_1} and θ_{C_1A}. The term $(T_J - T_A)$ is essentially constant within experimental error because q_1 is small compared to Q_t and the variations in q_1 do not measureably change the die temperature.

PLASTIC PACKAGE FRAME GEOMETRY



"A" PACKAGE

"B" PACKAGE

FIGURE 3

θ_{C_1A} decreases as the wire size of a copper-constantan thermocouple increases and it increases as the composition is changed from copper-constantan to iron constantan. The thermal conductivities of copper, iron, and constantan are respectively 0.9, 0.16, and 0.054 cal/°C-cm.

Data in Table 4 confirm the direction and change in $k_1\theta_{JC_1}$, with change in measuring system. Data were taken in the same oven ambient.

When the physical system for T_C measurement and the conditions for measurement are specified and held constant, values for $k_1\theta_{JC_1}$ are constants.

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A RELIABILITY CONSIDERATION

TABLE 4

VARIATIONS IN $k_i\theta_{JC_i}$ WITH MEASUREMENT SYSTEM (All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_1\theta_{C_1A}$	$k_1\theta_{JC_1}$
Test Device	0.005" Type "J" Thermocouple	127.6	52.2	75.4
Test Device	0.012" Type "J" Thermocouple	123.5	31.5	92.0
Linear Circuit	0.005" Type "T" Thermocouple	123.3	75.0	48.3

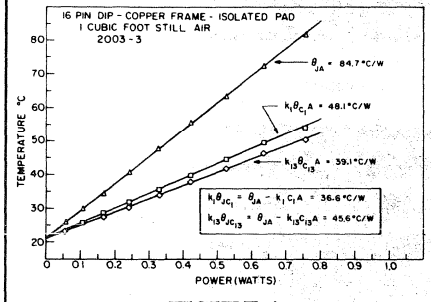


FIGURE 4

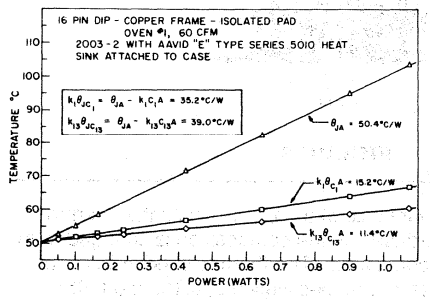


FIGURE 5

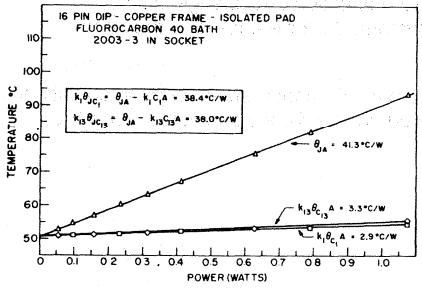


FIGURE 6

T_J MEASUREMENT FOR $k_i\theta_{JC_i}$ DETERMINATION

An accurate measurement of the value of $k_i\theta_{JC_i}$ requires a method of measuring the mean temperature of the die, T_J. Techniques to make this measurement have been discussed elsewhere. (See Ref. 2, 3, 4) They involve measurement of a temperature sensitive parameter of an element on the die. The forward voltage drop across a diode measured at constant current is a commonly used parameter. One must observe caution when applying the calibration data for an element in an unpowered die to the measured values of that element when the die is powered. It is rather unique if a parasitic voltage or current from the powered portion of the die does not interact with the temperature measuring element. This interaction leads to an inaccurate indication of the true temperature.

A test chip with a number of temperature sensitive elements is valuable. Figure 7 is a photo micrograph of a test chip designed to evaluate thermal resistance values for various packages as well as package surface interactions. The die contains 3 heat generators, and 6 primary temperature sensors, which are either diodes or special resistors. Parasitics normally interact differently with different elements because of location or structure variations. Agreement in the value of temperatures measured simultaneously for different elements on the chip normally indicates a correct measurement.

Figure 8 illustrates errors which can be introduced when making static steady state measurements of temperature during power application. Observe the plots of T_J (from V_{eb} calibration) versus P_D for three different diodes on the chip. Although the slopes of the plots after initial power agree within 10%, the initial portion of the curve indicates a negative thermal resistance and the offsets of the curves indicate a varying interaction at different power levels. Although calculation of thermal resistance by the slope method would introduce a similar error for all three diodes, the single power point method for calculating $k_i\theta_{JC_i}$, where $k_i\theta_{JC_i} = (T_J - T_{C_i})/P_D$, would introduce considerable and different levels of error in the calculated values for each diode measurement.

For example, if temperature measurements were made at a power level of 0.22 W, one would calculate a value of 44.6°C/W for $k_i\theta_{JC_i}$ using T_J from diode 7-15. 57.1°C/W using T_J from diode 7-5, and 63.8°C/W using T_J from diode 7-6. The true value which was verified by pulse measurements was 97°C/W.

THERMAL RESISTANCE—
A RELIABILITY CONSIDERATION

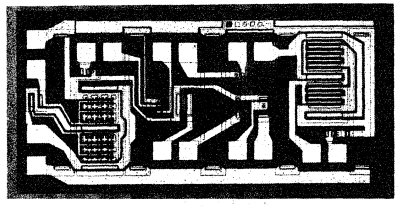


FIGURE 7

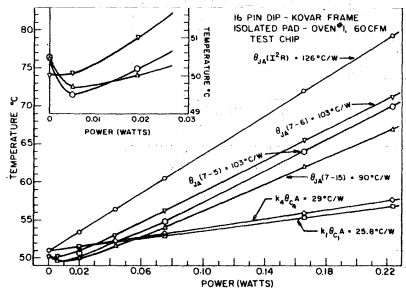


FIGURE 8

To eliminate interactions between the powered portion of a circuit and the temperature sensing element during measurement, the circuit shown in Figure 9 was developed. This circuit was designed for thermal evaluaton of packages in which the function could be a linear circuit, a digital circuit, or the standard test chip which has a number of different power sources and temperature sensing elements.

In operation, the circuit applies power at a measured level to the device under test for approximately one second, interrupts power for 40 microseconds, and continues this cycle throughout the test period. At the beginning of the 40-microsecond power off interval, a 10-microsecond delay allows circuit transients to decay before the diode current is activated. A 6-microsecond delay allows the current to settle before a sample and hold circuit samples the diode voltage to determine the chip temperature. This sequence allows the package under test to come to thermal equalibrium with the environment which approaches that for continuous power input. The power down sequence and temperature measurement interval are short enough to ensure that the actual temperature drop when power is removed is less than the sensitivity of the temperature sensitive element.

The case temperature measurements, T_{C_i}, can be made by thermocouple or by infra-red measurements.[4] In theory, the infra-red measurements would be preferred since a conductive contact is not made to the surface which is to be measured. In practice, a number of difficulties with I.R. measurements are encountered. The emissivity of the surface to be measured must be controlled to give accurate measurements. This normally requires painting the surface with a "proprietary" film. When the emissivity is mastered, two larger difficulties must be overcome; a) physically placing the infra-red measuring instrument into the system to view a package surface when the unit may be buried in a maze of printed wiring boards and circuitry and b) the cost of available instrumentation.

The thermocouple technique to measure case temperature is a practical and reliable method when the composition of the thermocouples, its physical size, its location on the package, and the method of its attachment are defined. The method of measurement can be standardized and provides an accurate, inexpensive method for the applications engineer or the reliability engineer to determine a reference temperature to which the temperature rise across the package path, $(k_i\theta_{JC_i})P_D$, can be applied in order to determine a true T_J.

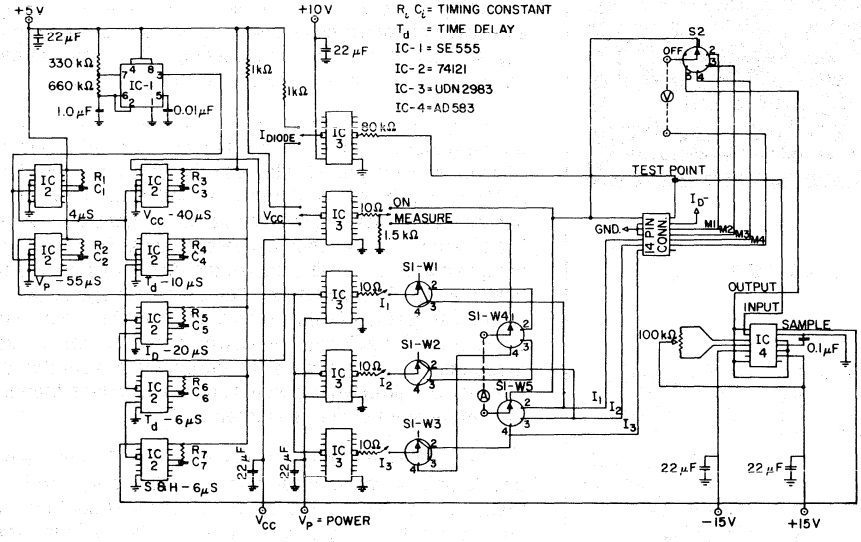


FIGURE 9

REFERENCES

1. S. Glasstone, *Textbook of Physical Chemistry,* 2nd Edition, D. Van Nostrand Co. Inc., New York, 1946

2. P. E. Roughan, *Thermal Resistance of Integrated Circuit Packages,* Technical Paper TP72-7, Sprague Electric Co., 1972

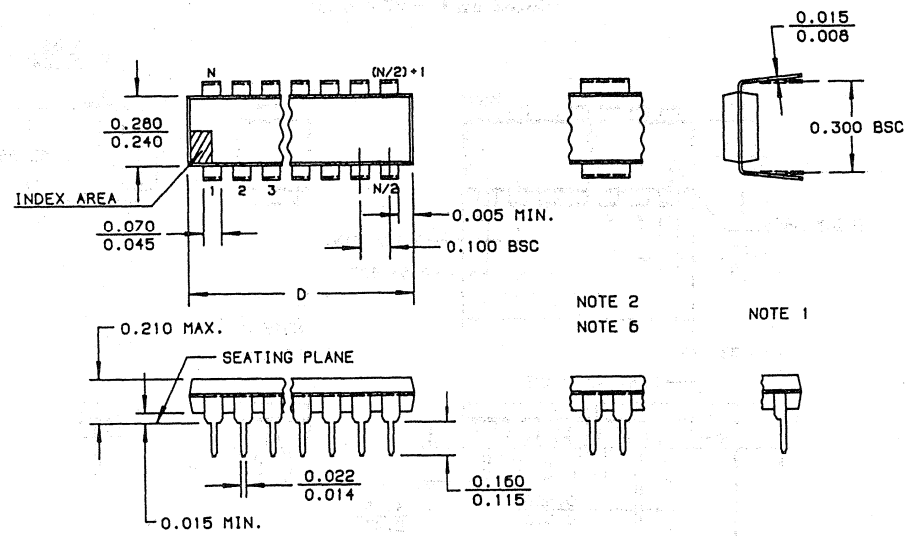
3. F. R. Dewey and P. R. Emerald, *Computing IC Temperature Rise,* Machine Design, pp 98-101, June 1977

4. C. A. Lidback, *Scanning I. R. Microscopy Techniques for Semiconductor Thermal Analysis.* 17th Annual Proceedings Reliability Physics 1979 IEEE Catalog No. 79CH1425-8 Phy.

PACKAGE OUTLINES

PLASTIC DIP
(0.300" row spacing)

PACKAGE DESIGNATORS A, B, or M
Dimensions in Inches



Dwg. MA-001 in

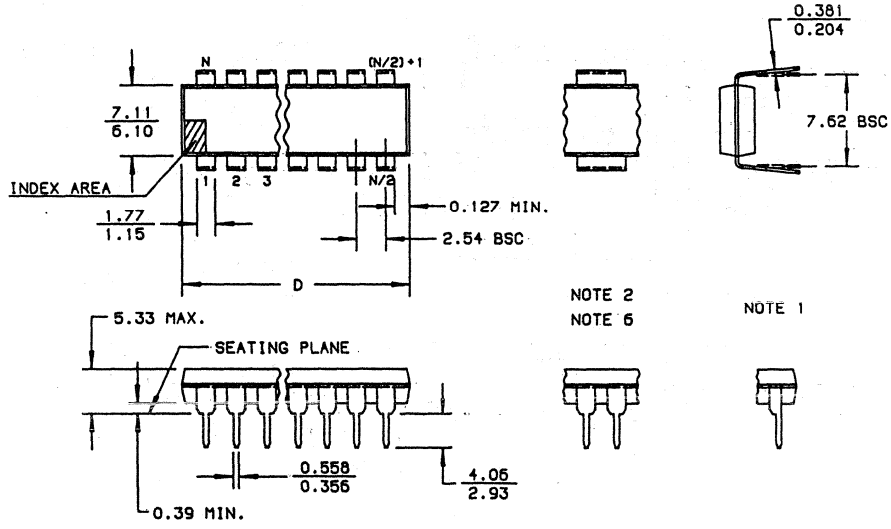
N	Number of Leads Pkg. Designator	8 M	14 A	16 A	16 B	18 A	20 A	24 B
D	Body Length	0.348/0.430	0.725/0.795	0.745/0.840	0.745/0.840	0.845/0.925	0.925/1.060	1.125/1.275
Notes	(Leads Affected)	1 (1, 4, 5, 8)	—	1 (1, 8, 9, 16)	1 (1, 8, 9, 16) 2 (4, 5, 12, 13) 3	—	—	2 (5-7, 18-20)
JEDEC Outline Designation		MS-001AB	MS-001AC	MS-001AA	—	MS-001AD	MS-001AE	MS-001AF

NOTES: 1. Leads 1, N/2, (N/2) + 1, and N may be half leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.
3. Maximum lead thickness is 0.020".
4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP
(7.62 mm row spacing)

PACKAGE DESIGNATORS A, B, or M
Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MA-001 mm

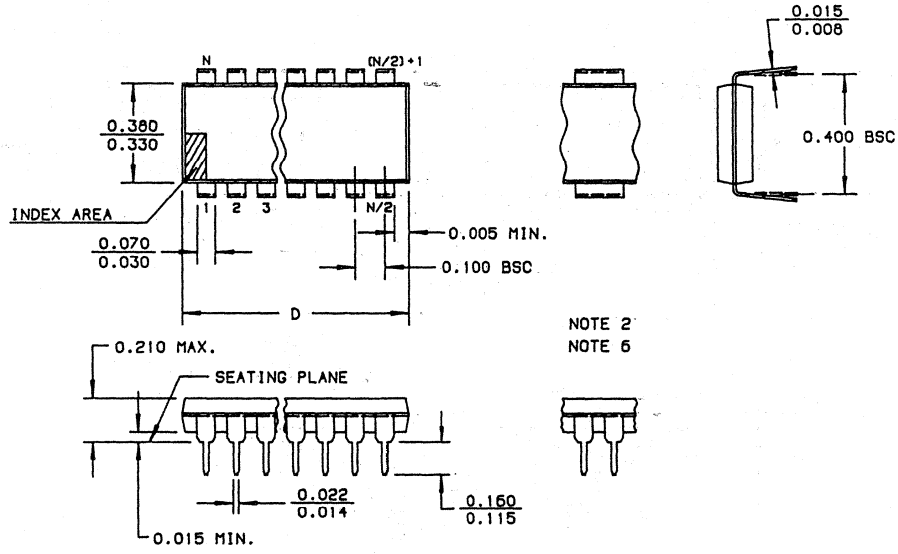
N	Number of Leads Pkg. Designator	8 M	14 A	16 A	16 B	18 A	20 A	24 B
D	Body Length	8.84/10.92	18.42/20.19	18.93/21.33	18.93/21.33	21.47/23.49	23.5/26.9	28.6/32.3
Notes	(Leads Affected)	1 (1, 4, 5, 8)	—	1 (1, 8, 9, 16)	1 (1, 8, 9, 16) 2 (4, 5, 12, 13) 3	—	—	2 (5-7, 18-20)
JEDEC Outline Designation		MS-001AB	MS-001AC	MS-001AA	—	MS-001AD	MS-001AE	MS-001AF

NOTES:
1. Leads 1, N/2, (N/2) + 1, and N may be half leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.
3. Maximum lead thickness is 0.508 mm.
4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP
(0.400" row spacing)

PACKAGE DESIGNATORS A or B
Dimensions in Inches



Dwg. MA-002 in

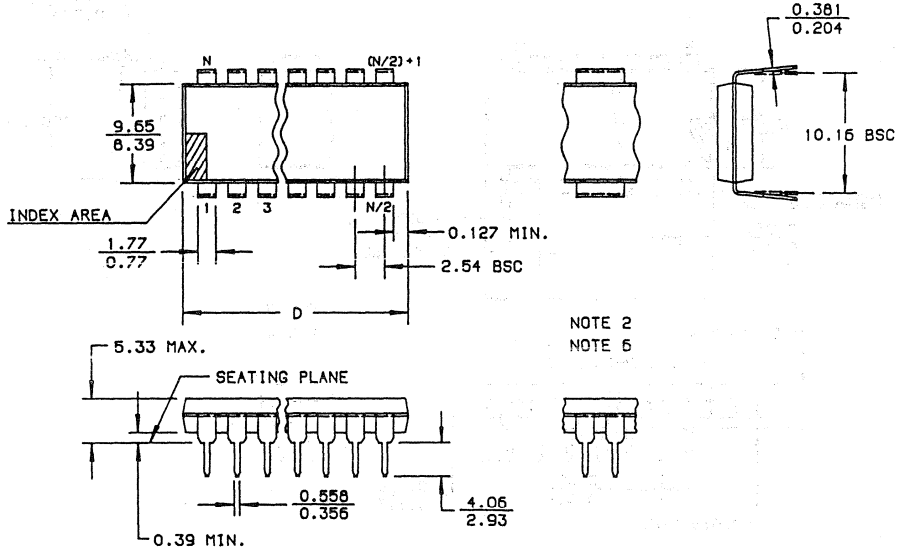
N	Number of Leads Pkg. Designator	22 A	22 B					
D	Body Length	1.050/1.120	1.050/1.120					
Notes	(Leads Affected)	—	2 (5, 6, 17, 18)					
JEDEC Outline Designation		MS-010AA	MS-010AA					

NOTES: 2. Webbed lead frame. Leads indicated are internally one piece.
4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP
(10.16 mm row spacing)

PACKAGE DESIGNATORS A or B
Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MA-002 mm

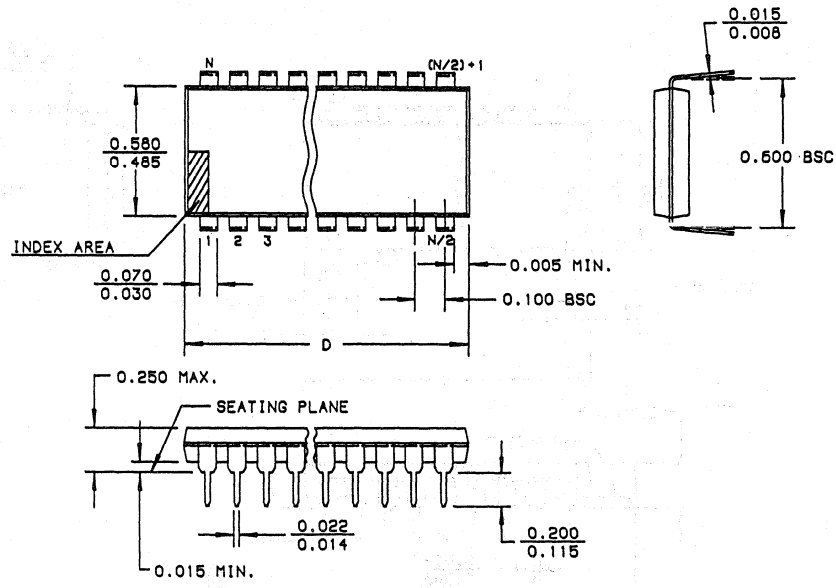
N	Number of Leads Pkg. Designator	22 A	22 B					
D	Body Length	26.67/28.44	26.67/28.44					
Notes	(Leads Affected)	—	2 (5, 6, 17, 18)					
JEDEC Outline Designation		MS-010AA	MS-010AA					

NOTES: 2. Webbed lead frame. Leads indicated are internally one piece.
4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP
(0.600" row spacing)

PACKAGE DESIGNATOR A
Dimensions in Inches



Dwg. MA-003 in

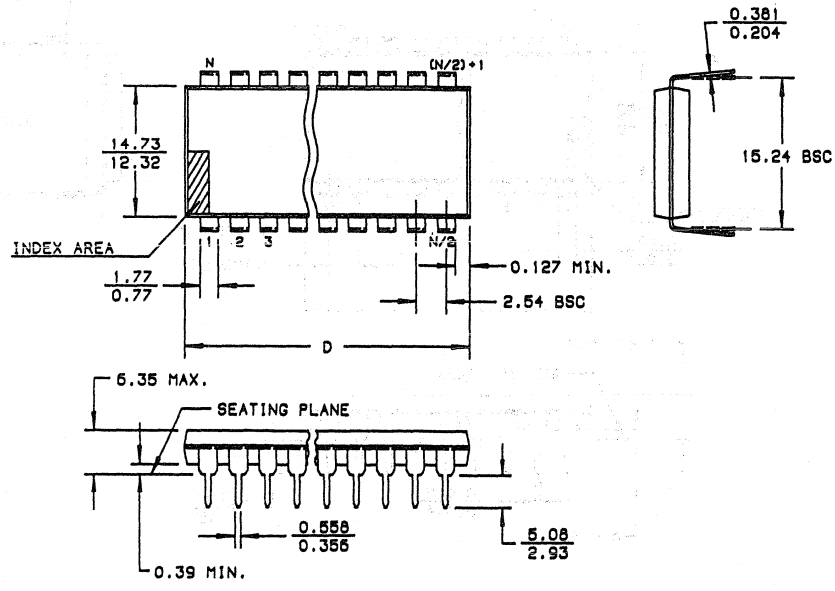
N	Number of Leads Pkg. Designator	28 A	40 A					
D	Body Length	1.380/1.565	1.980/2.095					
Notes		—	—					
JEDEC Outline Designation		MS-011AB	MS-011AC					

NOTES: 4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP
(15.24 mm row spacing)

PACKAGE DESIGNATOR A
Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MA-003 mm

N	Number of Leads Pkg. Designator	28 A	40 A					
D	Body Length	35.1/39.7	50.3/53.2					
Notes		—	—					
JEDEC Outline Designation		MS-011AB	MS-011AC					

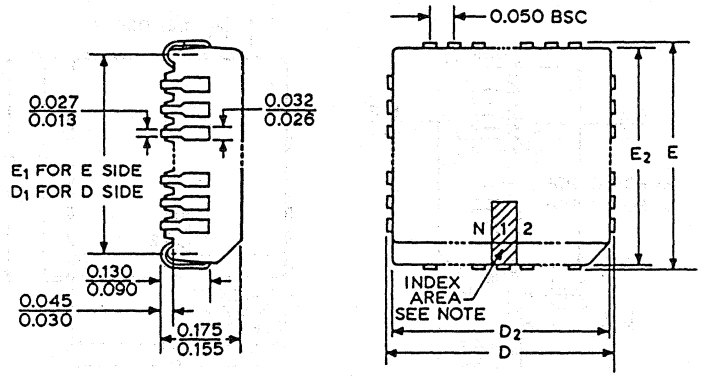
NOTES: 4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC LEADED CHIP CARRIER (PQCC)

PACKAGE DESIGNATORS EA, EB, or EP

Dimensions in Inches



Dwg. No. A-13,644 in

N	Number of Leads Pkg. Designator	20 EP	28 EA	28 EB	28 EP	44 EB	44 EP	
D	Overall Length	0.385/0.395	0.470/0.510	0.470/0.510	0.470/0.510	0.670/0.710	0.670/0.710	
D1	Row Spacing	0.290/0.330	—	—	—	—	—	
D2	Body Length	0.350/0.356	0.440/0.460	0.440/0.460	0.440/0.460	0.640/0.660	0.640/0.660	
E	Overall Width	0.385/0.395	0.470/0.510	0.470/0.510	0.470/0.510	0.670/0.710	0.670/0.710	
E1	Row Spacing	0.290/0.330	—	—	—	—	—	
E2	Body Width	0.350/0.356	0.440/0.460	0.440/0.460	0.440/0.460	0.640/0.660	0.640/0.660	
Notes	(Leads Affected)	—	2 (12-18)	2 (5-11, 19-25)	—	2 (7-17, 29-39)	—	
JEDEC Outline Designation		—	MS-007AA	MS-007AA	MS-007AA	MS-007AB	MS-007AB	

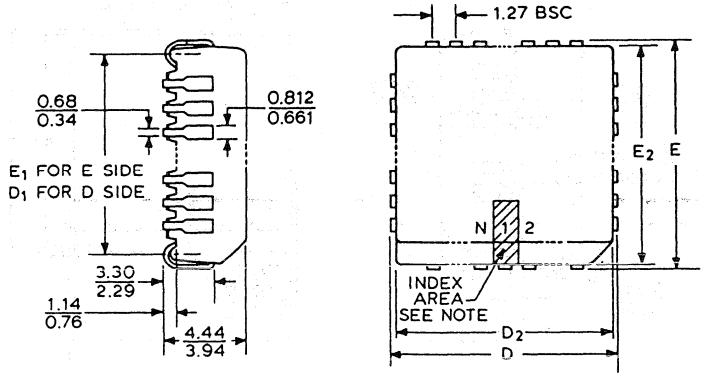
NOTES: 1. Index is centered on "D" side.
2. Webbed lead frame. Leads indicated are internally one piece.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC LEADED CHIP CARRIER (PQCC)

PACKAGE DESIGNATORS EA, EB, or EP

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. No. A-13,644 mm

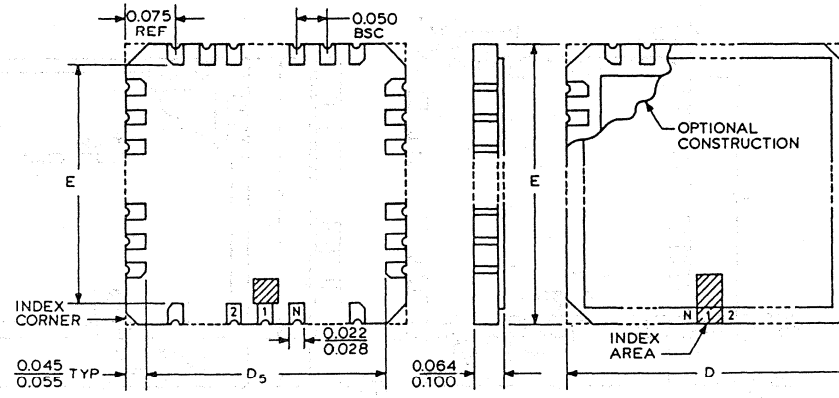
N	Number of Leads Pkg. Designator	20 EP	28 EA	28 EB	28 EP	44 EB	44 EP	
D	Overall Length	9.78/10.03	11.94/12.95	11.94/12.95	11.94/12.95	17.02/18.03	17.02/18.03	
D1	Row Spacing	8.89/9.042	—	—	—	—	—	
D2	Body Length	7.37/8.38	11.18/11.68	11.18/11.68	11.18/11.68	16.26/16.76	16.26/16.76	
E	Overall Width	9.78/10.03	11.94/12.95	11.94/12.95	11.94/12.95	17.02/18.03	17.02/18.03	
E1	Row Spacing	8.89/9.042	—	—	—	—	—	
E2	Body Width	7.37/8.38	11.18/11.68	11.18/11.68	11.18/11.68	16.26/16.76	16.26/16.76	
Notes	(Leads Affected)	—	2 (12-18)	2 (5-11, 19-25)	—	2 (7-17, 29-39)	—	
JEDEC Outline Designation		—	MS-007AA	MS-007AA	MS-007AA	MS-007AB	MS-007AB	

NOTES: 1. Index is centered on "D" side.
2. Webbed lead frame. Leads indicated are internally one piece.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

CERAMIC LEADLESS CHIP CARRIER (CQCC)

PACKAGE DESIGNATOR EK
Dimensions in Inches



Dwg. No. A-14,156

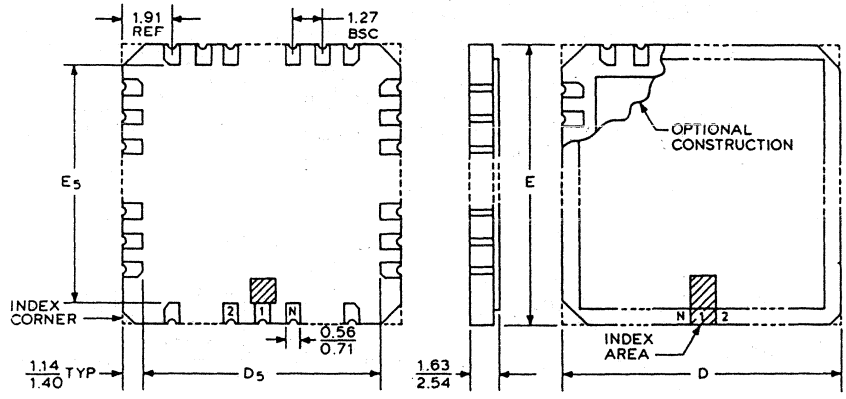
N	Number of Leads	20	28	44				
D	Overall Length	0.342/0.410	0.442/0.460	0.640/0.662				
D5	Contact Spacing	0.250 Ref.	0.350 Ref.	0.550 Ref.				
E	Overall Width	0.342/0.410	0.442/0.460	0.640/0.662				
E5	Contact Spacing	0.250 Ref.	0.350 Ref.	0.550 Ref.				
M38510F Case Outline		C-2	C-4	C-5				

NOTES: 1. Index is centered on "D" side.
2. Corner shape (square, notch, radius) optional.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

CERAMIC LEADLESS CHIP CARRIER (CQCC)

PACKAGE DESIGNATOR EK
Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. No. A-14,157

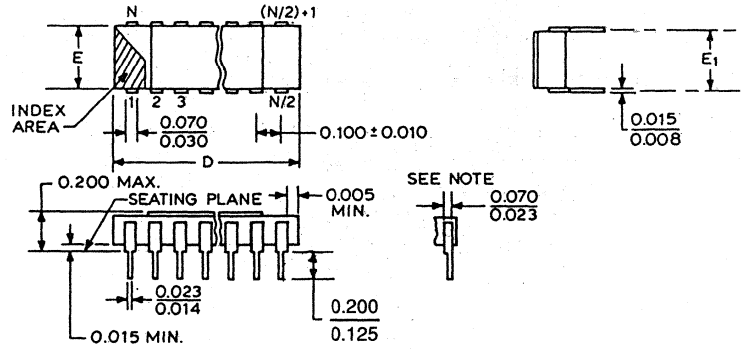
N	Number of Leads	20	28	44				
D	Overall Length	8.69/9.09	11.23/11.68	16.26/16.81				
D5	Contact Spacing	6.35 Ref.	8.89 Ref.	13.97 Ref.				
E	Overall Width	8.69/9.09	11.23/11.68	16.26/16.81				
E5	Contact Spacing	6.35 Ref.	8.89 Ref.	13.97 Ref.				
M38510F Case Outline		C-2	C-4	C-5				

NOTES: 1. Index is centered on "D" side.
2. Corner shape (square, notch, radius) optional.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

HERMETIC SIDE-BRAZED DIP

PACKAGE DESIGNATOR H
Dimensions in Inches



Dwg. No. A-13,646 in

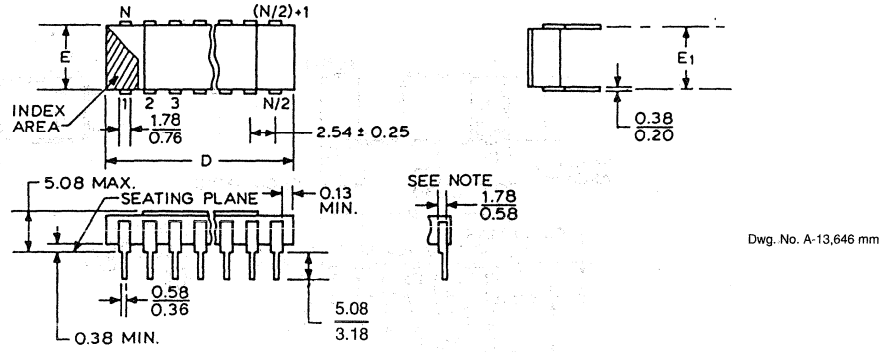
N	Number of Leads	8	14	16	18	20	22	
D	Body Length	0.528 Max.	0.785 Max.	0.840 Max.	0.960 Max.	1.060 Max.	1.260 Max.	
E	Body Width	0.220/0.310	0.220/0.310	0.220/0.310	0.220/0.310	0.220/0.310	0.350/0.390	
E1	Row Spacing	0.290/0.320	0.290/0.320	0.290/0.320	0.290/0.320	0.290/0.320	0.390/0.420	
Notes	(Leads Affected)	—	—	1 (1, 8, 9, 16)	—	—	—	
M38510F Case Outline		—	D-1 Conf. 3	D-2 Conf. 3	D-6 Conf. 3	D-8 Conf. 3	D-7 Conf. 3	

NOTES:
1. Leads 1, N/2, (N/2) + 1, and N may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.
5. Lead gauge plane is 0.030" below seating plane.

PACKAGE OUTLINES

HERMETIC SIDE-BRAZED DIP

PACKAGE DESIGNATOR H
Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. No. A-13,646 mm

N	Number of Leads	8	14	16	18	20	22	
D	Body Length	13.41 Max.	19.94 Max.	21.34 Max.	24.38 Max.	26.92 Max.	32.00 Max.	
E	Body Width	5.59/7.87	5.59/7.87	5.59/7.87	5.59/7.87	5.59/7.87	8.89/9.91	
E1	Row Spacing	7.37/8.13	7.37/8.13	7.37/8.13	7.37/8.13	7.37/8.13	9.91/10.67	
Notes	(Leads Affected)	—	—	1 (1, 8, 9, 16)	—	—	—	
M38510F Case Outline		—	D-1 Conf. 3	D-2 Conf. 3	D-6 Conf. 3	D-8 Conf. 3	D-7 Conf. 3	

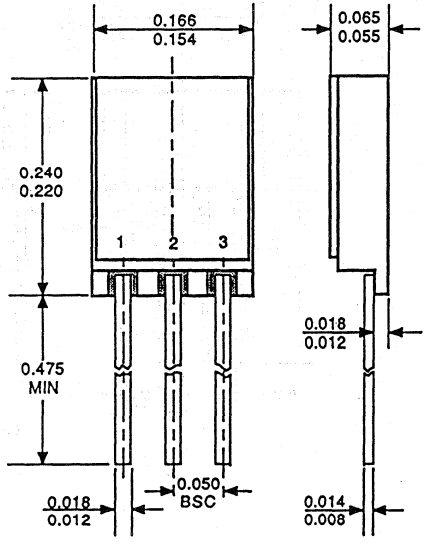
NOTES: 1. Leads1, N/2, (N/2) + 1, and N may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.
5. Lead gauge plane is 0.762 mm below seating plane.

PACKAGE OUTLINES

CERAMIC SIP
(TO-260AA)

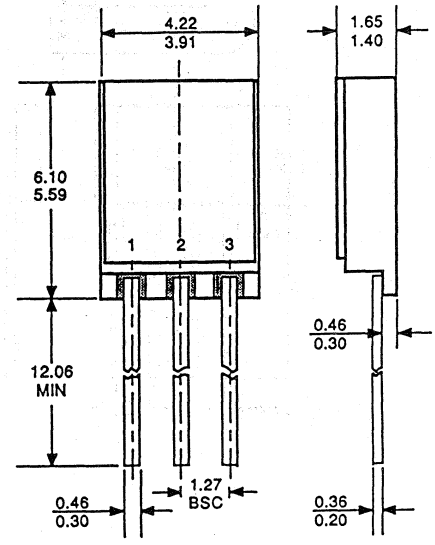
PACKAGE DESIGNATOR HH

Dimensions in Inches



Dwg. MH-012 in

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



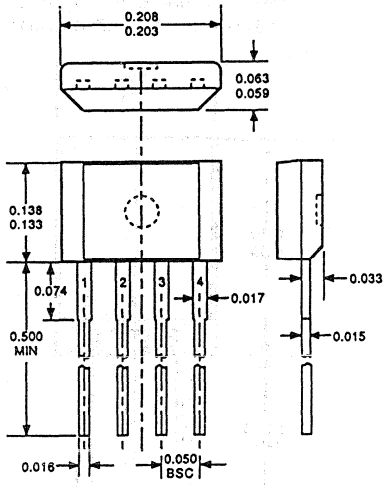
Dwg. MH-012 mm

PACKAGE OUTLINES

PLASTIC SIP

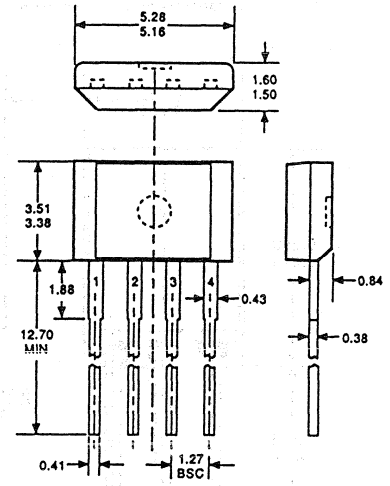
PACKAGE DESIGNATOR K

Dimensions in Inches



Dwg. MH-009 in

Dimensions in Millimeters (Based on 1" = 25.4 mm)



Dwg. MH-009 mm

NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).

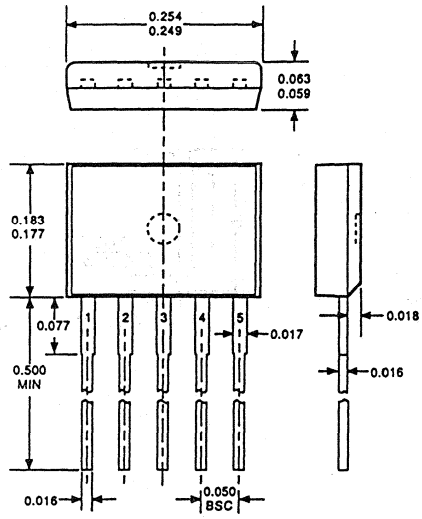
2. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC SIP

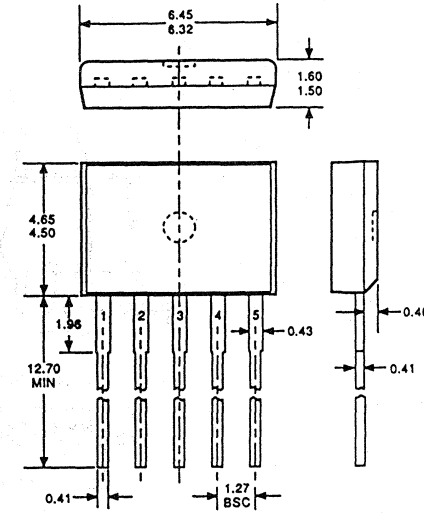
PACKAGE DESIGNATOR KA

Dimensions in Inches



Dwg. MH-010 in

Dimensions in Millimeters (Based on 1" = 25.4 mm)



Dwg. MH-010 mm

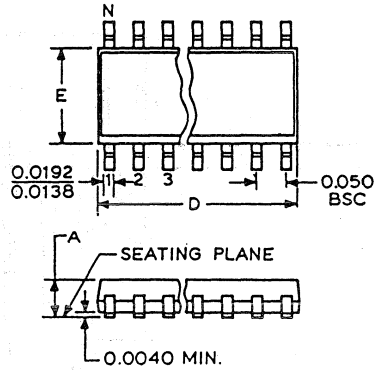
NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).

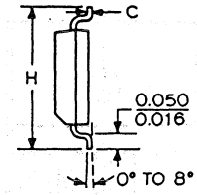
2. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC SOIC

PACKAGE DESIGNATORS L, LB, or LW
Dimensions in Inches
(Based on 1 mm = 0.3937")





Dwg. No. A-13,648 in

N	Number of Leads Pkg. Designator	8 L	14 L	16 L	18 LW	20 LB	24 LB	28 LW
A	Seated Height	0.0532/0.0688	0.0532/0.0688	0.0532/0.0688	0.0926/0.1043	0.0926/0.1043	0.0926/0.1043	0.0926/0.1043
C	Lead Thickness	0.0075/0.0098	0.0075/0.0098	0.0075/0.0098	0.0091/0.0125	0.0091/0.0125	0.0091/0.0125	0.0091/0.0125
D	Body Length	0.1890/0.1968	0.3367/0.3444	0.3859/0.3937	0.4469/0.4625	0.4961/0.5118	0.5985/0.6141	0.6969/0.7125
E	Body Width	0.1497/0.1574	0.1497/0.1574	0.1497/0.1574	0.2914/0.2992	0.2914/0.2992	0.2914/0.2992	0.2914/0.2992
H	Overall Width	0.2284/0.2440	0.2284/0.2440	0.2284/0.2440	0.394/0.419	0.394/0.419	0.394/0.419	0.394/0.419
Notes	(Leads Affected)	—	—	—	—	1 (4-7, 14-17)	1 (6, 7, 18, 19)	—
JEDEC Outline Designation		MS-012AA	MS-012AB	MS-012AC	MS-013AB	MS-013AC	MS-013AD	MS-013AE

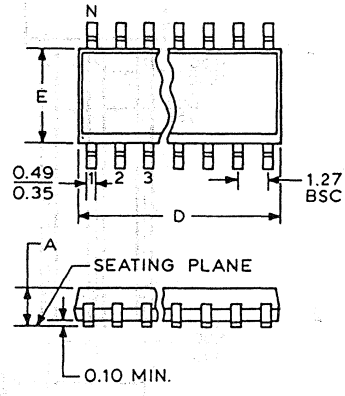
NOTES: 1. Webbed lead frame. Leads indicated are internally one piece.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.

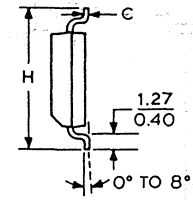
PACKAGE OUTLINES

PLASTIC SOIC

PACKAGE DESIGNATORS L, LB, or LW

Dimensions in Millimeters





Dwg. No. A-13,648 mm

N	Number of Leads Pkg. Designator	8 L	14 L	16 L	18 LW	20 LB	24 LB	28 LW
A	Seated Height	1.35/1.75	1.35/1.75	1.35/1.75	2.35/2.65	2.35/2.65	2.35/2.65	2.35/2.65
C	Lead Thickness	0.19/0.25	0.19/0.25	0.19/0.25	0.23/0.32	0.23/0.32	0.23/0.32	0.23/0.32
D	Body Length	4.80/5.0	8.55/8.75	9.80/10.0	11.35/11.75	12.60/13.00	15.20/15.60	17.70/18.10
E	Body Width	3.80/4.00	3.80/4.00	3.80/4.00	7.40/7.60	7.40/7.60	7.40/7.60	7.40/7.60
H	Overall Width	5.80/6.20	5.80/6.20	5.80/6.20	10.00/10.65	10.00/10.65	10.00/10.65	10.00/10.65
Notes	(Leads Affected)	—	—	—	—	1 (4-7, 14-17)	1 (6, 7, 18, 19)	—
JEDEC Outline Designation		MS-012AA	MS-012AB	MS-012AC	MS-013AB	MS-013AC	MS-013AD	MS-013AE

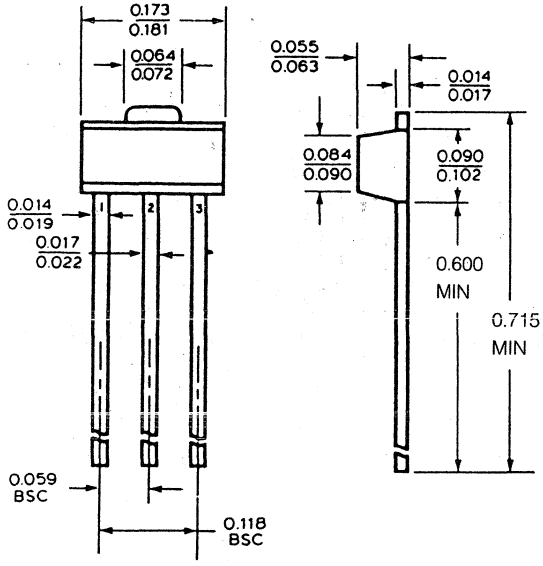
NOTES: 1. Webbed lead frame. Leads indicated are internally one piece.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

LONG-LEADED PLASTIC SOT

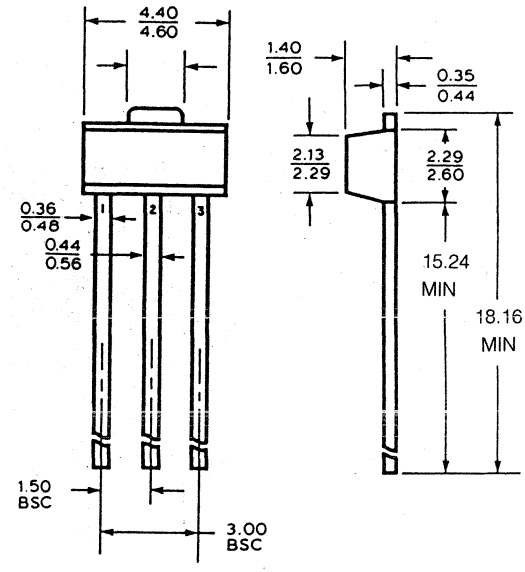
PACKAGE DESIGNATOR LL

Dimensions in Inches
(Based on 1 mm = 0.394")



Dwg. No. A-12,657A in

Dimensions in Millimeters



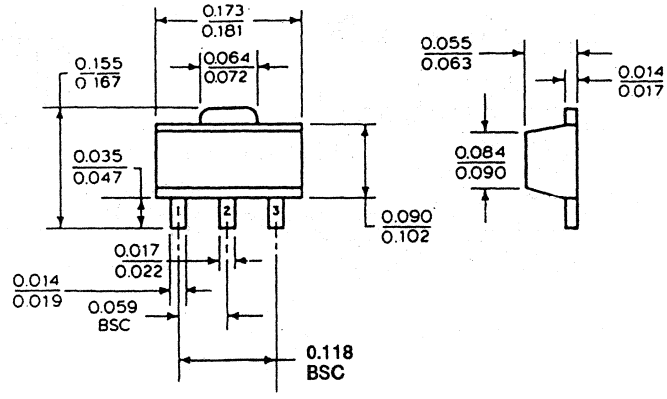
Dwg. No. A-12,657A mm

PACKAGE OUTLINES

PLASTIC SOT (SOT-89/TO-243AA)

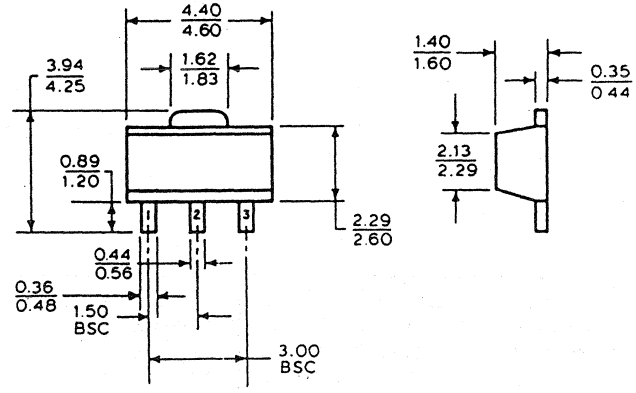
PACKAGE DESIGNATOR LT

Dimensions in Inches
(Based on 1 mm = 0.394")



Dwg. No. A-12,608A in

Dimensions in Millimeters

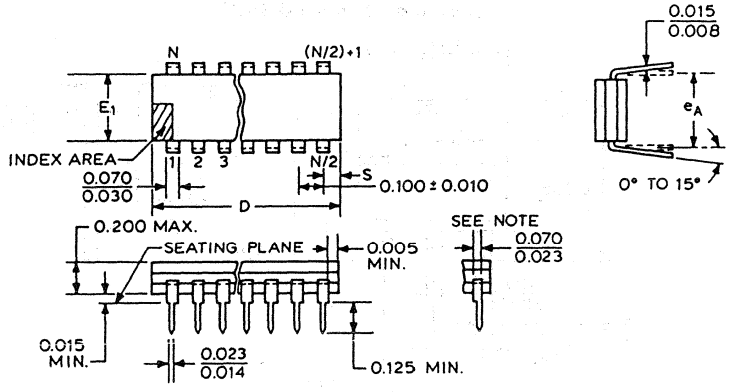


Dwg. No. A-12,608A mm

PACKAGE OUTLINES

HERMETIC CerDIP

PACKAGE DESIGNATOR R
Dimensions in Inches



Dwg. No. A-13,650 in

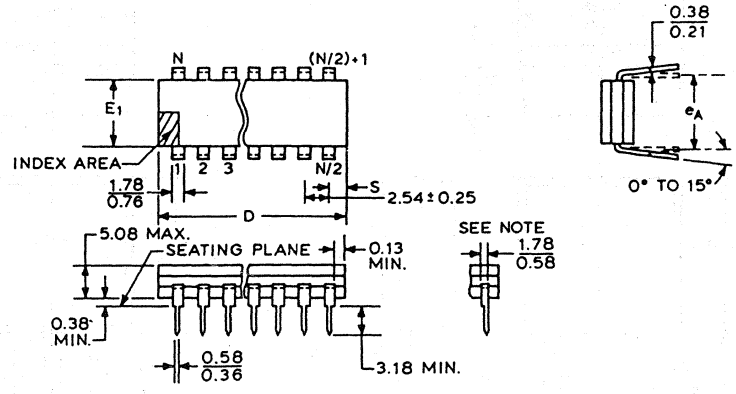
N	Number of Leads	14	16	18	22			
D	Body Length	0.785 Max.	0.840 Max.	0.960 Max.	1.260 Max.			
E1	Body Width	0.220/0.310	0.220/0.310	0.220/0.310	0.350/0.390			
eA	Row Spacing	0.300 BSC	0.300 BSC	0.300 BSC	0.400 BSC			
S	Lead CL to End	0.075 Ref.	0.025 Ref.	0.050 Ref.	0.025 Ref.			
Notes	(Leads Affected)	—	1 (1, 8, 9, 16)	—	—			
M38510F Case Outline		D-1 Conf. 1	D-2 Conf. 1	D-6 Conf. 1	D-7 Conf. 1			

NOTES: 1. Leads 1, N/2, (N/2) + 1, and N may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.
5. Lead gauge plane is 0.030" below seating plane.

PACKAGE OUTLINES

HERMETIC CerDIP

PACKAGE DESIGNATOR R
Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. No. A-13,650 mm

N	Number of Leads	14	16	18	22			
D	Body Length	19.94 Max.	21.34 Max.	24.38 Max.	32.00 Max.			
E1	Body Width	5.59/7.87	5.59/7.87	5.59/7.87	8.89/9.91			
eA	Row Spacing	7.62 BSC	7.62 BSC	7.62 BSC	10.16 BSC			
S	Lead CL to End	1.91 Ref.	0.64 Ref.	1.27 Ref.	1.27 Ref.			
Notes	(Leads Affected)	—	1 (1, 8, 9, 16)	—	—			
M38510F Case Outline		D-1 Conf. 1	D-2 Conf. 1	D-6 Conf. 1	D-7 Conf. 1			

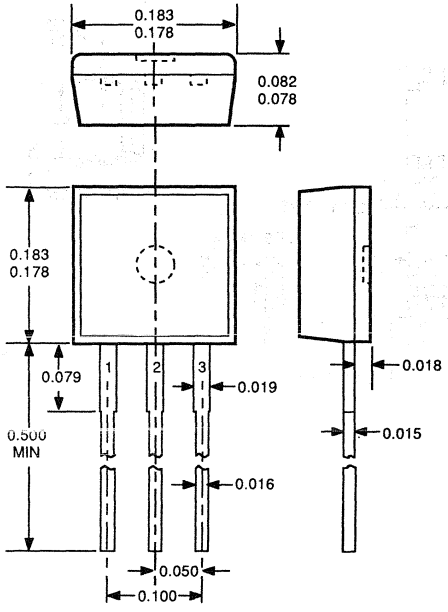
NOTES: 1. Leads 1, N/2, (N/2) + 1, and N may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.
5. Lead gauge plane is 0.762 mm below seating plane.

PACKAGE OUTLINES

PLASTIC SIP

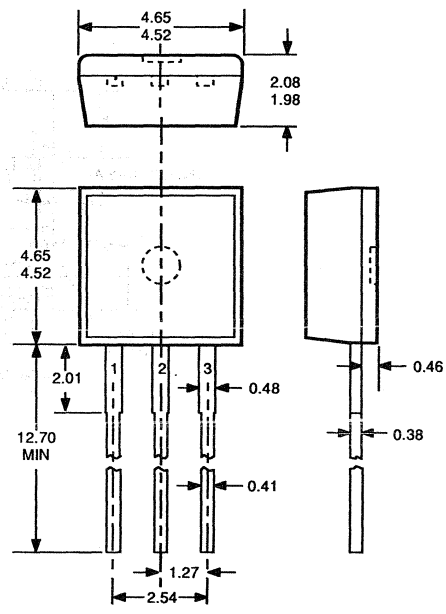
PACKAGE DESIGNATORS T and TA

Dimensions in Inches



Dwg. MH-004 in

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MH-004 mm

NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).

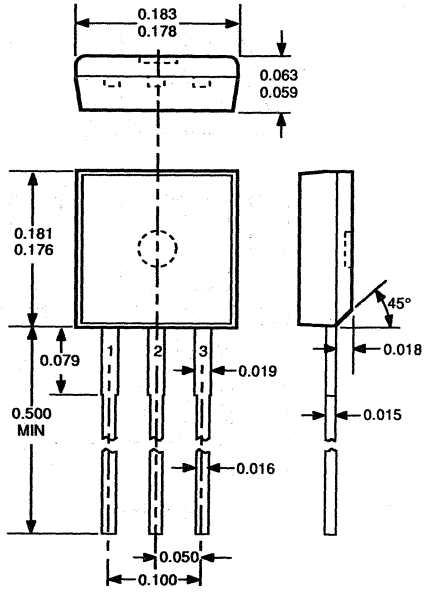
2. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC SIP

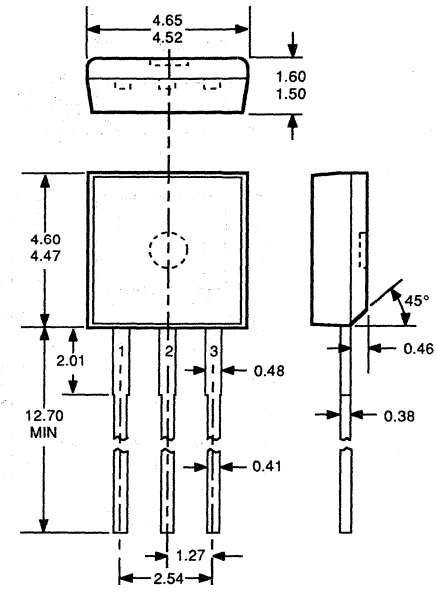
PACKAGE DESIGNATOR U

Dimensions in Inches



Dwg. MH-003 in

Dimensions in Millimeters (Based on 1" = 25.4 mm)



Dwg. MH-003 mm

NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).

2. Exact body and lead configuration at vendor's option within limits shown.

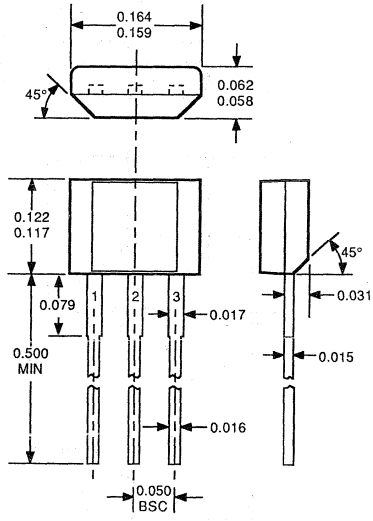
3. Height does not include mold gate flash.

PACKAGE OUTLINES

PLASTIC SIP

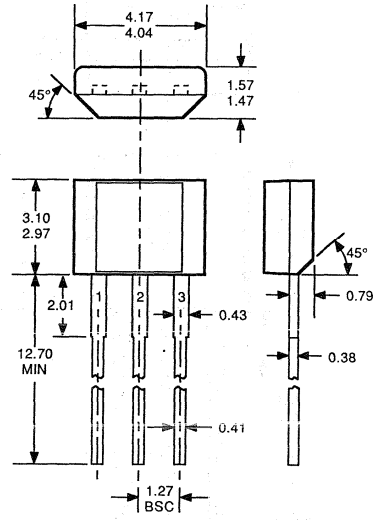
PACKAGE DESIGNATOR UA

Dimensions in Inches



Dwg. MH-014 in

Dimensions in Millimeters (Based on 1" = 25.4 mm)



Dwg. MH-014 mm

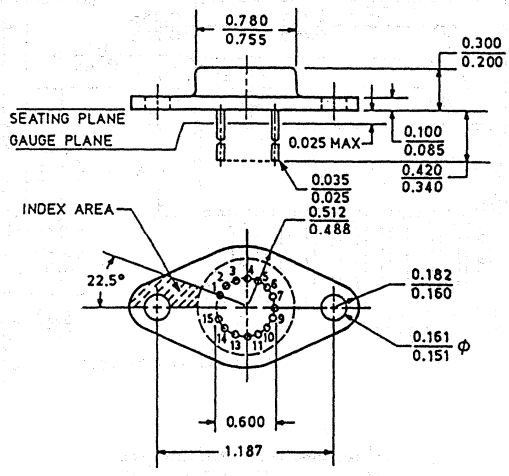
NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.

PACKAGE OUTLINES

HERMETIC FLANGE MOUNT (MO-097AA)

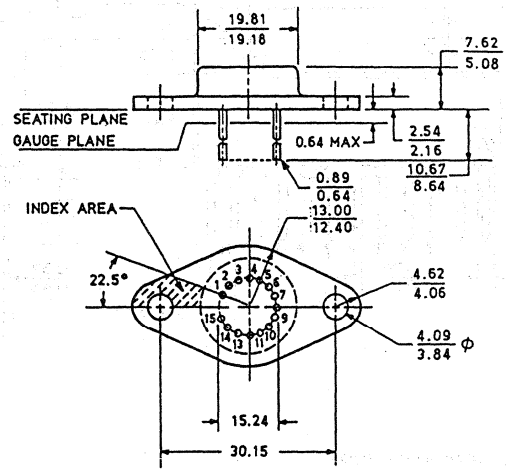
PACKAGE DESIGNATOR V

Dimensions in Inches



Dwg. MM-001 in

Dimensions in Millimeters (Based on 1" = 25.4 mm)



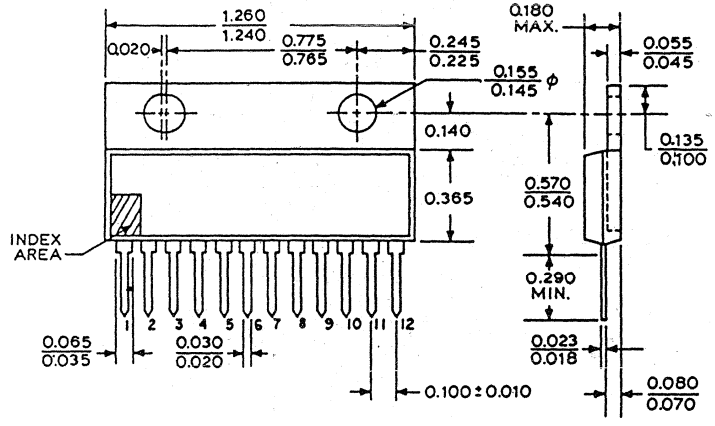
Dwg. MM-001 mm

PACKAGE OUTLINES

PLASTIC POWER-TAB SIP

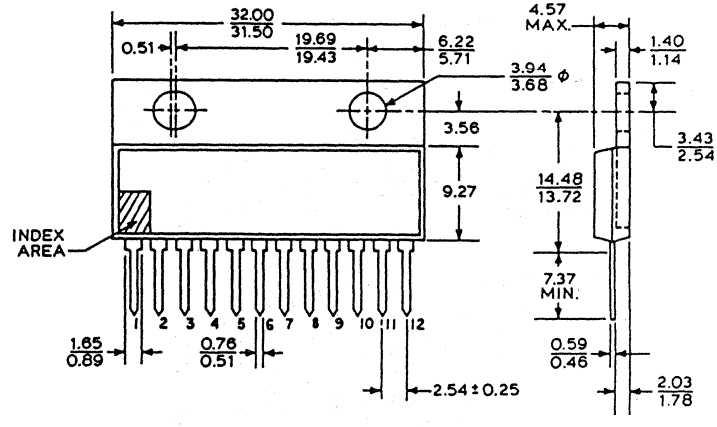
PACKAGE DESIGNATOR W

Dimensions in Inches



Dwg. No. A-13,652 in

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. No. A-13,652 mm

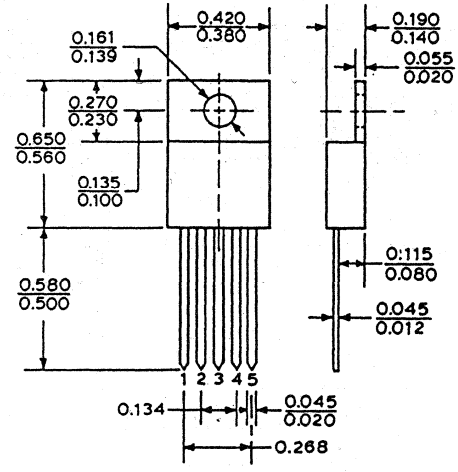
NOTES: 1. Lead thickness is measured at seating plane or below.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. Lead gauge plane is 0.030" (0.762 mm) below seating plane.

PACKAGE OUTLINES

PLASTIC POWER-TAB SIP

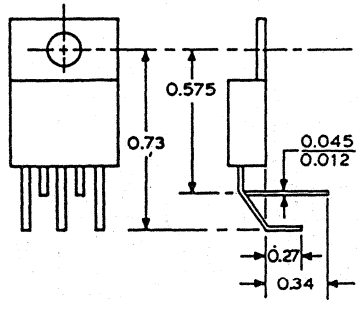
PACKAGE DESIGNATORS Z, ZH, or ZV
Dimensions in Inches

DESIGNATOR Z
(JEDEC Outline TO-220AB
except for number of leads)



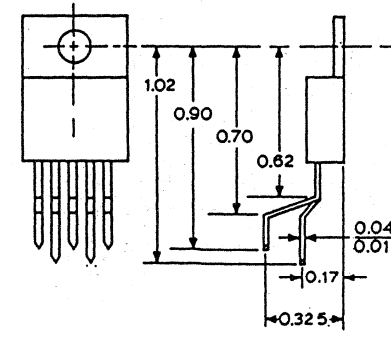
Dwg. No. A-13,654 in

DESIGNATOR ZH
(Package Z except as shown)



Dwg. No. A-13,655 in

DESIGNATOR ZV
(Package Z except as shown)



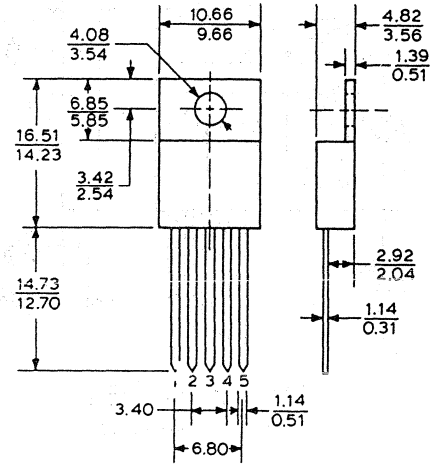
Dwg. No. A-13,656 in

PACKAGE OUTLINES

PLASTIC POWER-TAB SIP

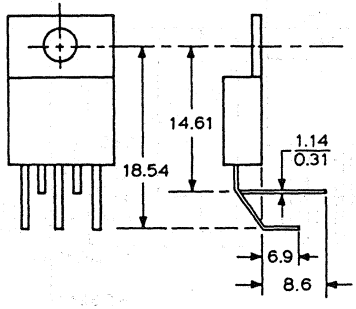
PACKAGE DESIGNATORS Z, ZH, or ZV
Dimensions in Millimeters
(Based on 1" = 25.4 mm)

DESIGNATOR Z
(JEDEC Outline TO-220AB
except for number of leads)



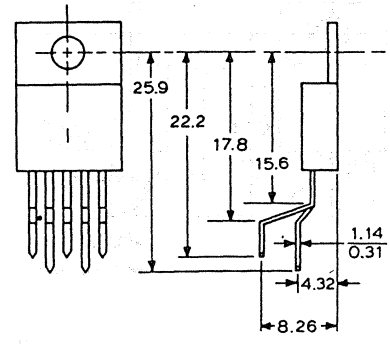
Dwg. No. A-13,654 mm

DESIGNATOR ZH
(Package Z except as shown)



Dwg. No. A-13,655 mm

DESIGNATOR ZV
(Package Z except as shown)

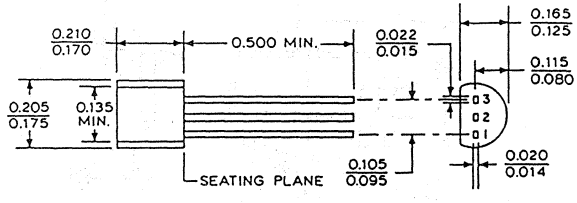


Dwg. No. A-13,656 mm

PACKAGE OUTLINES

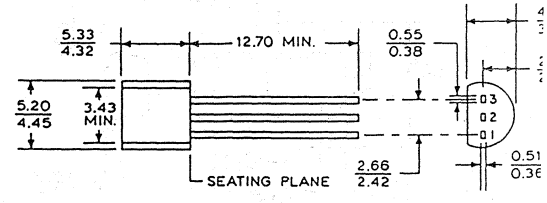
PLASTIC TRANSISTOR (TO-92/TO-226AA)

Dimensions in Inches

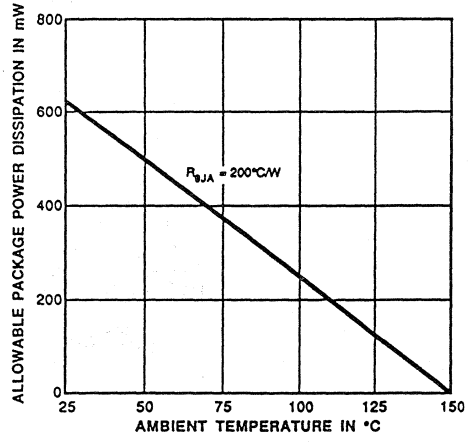


Dwg. No. A-13,610

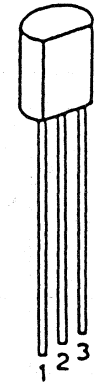
Dimensions in Millimeters (Based on 1" = 25.4 mm)



Dwg. No. A-13,611



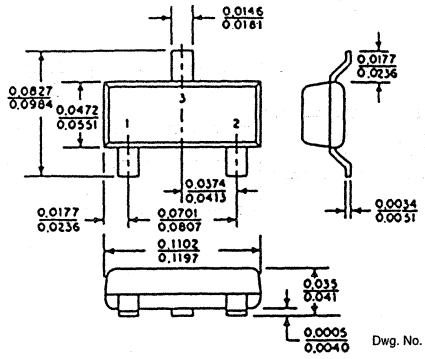
Dwg. GD-001



PACKAGE OUTLINES

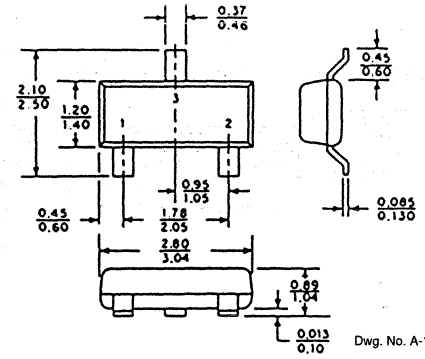
PLASTIC SMALL-OUTLINE TRANSISTOR (SOT-23/TO-236AB)

Dimensions in Inches (Based on 1 mm = 0.3937")

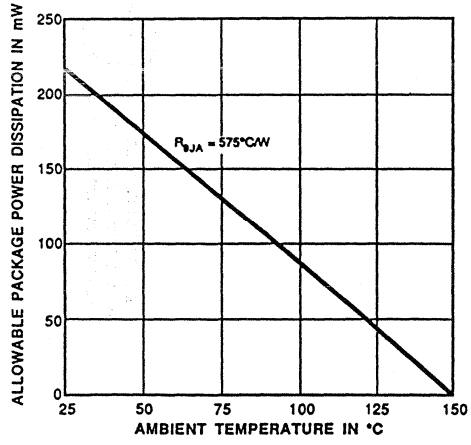


Dwg. No. A-12,238B in

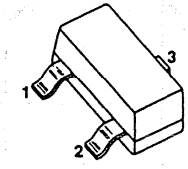
Dimensions in Millimeters



Dwg. No. A-12,238B in



Dwg. GD-002



Die size = 0.025" by 0.025" (0.635 mm by 0.635 mm). Other factors that determine allowable package power dissipation include circuit board material, pad size, and proximity of other heat-producing circuit elements.

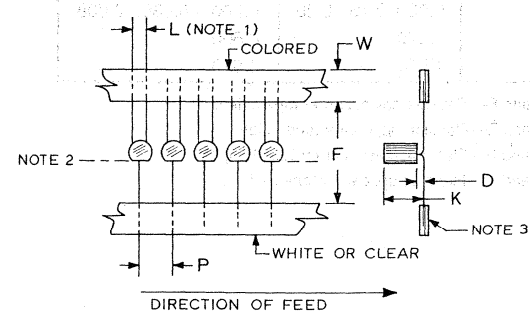
PACKAGE INFORMATION

TAPE AND REEL INFORMATION FOR DISCRETE DEVICES

AXIAL-TAPED TO-226AA TAPE DIMENSIONS

Dimensions	Millimeters	Inches
D Min.	0.38	0.015
D Max.	1.78	0.070
F Typ.	6.35	0.250
K Max.	6.73	0.265
L	2.54 ± 0.38	0.100 ± 0.015
P	6.35 ± 0.38	0.250 ± 0.015
W Min.	20.63	0.812
W Max.	22.15	0.872

NOTES: 1. Leads straight with 0.38 mm (0.015 in.) between body and type.
2. Component bodies in line within 0.38 mm (0.015 in.).
3. Lead length in contact with tape, each side, 1.78 mm (0.070 in.), minimum.

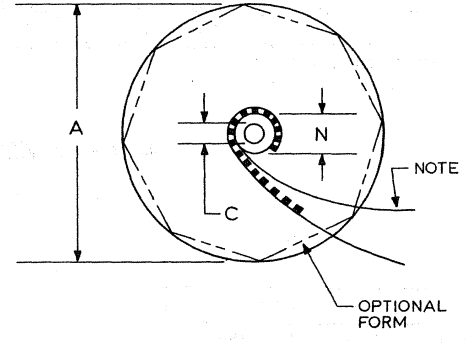


Dwg. No. A-13,626

REEL DIMENSIONS

Dimensions	Millimeters	Inches
A Max.	355.6	14
C	14.29	0.563
N Min.	76.20	3.0

NOTES: 1. Kraft paper, minimum 0.13 mm (0.005 in.) thick, as interliner.



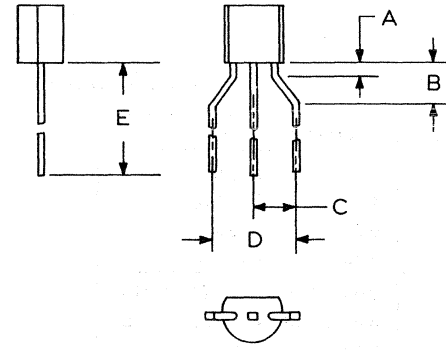
Dwg. No. A-13,627

TAPE AND REEL INFORMATION FOR DISCRETE DEVICES

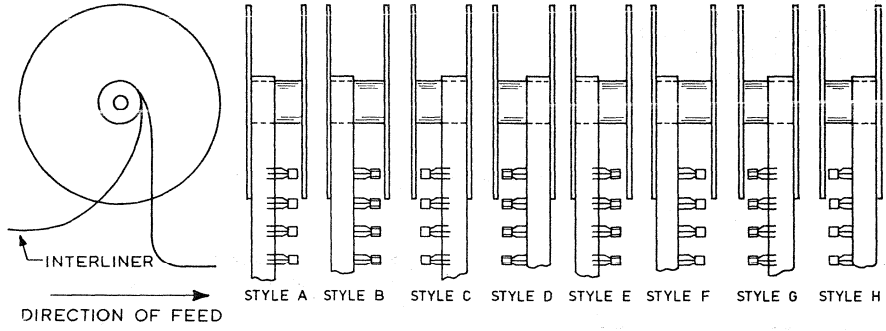
RADIAL-TAPED TO-226AA LEAD DIMENSIONS

Dimensions	Millimeters	Inches
A	1.52 ± 0.38	0.060 ± 0.015
B	3.18 ± 0.38	0.125 ± 0.015
C	2.54 ± 0.30	0.100 ± 0.012
D	5.08 ± 0.76, -0.20	0.200 + 0.030, -0.008
E Min.	12.70	0.500
E Max.	15.70	0.620

Styles A and F—Flat side down, carrier tape to left.
Styles B and E—Flat side up, carrier tape to left.
Styles C and H—Flat side down, carrier tape to right.
Styles D and G—Flat side up, carrier tape to right.



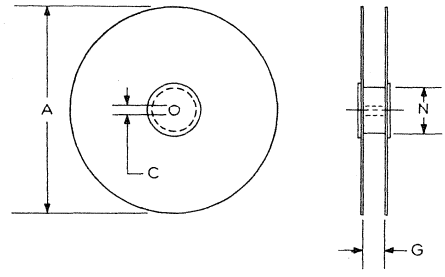
Dwg. No. A-13,628



Dwg. No. A-13,629

REEL DIMENSIONS

Dimensions	Millimeters	Inches
A	355.6 ± 6.35	14 ± 0.250
C	21.59 ± 6.35	0.850 ± 0.250
G	45.72 ± 7.62	1.800 ± 0.300
N Min.	76.20 ± 6.35	3.0 ± 0.250



Dwg. No. A-13,630

TAPE AND REEL INFORMATION FOR DISCRETE DEVICES

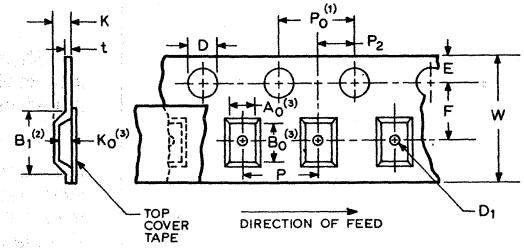
TAPE DIMENSIONS FOR TO-236AB

Dimensions	Millimeters	Inches
B_1 Max.[2]	4.2	0.165
D	1.5 (+0.10, -0.0)	0.059 (+0.004, -0.0)
D_1 Min.	1.0	0.039
E	1.75 (±0.10)	0.69 (±0.004)
F	3.5 (±0.05)	0.138 (±0.002)
K Max.	2.4	0.094
P	4.0 (±0.10)	0.157 (±0.004)
P_0[1]	4.0 (±0.10)	0.157 (±0.004)
P_2	2.0 (±0.05)	0.079 (±0.002)
R Min.	25	0.984
t Max.	0.400	0.016
t_1 Max.	0.10	0.004
W	8.0 (±0.30)	0.315 (±0.012)

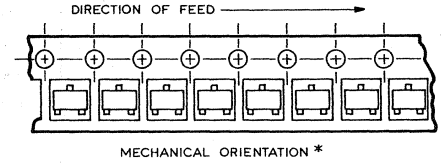
[1] Cumulative tolerance over 10 pitches = ±0.2 mm (±0.08 in.).

[2] For machine reference only, including draft and radii concentric around B_0.

[3] A_0, B_0, and K_0 are determined by component size. Clearance between the component and the cavity must be within 0.05 mm (0.002 in.), minimum, 0.50 mm (0.020 in.), maximum, for 8 mm tape; it must be within 0.05 (0.002 in.), minimum 0.65 mm (0.026 in.), maximum, for 12 mm tape.

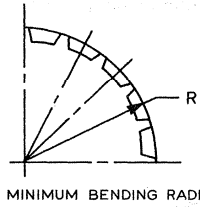


Dwg. No. A-13,310

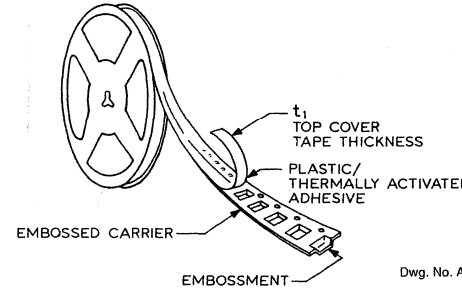


Dwg. No. A-13,313

*Available on request with double leads toward sprocket holes.



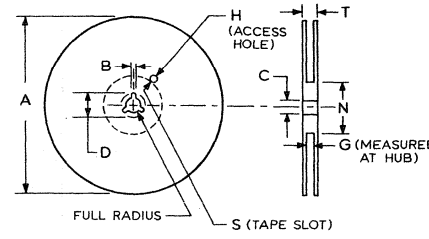
Dwg. No. A-13,312



Dwg. No. A-13,312

REEL DIMENSIONS FOR TO-236AB

Dimensions	Millimeters	Inches
A Max.	330	12.992
B Min.	1.5	0.059
C	13.0 (±0.20)	0.512 (±0.008)
D Min.	20.2	0.795
G	8.4 (+1.5, -0.0)	0.331 (+0.059, -0.0)
H Min.	40	1.575
N Min.	50	1.973
S Min.	2.5 Wide	0.098 Wide
	10 Deep	0.394 Deep
T Max.	14.4	0.567



Dwg. No. A-13,314

TO-236 AB

SHIPPING

Shipping options for small-outline transistors and diodes include vial pack and 8 mm tape and reel for use with automated insertion equipment.

The 8 mm tape pack puts 3000 devices on a 7-inch (178 mm) reel. Components can be placed in the tape cavity with the single lead toward the sprocket hole or with the double leads toward the sprocket hole. Tape and reel dimensions conform to EIA Standard 481 Rev. A.

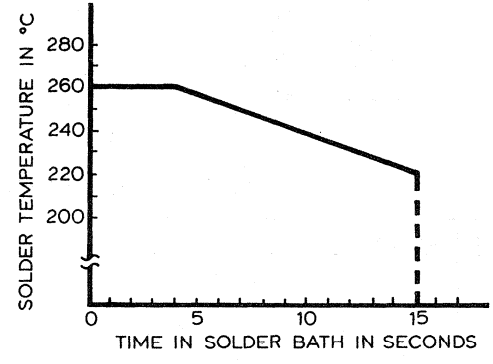
MOUNTING

Surface-mount semiconductors can be attached to substrates by conventional techniques such as vapor-phase or wave soldering and hot-plate methods.

Recommended maximum time/temperature soldering conditions are shown in the graph. In general, attachment with a soldering iron is not recommended due to the difficulty of consistently controlling temperature and time temperature.

CLEANING

Small-outline semiconductors are compatible with most commonly used defluxing solvents. Freon-based alcohol compounds such as Du Pont TMS or TES (or equivalents) are recommended. Solutions containing methylene chloride or other known epoxy solvents should not be used.



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